W88227F/W88227QD

ATAPI CD-ROM Decoder and uP8032

Draft Rev. 0.7

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W88227F/W88227QD Data Sheet Revision History

	Pages	Dates	Rev.	Version on Web	Main Contents
1	N/A	04/1999	0.40		First published, without DC/AC spec.
2	3, 8, 9, 12, 15, 34, 57, 63, 73, 75, 98-101	05/18/1999	0.50		With DC/AC spec.
3	12, 17, 18, 25, 26, 33, 42, 50, 60, 62, 86, 87	7/1999	0.60		Erroneous content/figure fix
4		10/1/1999	0.70		Add Diagram of Equivalent Circuit Add Absolute Maximum Ratings Add AC Timing Add IR Re-flow Profile Remove Application Circuit Add W88227QD package
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LIFE SUPPORT APPLICATIONS

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1. Overview

1.1 Features

Decoder

⇒ Supports ATAPI CD-ROM standard (SFF 8020)
⇒ Supports CD-ROM, CD-ROM/XA, CD-I, Video-CD, Photo-CD, CD-Plus, and i-trax formats
⇒ Supports drive speed up to 60-fold
⇒ Supports various types of DSPs
⇒ Supports various types of industry-standard DRAMs (256K*16 ~ 64K*16, 256K*8, 128K*8)
⇒ Supports real-time correction and buffer-independent-correction
⇒ Supports automatic repeated error correction
⇒ 32-byte FIFO to improve IDE interface throughput
⇒ Support data transfer to host in PIO, DMA , and UDMA/66 mode
⇒ Support block-offset-address-transfer and linear-address-transfer
⇒ Support automatic ATAPI hardware macro
⇒ Support automatic target header search and header comparison
⇒ Support automatic cache buffer management and transfer
⇒ Support Q-channel data extraction
⇒ Support high-speed CAV audio playback from DRAM buffer
⇒ Support left and right channels routing and muting
⇒ Support IEC-958 digital audio output
⇒ Programmable system clock for decoder operation
⇒ Support flash programming through IDE interface

Micro-controller

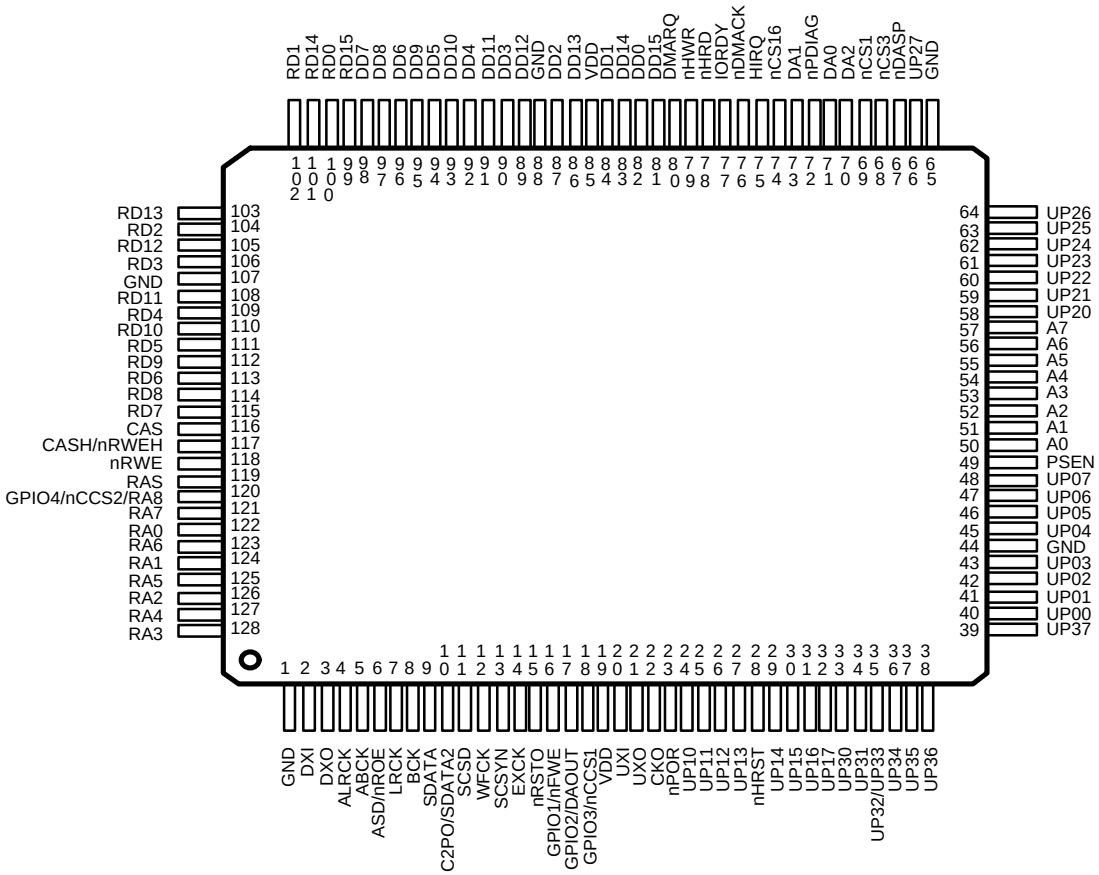
⇒ Up to DC-40MHz operation for built-in µP8032
⇒ 512 bytes of on-chip scratchpad RAM (including 256 bytes re-addressable AUX_RAM)
⇒ AUX_RAM can also be dynamically programmed as an AUX_ROM ,which can be used as an internal rom to support flash programming by uP
⇒ Internal crystal loop off in power-down mode to save more power
⇒ Support programmable wake-up from Power-Down Mode

Miscellaneous

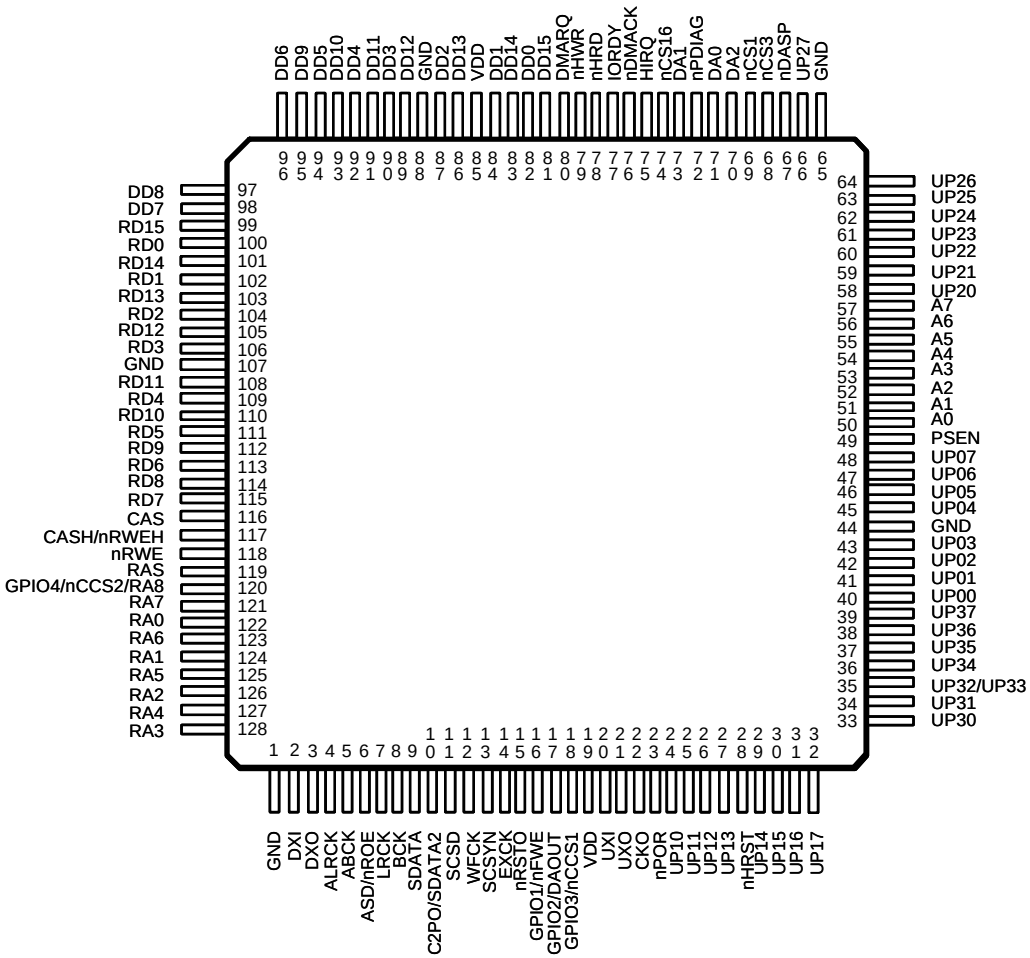
⇒ Glue logic circuit saving (built-in 74373)
⇒ External ROM/Flash chip enable pin to save power in Power-Down Mode
⇒ Support hardware and firmware controlled reset output
⇒ Programmable decoder and servo chip-select base address
⇒ Controllable clock output
⇒ Multi-level power management
⇒ 128-pin PQFP/ LQFP

1.2 Pin Map

W88227F



W88227QD


DD6 DD9 DD5 DD10 DD4 DD11 DD3 DD12 GND DD2 DD13 VDD DD1 DD14 DD0 DD15 DMARQ nHWR nHRD IORDY nDMACK HIRQ nCS16 DA1 nPDIAG DA0 DA2 nCS1 nCS3 nDASP UP27 GND
96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65
DD8 97
DD7 98
RD15 99
RD0 100
RD14 101
RD1 102
RD13 103
RD2 104
RD12 105
RD3 106
GND 107
RD11 108
RD4 109
RD10 110
RD5 111
RD9 112
RD6 113
RD8 114
RD7 115
CAS 116
CASH/nRWEH 117
nRWE 118
RAS 119
GPIO4/nCCS2/RA8 120
RA7 121
RA0 122
RA6 123
RA1 124
RA5 125
RA2 126
RA4 127
RA3 128
64 UP26
63 UP25
62 UP24
61 UP23
60 UP22
59 UP21
58 UP20
57 A7
56 A6
55 A5
54 A4
53 A3
52 A2
51 A1
50 A0
49 PSEN
48 UP07
47 UP06
46 UP05
45 UP04
44 GND
43 UP03
42 UP02
41 UP01
40 UP00
39 UP37
38 UP36
37 UP35
36 UP34
35 UP32/UP33
34 UP31
33 UP30
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
GND DXI DXO ALRCK ABCK ASD/nROE LRCK BCK SDATA C2PO/SDATA2 SCSD WFCK SCSYN EXCK nRSTO GPIO1/nFWE GPIO2/DAOUT GPIO3/nCCS1 VDD UXI UXO CKO nPOR UP10 UP11 UP12 UP13 nHRST UP14 UP15 UP16 UP17

1.3 Pin Arrangement

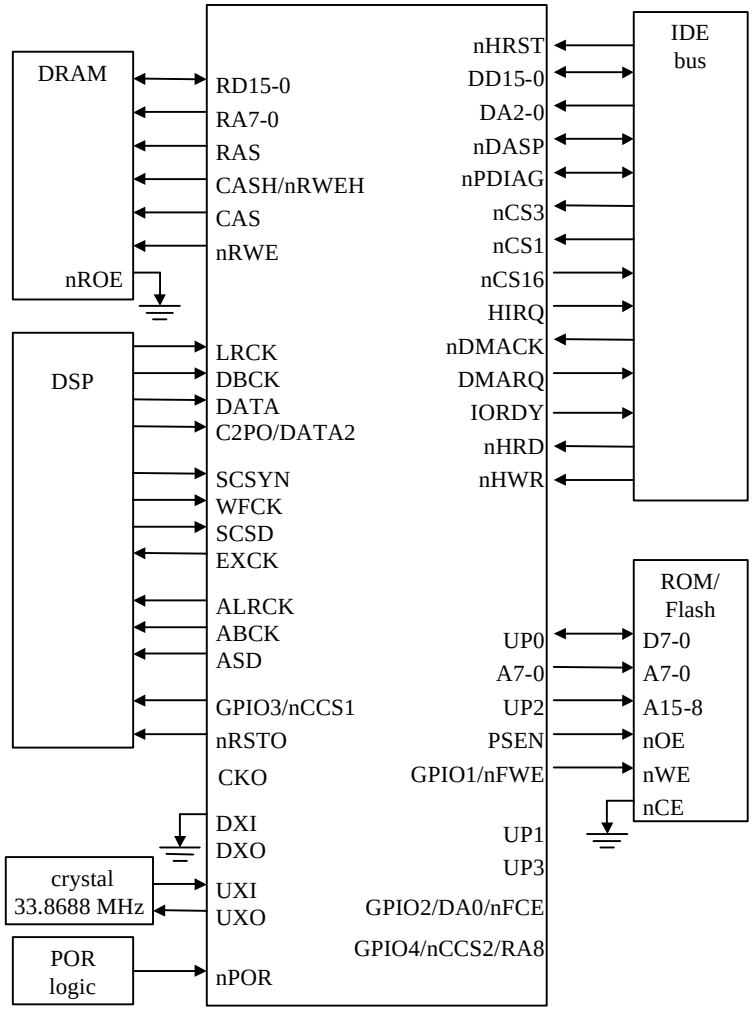
Number	Symbol	Type	Description	Remark
1	GND	P	Ground	
2	DXI	I	Decoder crystal in	Connect to GND if not used
3	DXO	O	Decoder crystal out	
4	ALRCK	I/OZ	Audio playback left/right clock	6mA, PU
5	ABCK	OZ	Audio playback bit clock	6mA, PU
6	ASD nROE	OZ O	Audio playback serial data DRAM read enable, active low	6mA, PU
7	LRCK	I	DSP left/right clock	CMOS level input
8	BCK	I	DSP bit clock	CMOS level input
9	SDATA	I	DSP serial data	CMOS level input
10	C2PO SDATA2	I I	DSP C2 flag DSP serial data 2	CMOS level input
11	SCSD	I	Subcode serial data	
12	WFCK	I	Subcode write frame clock	
13	SCSYN	I	Subcode sync	
14	EXCK	I/O	Subcode external clock	6mA, PU
15	nRSTO	O	Reset output, active low	6mA
16	GPIO1 nFWE	I/O O	General purpose IO Flash Write Enable, active low	6mA, PU
17	GPIO2 DAOUT nFCE	I/O O O	General purpose IO Digital audio output ROM/Flash Chip Enable, active low	6mA, PU
18	GPIO3 nCCS1	I/O O	General purpose IO Configurable chip select, active low	6mA, PU
19	VDD	P	Power	
20	UXI	I	uP crystal in	
21	UXO	O	uP crystal out	
22	CKO	O	clock output	6mA
23	nPOR	I	power on reset, acitve low	PU
24	UP10	I/O	uP port 1	4mA, PU
25	UP11	I/O	uP port 1	4mA, PU
26	UP12	I/O	uP port 1	4mA, PU
27	UP13	I/O	uP port 1	4mA, PU
28	nHRST	I	host reset input, active low	PU
29	UP14	I/O	uP port 1	4mA, PU
30	UP15	I/O	uP port 1	4mA, PU
31	UP16	I/O	uP port 1	4mA, PU
32	UP17	I/O	uP port 1	4mA, PU
33	UP30	I/O	uP port 3 (RXD)	4mA, PU

34	UP31	I/O	uP port 3 (TXD)	4mA, PU
35	UP32 UP33	I/O I/O	uP port 2 (INT0) uP port 3 (INT1)	4mA, PU
36	UP34	I/O	uP Port 3 (T0)	4mA, PU
37	UP35	I/O	uP port 3 (T1)	4mA, PU
38	UP36	I/O	uP port 3 (nWR)	4mA, PU
39	UP37	I/O	uP port 3 (nRD)	4mA, PU
40	UP00	I/O	uP port 0	8mA
41	UP01	I/O	uP port 0	8mA
42	UP02	I/O	uP port 0	8mA
43	UP03	I/O	uP port 0	8mA
44	GND	P	Ground	
45	UP04	I/O	uP port 0	8mA
46	UP05	I/O	uP port 0	8mA
47	UP06	I/O	uP port 0	8mA
48	UP07	I/O	uP port 0	8mA
49	PSEN	I/O	program store enable, acitve low	8mA, PU
50	A0	O	external ROM address	4mA
51	A1	O	external ROM address	4mA
52	A2	O	external ROM address	4mA
53	A3	O	external ROM address	4mA
54	A4	O	external ROM address	4mA
55	A5	O	external ROM address	4mA
56	A6	I/O	external ROM address	4mA, PU
57	A7	I/O	external ROM address	4mA, PU
58	UP20	I/O	uP port 2	4mA, PU
59	UP21	I/O	uP port 2	4mA, PU
60	UP22	I/O	uP port 2	4mA, PU
61	UP23	I/O	uP port 2	4mA, PU
62	UP24	I/O	uP port 2	4mA, PU
63	UP25	I/O	uP port 2	4mA, PU
64	UP26	I/O	uP port 2	4mA, PU
65	GND	P	Ground	
66	UP27	I/O	uP port 2	4mA, PU
67	nDASP	I/OD	drive active, active low	12mA, PU
68	nCS3	I	host chip select 1, active low	PU
69	nCS1	I	host chip select 0, active low	PU
70	DA2	I	host address 2	PU
71	DA0	I	host address 0	PU
72	nPDIAG	I/OD	passed diagnostics, active low	12mA, PU
73	DA1	I	host address 1	PU
74	nCS16	OD	16-bit IO select, active low	24mA

75	HIRQ	OZ	host interrupt	12mA
76	nDMACK	I	DMA acknowledge, active low	PU
77	IORDY	OZ	IO channel ready	24mA
78	nHRD	I	host read strobe, active low	PU
79	nHWR	I	host write strobe, active low	PU
80	DMARQ	OZ	dam request	12mA
81	DD15	I/O	host data	12mA, PU
82	DD0	I/O	host data	12mA, PU
83	DD14	I/O	host data	12mA, PU
84	DD1	I/O	host data	12mA, PU
85	VDD	P	Power	
86	DD13	I/O	host data	12mA, PU
87	DD2	I/O	host data	12mA, PU
88	GND	P	Ground	
89	DD12	I/O	host data	12mA, PU
90	DD3	I/O	host data	12mA, PU
91	DD11	I/O	host data	12mA, PU
92	DD4	I/O	host data	12mA, PU
93	DD10	I/O	host data	12mA, PU
94	DD5	I/O	host data	12mA, PU
95	DD9	I/O	host data	12mA, PU
96	DD6	I/O	host data	12mA, PU
97	DD8	I/O	host data	12mA, PU
98	DD7	I/O	host data	12mA, PU
99	RD15	I/O	DRAM data	6mA, PU
100	RD0	I/O	DRAM data	6mA, PU
101	RD14	I/O	DRAM data	6mA, PU
102	RD1	I/O	DRAM data	6mA, PU
103	RD13	I/O	DRAM data	6mA, PU
104	RD2	I/O	DRAM data	6mA, PU
105	RD12	I/O	DRAM data	6mA, PU
106	RD3	I/O	DRAM data	6mA, PU
107	GND	P	Ground	
108	RD11	I/O	DRAM data	6mA, PU
109	RD4	I/O	DRAM data	6mA, PU
110	RD10	I/O	DRAM data	6mA, PU
111	RD5	I/O	DRAM data	6mA, PU
112	RD9	I/O	DRAM data	6mA, PU
113	RD6	I/O	DRAM data	6mA, PU
114	RD8	I/O	DRAM data	6mA, PU
115	RD7	I/O	DRAM data	6mA, PU
116	CAS	OZ	DRAM column address strobe	8mA

117	CASH nRWEH	OZ OZ	DRAM column address strobe DRAM write enable, active low	8mA
118	nRWE	OZ	DRAM write enable, active low	8mA
119	RAS	OZ	DRAM row address strobe	
120	GPIO4 nCCS2 RA8	I/O O O	General purpose IO Configurable chip select, active low DRAM address	6mA, PU 6mA 6mA
121	RA7	I/O	DRAM address	6mA, PU
122	RA0	I/O	DRAM address	6mA, PU
123	RA6	I/O	DRAM address	6mA, PU
124	RA1	I/O	DRAM address	6mA, PU
125	RA5	I/O	DRAM address	6mA, PU
126	RA2	I/O	DRAM address	6mA, PU
127	RA4	I/O	DRAM address	6mA, PU
128	RA3	I/O	DRAM address	6mA, PU

1.4 Basic Configuration



2. Functional Description

2.1 Global Function

2.1.1 Decoder Register Access

The Decoder Index Register is latched from uP Port-0 by the built-in 74373 at the falling edge of internal *ALE* signal. The high byte address of decoder register is defined by *CCSA0 (40h)* with default value 40h.

<example>: decoder register read (read VER)

```
MOV   DPTR,#0401Ah
MOVX  A,@DPTR
```

<example>: decoder register write (set CCSA1 as 0xC0h)

```
MOV   A,#0C0h
MOV   DPTR,#04041h
MOVX  @DPTR,A
```

2.1.2 Reset Source

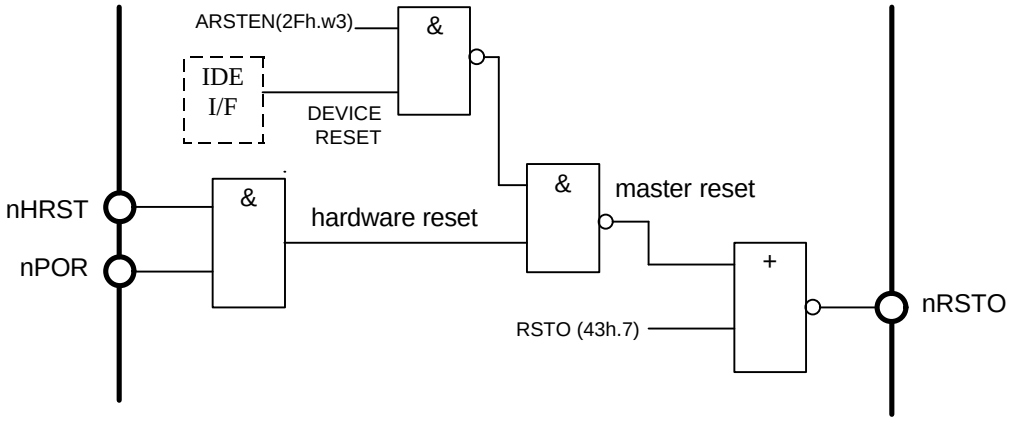
The chip will be reset when master reset, including:

(1) power on reset,

(2) host reset or

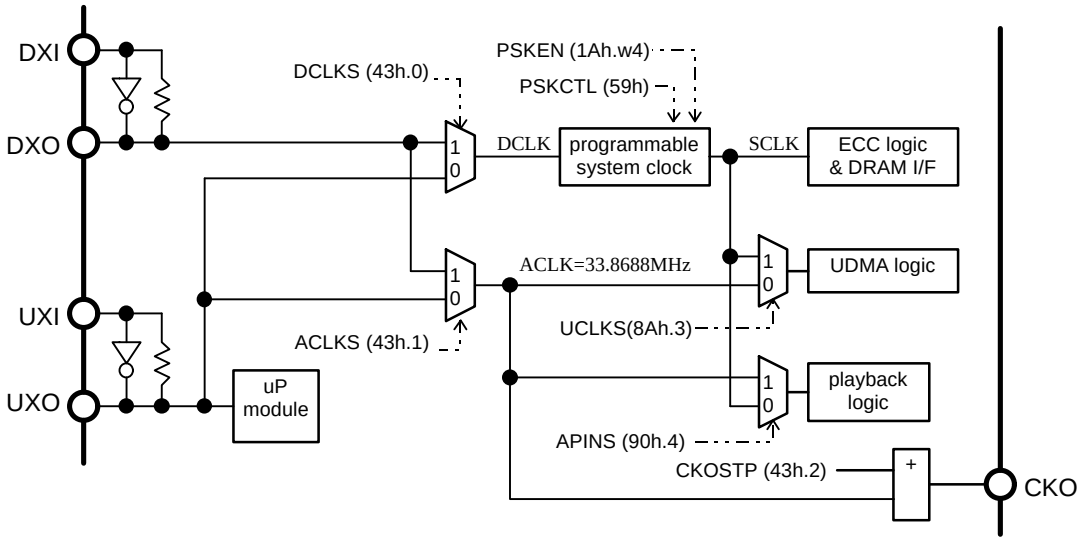
(3) reception of DEVICE RESET command (opcode 08h) if *ARSTEN (2Fh.w3)* is high.

The output of pin nRSTO can be controlled either by master reset or firmware. The state of *pin nRSTO* is the inverse value of control bit *RSTO (43h.7)*.



2.1.3 Clock Source and Power Management

If the frequency on UXI is 33.8688 MHz, then the crystal on DXI can be saved. If the frequency on UXI is not 33.8688 MHz, then the input frequency on DXI must be 33.8688 MHz to support audio playback. A clock output pin CKO can be used as clock source. If *CKOSTP (43h.2)* is set high, the output of pin CKO holds a "high" status so that the external device is in idle mode. Note that DXI should be connected to ground if not used.



Decoder Idle Mode

Setting *CKSTP (19h.w7)* stop the clock of decoder. The decoder exits idle mode on reset or host command.

UP8032 Idle Mode

Setting the *IDL (PCON.0)* high stop the clock of uP8032. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-Down Mode

When *PD (PCON.1)* is set high, the chip enters the power-down mode. In this mode, the crystal feedback loop between UXI and UXO can be closed by setting *PD (PCON.1)* high, and that between DXI and DXO can be closed by setting *XOFF (8Ah.7)* high. In two-crystal case, *XOFF* should be set before *PD*. These two loops resume on the following conditions.

EA	EHWK	EIWK	HIIEN	ARSTIEN	wake-up event
x	x	x	x	x	power on reset or host reset
1	1	x	1	x	software reset by setting SRST high
1	1	x	x	1	DEVICE RESET command
1	x	1	x	x	interrupt on INT0 or INT1

Before entering power-down mode, internal pull-up resistors can be closed by setting *PUCTL (98h)*.

2.1.4 Multi-function Pins

The state of general-purpose I/O pins can be controlled through register *GIOCTL (5Fh)*.

2.1.4.1 GPIO1/nFWE Configuration

If the *IDE Programming Ready Signature (E8)* is high by executing the IDE programming sequence, this pin is used as nFWE. Otherwise, this pin is used as GPIO1.

2.1.4.2 GPIO2/DAOUT/nFCE Configuration

G2CF (5Dh.3)	DAOEN (87h.7)	pin function	Remark
0b	0b	nFCE	(default)
1b	0b	GPIO2	
x	1b	DAOUT	

This pin is configured as nFCE and output "low" after master reset. It holds "high" when uP enter power-down mode by setting *PD (PCON.1)* high and returns to low active status when:

1. Hardware reset,
2. Software reset if *HIIEN (2Eh.w7)* is set high,
3. or DEVICE RESET command if *ARSTIEN (2Fh.w1)* is set high.

This function can be utilized to save power of external ROM in Sleep mode.

If a pull-down resistor is connected to pin RA4, the pin is configured as GPIO2 after master reset. If *DAOEN (87h.7)* is set high, this pin is used as DAOUT, digital audio output.

2.1.4.3 GPIO3/nCCS1 Configuration

The value of CCSA1 (41h) is 00h after master reset.

G3CF (5Dh.2-0)	Function	nCCS1 active (low) condition	Remark
0xxb	GPIO3	n/a	Default
100b	nCCS1	(P2 = CCSA1)	
101b	nCCS1	(P2 = CCSA1) & (P36 = "L")	
110b	nCCS1	(P2 = CCSA1) & (P37 = "L")	
111b	nCCS1	(P2 = CCSA1) & (P36 = "L" or P37 = "L")	

2.1.4.4 GPIO4/nCCS2/RA8 Configuration

The value of CCSA2 (42h) is 00h after master reset.

G4CF (5Dh.7-4)	Function	nCCS2 active (low) condition	Remark
0xxxb	RA8	output is tri-state after master reset and is enabled when RTC (2Ah.2-0) ≠ 000b	Default
10xxb	GPIO4	n/a	
1100b	nCCS2	(P2 = CCSA2)	
1101b	nCCS2	(P2 = CCSA2) & (P36 = "L")	
1110b	nCCS2	(P2 = CCSA2) & (P37 = "L")	
1111b	nCCS2	(P2 = CCSA2) & (P36 = "L" or P37 = "L")	

2.1.4.5 UP32/UP33 Configuration

UP323S (43h.4)	Pin UP32/UP33	Internal Decoder Interrupt	Remark
0b	INT0	INT1	Default
1b	INT1	INT0	

2.1.4.6 ASD/nROE Configuration

This pin is used as nROE after master reset. It is configured as ASD (audio playback serial data) when setting *APOUT (90h.1-0)* as 01b.

2.1.4.7 CASH/nWREH Configuration

This pin is tri-state after master reset. It is configured as output when *RTC (2Ah,2-0)* is 10xb. It is used as CASH when *TWES (2Ah,3)* is low and as nRWEH when *TWES (2AH,3)* is high.

2.1.5 IDE Programming Mode

This chip enters *IDE Programming Mode* when the last initiation key is written to Control Port. The status can be verified by read *IDE Programming Ready Signature (E8h)* from Feature Port.

2.1.5.1 Pin Mapping

Flash Pin Name	W88227 Pin Name	Function
A15-8	UP27-UP20	Address High
A7-0	A7-0	Address Low
DQ7-0	UP07-UP00	Data
CEN	GPIO2/DAOUT/nFCE	Chip Enable
OEN	PSEN	Output Enable
WEN	GPIO1/nFWE	Write Enable

2.1.5.2 IDE Programming Sequence

The following sequence is only an example. Please properly adjust it to fit the specification of different Flash.

1. Select the drive
2. Write **Initiation Key** to 1F3h/173h
3. Read 1F3h/173h to verify **IDE Programming Ready Signature (E8h)**
4. Write address to 1F4h/174h and 1F5h/175h
5. Write data to 1F1h/171h
6. Activates NFCE by writing 04h to 1F2h/172h
7. Activates NFWE by writing 05h to 1F2h/172h
8. Releases NFWE by writing 04h to 1F2h/172h
9. Go back to step 4 until all data are written
10. Write address to 1F4h/174h and 1F5h/175h
11. Activates NFOE by writing 06h to 1F2h/172h
12. Read from 1F1h/171h to verify data
13. Releases NFOE by writing 04h to 1F2h/172h
14. Go back to step 10 until all data are verified
15. DEVICE RESET (re-start uP program counter from 0) or Re-boot

2.1.5.3 Initiation Key

The exact sequence for the initiation key in hexadecimal notation is:

```
4C, 26, 93, 49, A4, 52, A9, D4,
6A, B5, DA, ED, F6, FB, 7D, BE,
DF, 6F, 37, 1B, 0D, 86, C3, 61,
B0, 58, 2C, 16, 8B, 45, A2, D1
```

2.1.5.4 IDE Programming Registers

Port Name	Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data	1F1h/171h	r/w	Flash data							
Control	1F2h/172h	w	x	x	x	x	x	fce	foe	fwe
Feature	1F3h/173h	r/w	Programming signature							
Address Low	1F4h/174h	w	Flash low address							
Address High	1F5h/175h	w	Flash high address							

2.1.6 Power-On Setting

Pin RA7-0 are input with weak pull-up during master reset or when *RTC (2Ah.2-0)* is 000b. RA7-5 are used as power-on setting and RA4-0 can be used as general input when *RTC (2Ah.2-0)* is 000b. The status of RA7-0 can be read from *RASTA (2Dh,r)*.

pin RA7 4.7 KΩ pull-down	Operation Mode	remark
no	Normal mode	default
yes	EUP mode	for ICE debugging

pin RA6 4.7 KΩ pull-down	decoder chip select base address	remark
no	40xxh	default
yes	C0xxh	

pin RA5 4.7 KΩ pull-down	Operation Mode	remark
no	normal mode	default
yes	uP test mode	for factory test only

2.1.7 External uP (EUP) Mode

If a 4.7K pull-down is connected to pin RA7 during power-on, this chip enters the External uP (EUP) mode. In EUP mode, the internal uP do not work and some pins are redefined by the following table to work with an external uP. This testing mode is specially designed for firmware debug using ICE. Note that one TTL is needed to support external uP reset signal in EUP mode.

Normal	I/O	EUP mode	I/O	Remark
P0	I/O	UD	I/O	
P1	I/O	n/a	Z	
P2	I/O	n/a	I	Be used to generate internal UCSb
A7-0	O	A7-0	O	
UP30	I/O	n/a	Z	
UP31	I/O	n/a	Z	
UP33/UP32	I/O	UINTb	O	One 0 ohm option resistor may be needed
UP34	I/O	n/a	Z	
UP35	I/O	n/a	Z	
UP36	I/O	UWRB	I	
UP37	I/O	URDB	I	
PSEN	O	ALEIN	I	One 0 ohm option resistor may be needed

2.1.8 uP Test (UPT) Mode

If a 4.7K pull-down is connected to pin RA5 during power-on, this chip enters the uP test (UPT) mode. In UPT mode, some pins are redefined by the following. This mode is for factory test only.

Normal	I/O	UPT mode	I/O	Remark
P32/P33	I/O	P32	I/O	
A7	O	P33	I/O	
A6	O	ALE	O	

2.2 Decoder Function

2.2.1 DRAM Interface

2.2.1.1 Memory Layout

The whole DRAM can be divided into Sector *Data Area* and *Working Area.* Sectors from DSP are buffered into Sector Data Area and then are retrieved for ECC/EDC operation. Some information is stored in working area for transfer to host on request, for example, TOC.

Sector data buffering is a block-based ring operation. If the decoded-block-number in *DDBH/L (29h/28h)* is *N - 1*, the sector is buffered into block with number *N*. The decoded-block-number is automatically incremented by one at each sync. When the decoded-block-number equals the value in *WBRCH/L (57h/56h)*, the sector is buffered into the block with number specified by *WBRBH/L (55h/54h)*.

The data transfer is also a block-based ring operation if multi-block-transfer is used. The transfer ring is controlled by *DTRCH/L (53h/52h)* and *DTRBH/L (51h/50h)*. The buffer ring and transfer ring are usually defined in the same range.

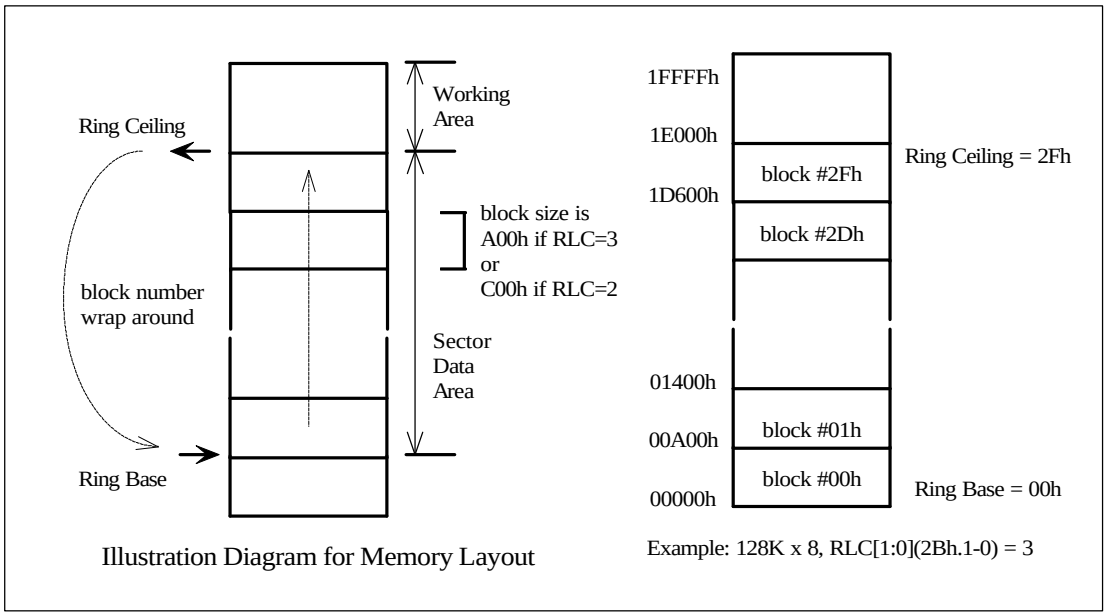


Illustration Diagram for Memory Layout

Example: 128K x 8, RLC[1:0](2Bh.1-0) = 3

2.2.1.2 Block Configuration

The configuration of each memory block depends on the data format. The following tables show the recommended configuration of block whose size is A00h and C00h, respectfully.

■ If BIA (09h/08h) = 000Ch and RLC (2Bh.1-0) = 3, block size is A00h.

Item	Mode 1	Mode 2	Mode2 Form1	Mode2 Form2	CD-DA
Sync	000h (12)	000h (12)	000h (12)	000h (12)	N/A
Header	00Ch (4)	00Ch (4)	00Ch (4)	00Ch (4)	N/A
Subheader	N/A	N/A	010h (8)	010h (8)	N/A
User Data	010h (2048)	010h (2336)	018h (2048)	018h (2324)	000h (2352)
ECC & EDC	810h (288)	N/A	818h (280)	92Ch (4)	N/A
Subcode	980h (96)	980h (96)	980h (96)	980h (96)	980h (96)
Q-channel	9E0h (12)	9E0h (12)	9E0h (12)	9E0h (12)	9E0h (12)

Note: Table format: Starting offset address (No. of bytes)

■ If BIA (09h/08h) = 000Ch and RLC (2Bh.1-0) = 2, block size is C00h.

Item	Mode 1	Mode 2	Mode2 Form1	Mode2 Form2	CD-DA
Sync	000h (12)	000h (12)	000h (12)	000h (12)	N/A
Header	00Ch (4)	00Ch (4)	00Ch (4)	00Ch (4)	N/A
Subheader	N/A	N/A	010h (8)	010h (8)	N/A
User Data	010h (2048)	010h (2336)	018h (2048)	018h (2324)	000h (2352)
ECC & EDC	810h (288)	N/A	818h (280)	92Ch (4)	N/A
C2 flag	A00h (294)	A00h (294)	A00h (294)	A00h (294)	A00h (294)
Subcode	B80h (96)	B80h (96)	B80h (96)	B80h (96)	B80h (96)
Q-channel	BE0h (12)	BE0h (12)	BE0h (12)	BE0h (12)	BE0h (12)

The rule for configuration is that the first byte of the sector is stored at:

BIAH/L(09h/08h,w) - 0Ch

And the following byte is stored into the incremented offset address. If the offset address reaches the block limit, the next offset address is wrap around to zero. For example, the byte following that at offset 9FFh is at 000h if block limit is A00h. By this mechanism and following example settings, the first byte of user data is always located at 000h.

The Subcode (980h/B80h) and Q-channel (9E0h/BE0h) data are stored at fixed address if its associated function is enabled. But the 2352 bytes sector data (including sync, header, user data, ECC, EDC for Mode 1 sector) can be re-arranged to any other area in the block.

2.2.1.3 Linear Transfer Address Counter

When *LATXF (03h.w7)* is high, the address defined by *RACU/H/L (2Dh/1Dh/1Ch,w)* is loaded to a internal Linear Transfer Address Counter at the begin of data transfer. This separate counter leaves *RACU/H/L (2Dh/1Dh/1Ch,w)* free for uP to DRAM access after the transfer is triggered. The uP can access DRAM data defined by *RACU/H/L (2Dh/1Dh/1Ch,w)* regardless the setting of *LATXF (03h.w7)*.

2.2.1.4 Linear Address v.s. Block-Offset Address

The microprocessor can write/read external RAM through register *RAWR/RAMRD (1Eh)* based on linear address defined by *RACU/H/L (2Dh/1Dh/1Ch,w)*. But the operation of data transfer from DRAM to host can base on block-offset address or linear address. The following equation defines the relation between these two types of address.

$$\text{linear address} = (\text{block number} \times \text{block size}) + \text{address offset}$$

<Example 1> Data Transfer in Working Area

Conditions: 64 bytes of TOC data are stored starting from linear address 3EA00h at disc initialization and TOC is requested by host (block size is A00h).

A) Sequence at disc initialization:

a) set RACL (1Ch) as 00h
b) set RACH (1Dh) as EAh
c) set RACU (2Dh) as 03h
d) wait UTBY (1Fh.7) low
e) write data to register RAMWR (1Eh)
f) goto step e) until all 64 bytes are written to DRAM

B1) Setting for ***block-offset address*** transfer:

- set TBH/L (25h/24h) as 0064h
- set TACH/L (05h/04h) as 0200h
- set TWCH/L (03h/02h) as 001Fh

B2) Setting for ***linear address*** transfer:

- set RACL (1Ch) as 00h
- set RACH (1Dh) as EAh
- set RACU (2Dh) as 03h
- set TWCH/L (03h/02h) as 801Fh

<Example 2> Data Transfer in User Area

Case 1: The 2048 bytes of user data are requested by host.

- set TBH/L (25h/24h) as 001Fh
- set TWCH/L (03h/02h) as 03FFh
- set TACH/L (05h/04h) as 0010h

Case 2: The 288 bytes of EDC&ECC data are request by host.

- set TBH/L (25h/24h) as 001Fh
- set TWCH/L (03h/02h) as 008Fh
- set TACH/L (05h/04h) as 0810h

If the requested data is not stored continuously in DRAM, e.g., header and EDC&ECC data, more than one transfer has to be triggered.

2.2.2 Microcontroller Interface

2.2.2.1 Programmable System Clock

The internal system frequency is controlled by *CCTL1 (1Ah,w)* and *PSKCTL (59h,w)*. Register *PSKCTL (59h,w)* should be set before the programmable system clock is enabled by setting *PSKEN (1Ah.w4)* high. If both *PSKEN (1Ah.w4)* and *PSKSEL (59h.w7)* are high, *PSK5-0 (59h.5-0)* are used to controlled the internal system frequency. Register *PSKCTL (59h,w)* should be set before the programmable system clock is enabled by setting *PSKEN (1Ah.w4)* high. The equation is:

$$\text{frequency of system clock} = \text{frequency of ACLK} \times (\text{PSK[5:0]} + 2) \div 16$$

The variation of the resultant system frequency is normally less than 5%.

<example> If the frequency of ACLK is 33.8688 MHz, *PSKEN (1Ah.w4)* and *PSKSEL (59h.w7)* are high:

PSK5-0	System Frequency	Remark
0Fh	36 MHz	
11h	40.2 MHz	
13h	44.4 MHz	
15h	48.7 MHz	
17h	53 MHz	
19h	57.2 MHz	
1Bh	61.4 MHz	

2.2.3 Host Interface

The host interface is a standard ATAPI interface with enhanced Ultra DMA support. The Ultra DMA protocol could double the current burst transfer rate of 16.6MB/sec to 66MB/sec without hardware changes such as termination devices or different cabling.

2.2.3.1 Ultra DMA Mode Setting

This decoder is capable of supporting Ultra DMA Mode 4. Device firmware could claim that *Ultra DMA mode 4 and below are supported* in IDENTIFY DEVICE information.

The value of *UDT1-0 (8Ah,5-4)* defines the Ultra DMA Timing Factor, ***udtf***, which control the timing of Ultra DMA transfer.

Tcyc = (2 + ***udtf***) × Tudma

where Tudma is clock period depends on setting of *UDTA (8Ah.6)* and *UCLKS (8Ah.3)*
and Tcyc is Ultra DMA cycle time (from DSTROBE edge to DSTROBE edge)

Device firmware should set ***udtf*** according to the clock source and the assigned Ultra DMA transfer mode after host issues SET FEATURE command. If there are frequent CRC errors in data-in bursts, device firmware may switch system to slower Ultra DMA mode by increasing ***udtf*** to improve data integrity.

Example: If *UCLKS (8Ah.3)* is high and frequency of ACLK is 33.8688MHz, the ***udtf*** should be the following value to abide by the determined Ultra DMA mode.

Ultra DMA	T2cyc Min. Spec.	T2cyc	***udta***	***udtf***
Mode 0	230 ns	236 ns	0	2
Mode 1	154 ns	177 ns	0	1
Mode 2	115 ns	118 ns	0	0
Mode 3	86 ns	88.6 ns	1	1
Mode 4	57 ns	60 ns	1	0

2.2.3.2 Ultra DMA Error Handling

Flag *UCRCOKb (30h.r3)* is used to determine if a CRC error event has occurred during latest Ultra DMA burst. If *AUCRCEN (18h.2)* and *ASCEN (18h.5)* are both set high, the automatic status complete logic would not be triggered if *UCRCOKb (30h.r3)* is high. Therefore, firmware should check *UCRCOKb (30h.r3)* flag after each Ultra DMA burst. If a CRC error has occurred, firmware should set *CHK (37h.0)* to one and manually trigger status complete.

2.2.3.3 Ultra DMA Data-out

The programming of Ultra DMA transfer is similar to that of Multi-word DMA transfer. One thing should be noted is that *device should prepare to receive one additional word at the end of a data out burst*. Since 12-byte Packet FIFOs are used to receive data in Ultra DMA data-out transfer, the value of registers *TWCH/L (03h/02h)* should be set 4 instead of 5. Then firmware should repeatedly read register *PFAR (00h,r)* after Transfer End Interrupt asserts until flag *PFNEb (01h.r7)* becomes one.

<example> data-out transfer sequence:

1. TENDEN (01h.w6) ← 1
2. ASCTRL (18h,w) ← 58h
3. HICTL0 (1Fh.w) ← 0Bh // UDMA data-out
4. TWC (03h/02h,w) ← min(0004h, byte_cnt/2-1)
5. ADTT (17h.w2) ← 1 // automatic data transfer trigger
6. wait TENDb (01h.r6) = 0 and TDIR (30h.r5) = 1 and FPKT (30h.r1) = 1
7. TACK (07h,w) ← FFh
8. read PFAR (00h,r); byte_cnt =byte_cnt - 1
9. if PFNEb (01h.r7) is low, repeat step (8)
10. if (byte_cnt ≠ 0) goto step (4)
11. SCT (17h.0) ← 1 // status complete trigger

2.2.3.4 BSY flag control

BSY is bit-7 of ATAPI Status Register.

BSY set	BSY clear
Chip reset	Set *CLRBSY (20h.w4)* if *APKT (30h.r0)* is low
Host reset	Set *DRQT (17h.w1)* if *PIO (1Fh.2*) is high
Set bit *SRST* in ATAPT Device Control Register	Host issue ATAPI Command (opcode A0h) if *APKTEN (18h.7)* is high
Set *SETBSY (20h.w3)* if *APKT (30h.r0)* is low	Automatic Status Completion sequence, enabled by *SCT (17h.w0)* or *ASCEN (18h.5)*
Host issues Execute Diagnostics Command (opcode 90h)	*DFRDYb (01h.r1)* becomes low after *ADTT (17h.w2)* is set, if *PIO (1Fh.2*) is high
Host issue ATA Command when drive is selected	
Transfer end if *ADCEN (18h.6)* is enabled	
Set *ADTT (17h.w2)*	
Set *DSCT (17h.w5)* if *ABYEN (18h.1)* is enabled - lasting 3 system clocks	

2.2.3.5 Pin HIRQ control

Pin HIRQ is set or clear by the following conditions if the drive is selected and *nIEN* is enabled in the ATAPI Device Control Register.

HIRQ is activated by the following events:

- Automatic Packet Transfer sequence, enabled by *APKTEN (18h.7)*
- Automatic Status Completion sequence, enabled by *SCT (17h.w0)* or *ASCEN (18h.5)*
- Write *MISC0 (2Eh)* with bit-3 high

HIRQ is de-activated by the following events:

- Chip reset or host reset or firmware rest
- Set bit SRST in the ATAPI Device Control Register high
- Host issue ATA command while the drive is selected
- Host read ATAPI Status Register while the drive is selected
- Write *MISC0 (2Eh)* with bit-3 low

2.2.4 Decoder Logic

2.2.4.1 Sync Detection/Insertion

The sync field of CD-ROM data is recorded as following: 1 (00h) bytes, 10 (FFh) bytes and 1 (00h) byte. This sync field is detected for sector synchronization if *SDEN (0Bh.w6)* is enabled. To prevent loss of synchronization caused by broken sync, an internal counter can provide inserted sync signal if *SIEN (0Bh.7)* is enabled. There are no sync bytes in CD-DA format, so *SDEN (0Bh.w6)* should not be set.

2.2.4.2 Descramble

Bytes 12 to 2351 of each CD-ROM sector is scrambled in decoding. Setting *DSCREN (0Bh.5)* high enables the descramble logic. Descramble logic should be disabled while reading of CD-DA data.

2.2.4.3 Disk-Monitor Mode

The decoder logic is in disk-monitor mode if *CTRL0 (0Ah,w)* is set as 80h. In disc-monitor mode, no ECC correction and EDC checking is carried. The sector ready interrupt flag *SRIb (01h.r5)* is immediately generated when the header bytes are available in *HEAD0-3 (04h-07h,r)*. The header bytes in disc-monitor mode are less trustworthy than that in buffer-correction mode.

2.2.4.4 Parallel ECC Correction

The error correction of the CD-ROM sector is carried by a Reed-Solomon Product-Like Code (RSPC). The RSPC is a product code over GF(2^8) field which is generated by the primitive polynomial

$$P(x) = x^8 + x^4 + x^3 + x^2 + 1$$

The primitive element α of GF(2^8) is

$$\alpha = (00000010)$$

where the right-most bit is the least significant bit.

The data is divided into high byte plane and low byte plane before decoding. The RSPC decoding, operating on bytes, is then applied twice, once to the high byte plane, once to the low byte plane.

To improve the efficiency of RSPC decoding, a parallel ECC correction logic is implemented on chip. After sync detection and descramble, the parallel ECC correction is carried on high byte plane and low byte plane simultaneously. This correction scheme is about 33% faster than conventional decoder.

The Q-code correction and P-code correction are enabled by *QCEN (0Ah.w1)* and *PCEN (0Ah.w0)* respectively. If both correction operations are enabled, Q-code correction is executed first. The corrected data are written back to external RAM if *CWEN (0Bh.w4)* is high.

2.2.4.5 EDC Checking

The EDC checking logic carry 32-bit CRC checking on error corrected data according to its mode. The checking result can be monitored through flag *CRCOK (0Ch.r7)*. If the result is error, the errors in sector may exceed the capacity of correction logic and some data might be miscorrected.

2.2.4.6 Real Time EDC Checking

If real time EDC checking logic is enabled by setting *RTEDC (0Ah.w6)* high, the remainder of serial data is calculated while the sector is being buffered into DRAM. The sector ready interrupt flag *SRIb (01h.r5)* is immediately activated at next sync if the resultant remainder is zero, i.e., no EDC error. If there is error, the specified error correction is then applied to the buffered data. This function should not be enabled in disk-monitor mode.

2.2.4.7 Disc Format Selection

Before enable decoder logic through register *CTRL0 (0Ah,w)*, appropriate value should be set to register *CTRL1 (0Bh.w)* according to different disc format. If *ACEN (0Ah.w4)* and *M2RQ (0Bh.w3)* are both high, the type of error correction is automatically determined by FORM bit in the subheader byte rather than setting of *F2RQ (0Bh.w2)*. The value of *ACEN (0Ah.w4)* does not affect the yellow-book mode-1 correction.

disc format	SIEN (0Bh.7)	SDEN (0Bh.6)	DESCREN (0Bh.5)	CWEN (0Bh.4)	M2RQ (0Bh.3)	F2RQ (0Bh.2)
CD-DA	1	0	0	0	0	0
yellow book Mode 1	1	1	1	1	0	0
yellow book Mode 2	1	1	1	0	0	0
CD-ROM XA M2F1	1	1	1	1	1	0
CD-ROM XA M2F2	1	1	1	x	1	1

2.2.4.8 DSP Main Data Format

If *D2EN (1Bh.w3)* is set high, pin C2PO/SDATA2 is used as second serial data input pin. The two-bit format can dramatically reduce the frequency on DSP main data interface and improve EMI.

DSPSL	DSP Data Format
07h	Toshiba
0Bh	Winbond two-bit
24h	Sanyo
A3h	Sony 48-bit slot
C3h	Philip

2.2.4.9 CD-DA data & Q-channel Extraction

There are no sync bytes in CD-DA format, so absolute MSF bytes of *Mode 1Data-Q* (ADR = 0001) should be utilized as synchronization when reading CD-DA data. Q-channel extraction can be enabled by setting both *QEN (80h.w5)* and *SCEN (2Ch.w6)* high. Once decoder and Q-channel extraction are both enabled, the extracted Q-channel bytes are written into the DRAM starting from offset 9E0h of each block regardless of what mode of data is set.

The first byte of Q-channel (CONTROL and ADR) can be retrieved from offset 9E0h. When *QSIGEN (21h.4)* is set high, a signature 0xFFh will be placed in offset 9E0h if CRC checking of Q-code is erroneous.

The absolute MSF information can be retrieved from offset 9E7h, 9E8h and 9E9h of each block.

There is an alternative way to access MSF of Q-channel information. If control bit *QMSF (80h.w4)* is set high, the corresponding MSF bytes in Q-channel information would be automatically loaded into *HEAD0-2 (04h-06h,r)* when each byte is ready from DSP. The register *HEAD3 (07h,r)* hold first byte of *DATA-Q*, (CONTROL and ADR) or 0xFFh if CRC checking of Q-channel is erroneous.

If Q-channel extraction is enabled, device firmware can check flag *QCRCOK (22h.r4)* to see if there is a CRC error in the latest Q-channel information.

<example> SMD1 format setting:

- BIAH/L (09h/08h) = 000Ch
- CTRLW (10h.w) = 30h
- SICTL0 (21h) = 30h
- SICTL1 (2Ch,w) = 55h (SMD1 mode)
- QEN (80h.w5) = 1 and QMSF (80h.w4) = 1
- SDBS (88h.w4) = 1 and SBCK (88h.w3) = 1
- CTRL1 (0Bh.w) = 80h
- CTRL0 (0Ah.w) = 84h
- SCIb (01h.r0)
- SUBSTA (22h.r)

Following the above setting, there is no need to set *SICTL (21h.w), SCBH/L (27h/26h,w)* and *SCTC (5Ah,w)*. In order to transfer the whole sector to host, 2352 bytes, the value in *TWCH/L (03h/02h)* should be 0497h and the value in *TACH/L (05h/04h)* should be 0000h.

2.2.4.10 Target Search

The target search logic is initialized by: (1) setting Search Limit, (2) setting Target and (3) setting *TARGEN (80h.w7)* high. After the decoding is triggered through *CTRL0 (0Ah,w)*, the first sector ready interrupt is generated when: i) the target sector is found, ii) header is larger than target or iii) search limit is reached. If event ii) or iii) occurs, the microprocessor may read out *HEAD0-2 (04h-06,r)* to determine the current distance from target. Setting *LTTIEN (80h.w2)* and *TNFEN (80h.w1)* high can generate the associated interrupt flag on *SRIb (01h.r5)* before the target is found.

2.2.4.11 Automatic Header Comparison

The automatic header comparison logic is enabled by setting *TARGEN (80h.w7)* and *HCEEN (80h.w0)* high. After the first target is found, the value in *TARGET (84h-86h)* increases from *(T - 1)* to *T*. And the decoder is changed from disk-monitor mode to buffer-correction mode. Then *HEAD0-2 (04h-06h,r)* are compare with *TARGET (84h-86h)* and generate flag *HCEI (80h.r0)* at the end of EDC-checking. Unless flag *STAERR (80h.r6)* or *HCEI (80h.r0)* is generated, the value in *TARGET (84h-86h)* is automatically incremented by one and ready to be compared with next sector.

2.2.4.12 Status Collection

The status collection logic is enabled if any bit in the *Status-Mask-Register (8Ch-8Fh,w)* is set high. At the end of EDC-checking, flag *STAERR (80h.r6)* becomes high if any status bit error that is enabled by its associating mask bit occurs. The microprocessor can reduce the system overhead by checking *STAERR (80h.r6)* rather than reading out *STAT (0Ch-0Fh,r)*.

2.2.4.13 Buffer-Independent-Correction

Buffer-Independent-Correction (BIC) is enabled if *BICEN (9Ah.7)* is high. In *BIC* mode, the correction is triggered when the sectors not decoded in buffer is larger than one. In *BIC* mode, the *DDBH/L (29h/28h)* controls the decoding block and increments at the end of EDC-checking, except erroneous sectors. Meanwhile, the buffering block (internal) increments at each sync. Because of the independence of the buffering block and decoding block, the *automatic repeat correction* can be enabled by setting *RCLIM3-0 (9Ch.3-0)* the maximum rounds of repeat correction.

2.2.4.14 Remove Frequent SRIb & Automatic Cache Management

Control bit *RMSRI (5Ch.0)* should be set when entering buffer mode and be disabled in decoder_off routine. When *RMSRI (5Ch.0)* is high, flag *SRIb (01h.r5)* is generated only by *STAERR (80h.r6), LASTBK (80h.r3)* or *HCEI (80h.r0)*.

So after the target is found and buffer-correction mode is enabled, the first interrupt is generated by *LASTBK (80h.r3)* if there is no decoding error. Setting *RMSRI (5Ch.0)* high can reduce the overhead of microcontroller while the automatic cache management is used.

Since the *SRIb (01h.r5)* interrupt is removed except for erroneous sectors, the cache management should be implemented through *TCC (9Dh)*. If *TCINCEN (9Ch.5)* is high, *TCC (9Dh)* increments at the end of EDC-checking if there is no *STAERR (80h.r6)* or *HCEI (80h.r0)* error. If *ACMEN (9Ch.6)* is high, *TCC (9Dh)* decrements at the end of each data-in block transfer. The transfer of working area data should be implemented as linear transfer to prevent error.

Writing value to *SKIPC (9Eh)* can be used to implement the cache-partial-hit event. For the cache-miss event, *TCC (9Dh)* should be set 0.

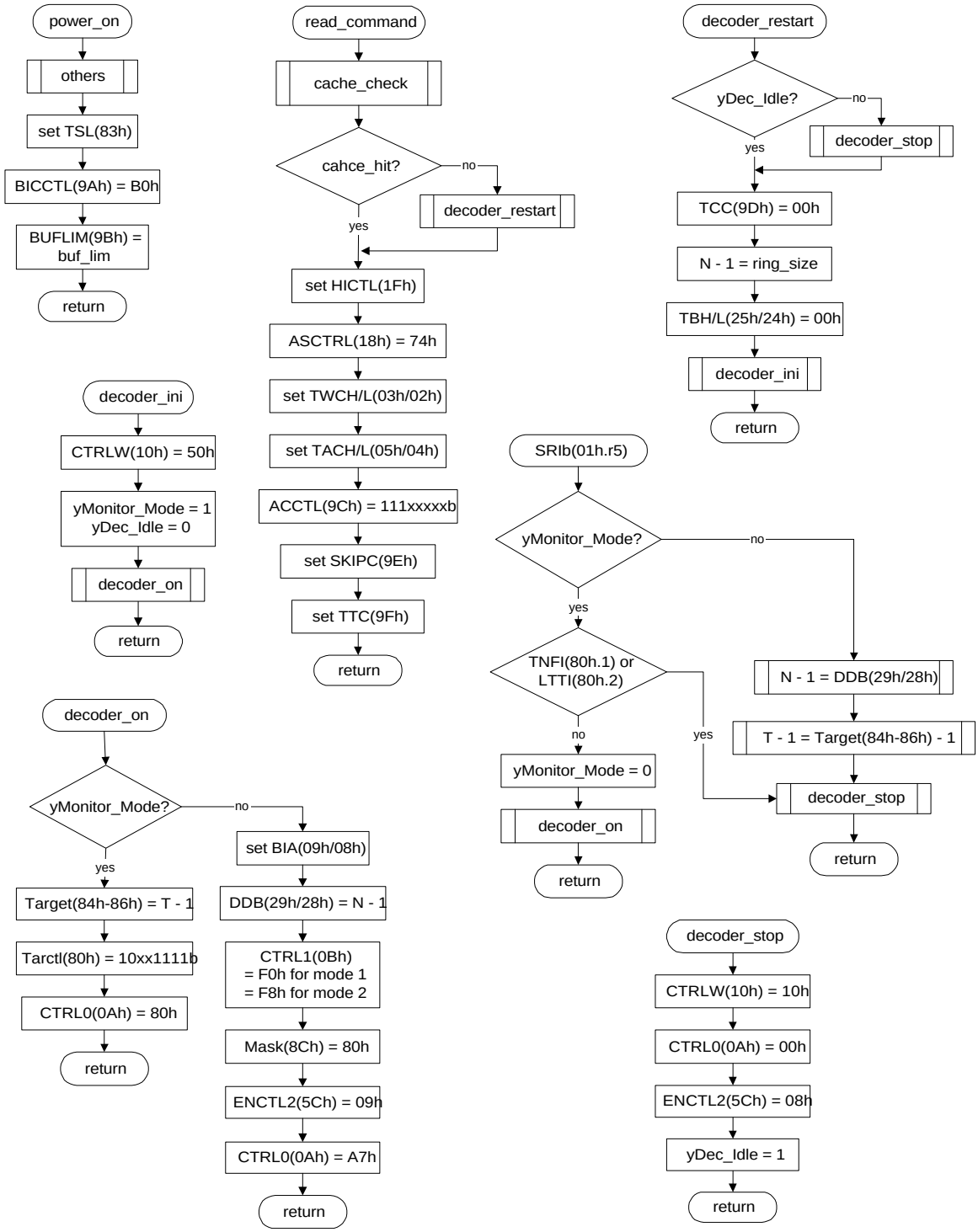
The stop of DSP buffering is implemented by following setting ininitialization to prevent buffer wrap-around:

- *BICCTL (9Ah)* ← B0h
- BUFLIM (9Bh) ← *cache_limit*

The following figure shows an example flowchart under following conditions:

- Buffer-Independent-Correction is enabled
- Remove frequent SRIb is enabled in buffer mode
- Automatic transfer and cache management is enabled
- Linear address transfer for working area data is enabled

In this case, the flag *TENDb (01h.r6)* is generated only when the last block is transferred to host, i.e., *TTC (9Fh)* is zero.


power_on
others
set TSL(83h)
BICCTL(9Ah) = B0h
BUFLIM(9Bh) = buf_lim
return
read_command
cache_check
cahce_hit?
no
yes
decoder_restart
set HICTL(1Fh)
ASCTRL(18h) = 74h
set TWCH/L(03h/02h)
set TACH/L(05h/04h)
ACCTL(9Ch) = 111xxxxxb
set SKIPC(9Eh)
set TTC(9Fh)
return
decoder_restart
yDec_Idle?
no
yes
decoder_stop
TCC(9Dh) = 00h
N - 1 = ring_size
TBH/L(25h/24h) = 00h
decoder_ini
return
decoder_ini
CTRLW(10h) = 50h
yMonitor_Mode = 1
yDec_Idle = 0
decoder_on
return
SRIb(01h.r5)
yMonitor_Mode?
no
yes
TNFI(80h.1) or LTTI(80h.2)
yes
no
N - 1 = DDB(29h/28h)
T - 1 = Target(84h-86h) - 1
decoder_stop
return
yMonitor_Mode = 0
decoder_on
return
decoder_on
yMonitor_Mode?
no
yes
Target(84h-86h) = T - 1
Tarctl(80h) = 10xx1111b
CTRL0(0Ah) = 80h
return
set BIA(09h/08h)
DDB(29h/28h) = N - 1
CTRL1(0Bh)
= F0h for mode 1
= F8h for mode 2
Mask(8Ch) = 80h
ENCTL2(5Ch) = 09h
CTRL0(0Ah) = A7h
return
decoder_stop
CTRLW(10h) = 10h
CTRL0(0Ah) = 00h
ENCTL2(5Ch) = 08h
yDec_Idle = 1
return

2.2.5 Audio-playback

2.2.5.1 Configuration Phase

1. Configure input/output pin for Audio-playback through *APCNF (90h).*
   - Bit 6: Audio Playback Interrupt Enable
   - Bit 4: Audio Reference Clock Select
   - Bit 3,2: Audio Input Reference Clock Setting
   - Bit 1:0: Audio Data Output Setting
2. Select Audio-playback output format through *APFMT (91h).*

After configuration, *pin ABCK* becomes active but data pin keep "mute."

2.2.5.2 Playback Phase

If the desired data sectors are buffered in DRAM, the following steps can trigger audio playback:

1. Set Audio-playback start block through *APBKH/L (93h/92h).*
2. Enable Audio-playback by setting *APEN (90h.7)* high.
3. Wait for interrupt or polling flag *APIb (01h.r2).*
4. If *APIEN (90h.6)* is enabled, write *APACK (97h,w)* to deactivate audio-playback-interrupt.
5. If buffer is not empty or end of command, go to step 3.
6. Disable Audio-playback by setting *APEN (90h.7)* low.

The status of playback is directly controlled by the setting of *APEN (90h.7).* So the buffer should be carefully managed to prevent noise or broken song.

2.2.5.3 IEC-958 Digital Audio Output

The digital output function complies with the IEC-958 standard. This internal function is automatically enabled after configuration of audio playback function. The digital audio signal is output to *pin GPIO2/DAOOUT/nFCE* when *DAOEN (87h.7)* is set high after master reset.

2.2.6 Function Differences Between W88227 and W88113CF

W88227	W88113CF
Internal Linear Address Transfer Counter is added	RAC(1Ch,1Dh,2Dh) can not be accessed during linear address transfer
TARGET (84h-86h) decrement by setting TARDEC (16h.w0) high	TARGET decrement must be performed by uP
Host write to Packet FIFO generate Automatic Status Completion only if ASCEN (18h.w5) is high and PFFACB (01h.w3) is low	Host write to Packet FIFO generate Automatic Status Completion if ASCEN (18h.w5) is high
TCC (9Dh) update source is controlled by TCCCTL (58h.3-0)	n/a
Also support 2 nRWE DRAM	Support 2 CAS DRAM only
CTRL0 can read from 0Ah	CTRL0 is write only to 0Ah
CTRL1 can read from 0Bh	CTRL1 is write only to 0Bh
TARCTL can read from 10h	TARCTL is write only to 80h
INTCTL can read from 11h	INTCTL is write only to 01h
SICTL0 cand read from 21h	SICTL1 is write only to 21h
MEMCF can read from 2Bh	MEMCF is write only to 2Bh
SICTL1 can read from 2Ch	SICTL1 is write only to 2Ch
New control bit PFFACB (01h.w3)	n/a
New control bit TARDEC (16h.w0)	n/a
New control bit TARINC (16h.w1)	n/a
New control bit TARINC7 (16h.w2)	n/a
New control bit D2EN (1Ah.w3)	n/a
New control bit ASCEND (21h.6)	n/a
New control bit QSIGEN (21h.5)	n/a
New control bit TWES (2Bh.3)	n/a
New register RASTA (2Dh,r)	n/a
Control bits (2Fh.w3-2) are re-defined	Control bits (2Fh.w3-2) as ARSTS
New global control registers (40h-43h)	n/a
New register TCCCTL (58h)	n/a
New control bit DSPDW (5Bh.2)	n/a
New control bit UDTA (8Ah.6)	n/a
New control bit APACENB (93h.5)	n/a
HRSTS (2Fh.w5-4) are obsolete	available
ALRT (5Bh.3) is obsolete	available
ASRIT (5Bh.6) is obsolete	available
ALE2 (5Ch.3) is obsolete	available
LSTA (48h-4Bh), LHD (4Ch-4Fh) are obsolete	available

2.2.7 Decoder Register Map

index	type	name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
-	r/w	IR	index							
00h	r	PFAR	b7	b6	b5	b4	b3	b2	b1	b0
01h 11h	w r	INTCTL	pfneen	tenden	srien	0	pffscb	0	dten	0
01h	r	INTREA	pfne	tend	srib	hcib	tbsyb	apib	dfrdyb	scib
02h	r/w	TWCL	b7	b6	b5	b4	b3	b2	b1	b0
03h	r/w	TWCH	latxf	x	x	x	b11	b10	b9	b8
04h	w	TACL	a7	a6	a5	a4	a3	a2	a1	a0
05h	w	TACH	a15	a14	a13	a12	a11	a10	a9	a8
06h	w	THTRG	data unused							
07h	w	TACK	data unused							
04h	r	HEAD0	header minutes (bcd)							
05h	r	HEAD1	header second (bcd)							
06h	r	HEAD2	header frames (bcd)							
07h	r	HEAD3	header mode (bcd)							
08h	w	BIAL	a7	a6	a5	a4	a3	a2	a1	a0
09h	w	BIAH	a15	a14	a13	a12	a11	a10	a9	a8
0Ah	r/w	CTRL0	decen	rtedc	edcen	acen	x	bufen	qcen	pcen
0Bh	r/w	CTRL1	sien	sden	dscren	cwen	m2rq	f2rq	mcrq	shden
0Ch	r	STAT0	crcok	ilsyn	nosyn	lbkf	wshort	sbkf	0	uceblk
0Dh	r	STAT1	bi2	bi1	bi0	hdera	0	0	0	shdera
0Eh	w	DHTACK	data unused							
0Eh	r	STAT2	rmod3	rmod2	rmod1	rmod0	mode2	nocor	rfera	rform
0Fh	w	FRST	data unused							
0Fh	r	STAT3	stavab	0	ecf	0	0	0	c2df	0
10h	w	CTRLW	0	swen	sdss	dcken	0	c2wen	eccrst	dsprst
11h	w	CRTRG	data unused							crrl
12h	r/w	MBTC0	mbvab/r	mbinc/r	0	mbc4	mbc3	mbc2	mbc1	mbc0
13h	r/w	MBTC1	0	0	0	0	0	mbtien	mbtfen	incmbc
14h	w	ECTRL	0	0	0	0	0	0	ir7f	disai
14h	r	SUBHO	subheader(file)							
15h	r	SUBH1	subheader(channel)							
16h	r	SUBH2	subheader(submode)							
17h	r	SUBH3	subheader(coding)							
16h	w	EVTRG	x	x	x	x	x	tarinc7	tarinc	tardec
17h	w	ASTRG	0	csrt	dsct	sigt	cpft	adtt	drqt	sct
18h	r/w	ASCTRL	apkten	adcen	ascen	autoen	stwcen	aucrcen	abyen	pktien
19h	w	CCTL0	ckstp	x	jpss	0	csk3	csk2	cks1	csk0
1Ah	w	CCTL1	clkoen	tsync	xininv	psken	clk1	clk0	0	xtald2
1Ah	r	VER	E7h							
1Bh	w	DSPSL	c2ml	s16o	lchp	sft8	d2en	sel16	dir	edge
1Bh	r	C2BEB	b7	b6	b5	b4	b3	b2	b1	b0

1Ch	w	RACL	a7	a6	a5	a4	a3	a2	a1	a0
1Dh	w	RACH	a15	a14	a13	a12	a11	a10	a9	a8
2Dh	w	RACU	0	0	0	0	a19	a18	a17	a16
1Eh	w	RAMWR	b7	b6	b5	b4	b3	b2	b1	b0
1Eh	r	RAMRD	b7	b6	b5	b4	b3	b2	b1	b0
1Fh	w	HICTL0	x	x	x	laen	mdma	pio	dinb	udma
1Fh	r	STAT5	utby	0	0	0	mdma	pio	dinb	udma
20h	r/w	HICTL1	0	pdiagen	daspen	clrbsy	setbsy	scod	rdyen	io16en
21h	w	SICTL0	0	0	ascend	qsigen	pqenb	subcs2	subcs1	subcs0
22h	w	SCIACK	data unused							
22h	r	SUBSTA	x	x	x	qcrcok	x	mss	nesbk	iss
24h	r/w	TBL	b7	b6	b5	b4	b3	b2	b1	b0
25h	r/w	TBH	data unused							b8
26h	r/w	SCBL	b7	b6	b5	b4	b3	b2	b1	b0
27h	r/w	SCBH	data unused							b8
28h	r/w	DDBL	b7	b6	b5	b4	b3	b2	b1	b0
29h	r/w	DDBH	data unused							b0
2Ah	w	RAMCF	rftyp	rftrg	x	swap	b3	rtc2	rtc1	rtc0
2Ah	r	RAMCF	rftyp	rftrg	rfc	swap	twes	rtc2	rtc1	rtc0
2Bh	r/w	MEMCF	0	0	0	0	dfrst	frdy	rlc1	rlc0
2Ch	r/w	SICTL1	sbxck	scen	cd2sc	scien	exinv	exop	scf1	scf0
2Dh	r	RASTA	rasta7	rasta6	rasta5	rasta4	rasta3	rasta2	rasta1	rasta0
2Eh	w	MISC0	hiien	0	drveb	mdrv	hirq	shien	0	0
2Eh	r	MISS0	1	1	srub	mdrvf	hintf	1	nPDIAG	nDASP
2Fh	w	MISC1	arrc	sarrc	hrsts1	hrsts0	arsts1	arsts0	arstien	arwc
2Fh	r	MISS1	srst	atac	diag	shdc	arst	rst	frst	hrst
30h	w	ARSTACK	data unused							
30h	r	MISS2	srstd	cmdc	tdir	mbti	ucrcokb	crst	fpkt	apkt
31h	w	ATERR	b7	b6	b5	b4	mcr	abrt	eom	ili
31h	r	ATFEA	0	0	0	0	0	0	0	dma
32h	r/w	ATINT	0	0	0	0	0	0	io	cod
33h	r/w	ATSPA	b7	b6	b5	b4	b3	b2	b1	b0
34h	r/w	ATBLO	b7	b6	b5	b4	b3	b2	b1	b0
35h	r/w	ATBHI	b7	b6	b5	b4	b3	b2	b1	b0
36h	r/w	ATDRS	1	l	1	drv	0	0	0	0
37h	w	ATSTA	0	drdy	0	dsc	drq	corr	0	check
37h	r	ATCMD	b7	b6	b5	b4	b3	b2	b1	b0
38h	w	ASERR	0	0	0	0	0	0	0	scheck
38h	r	ATSTA	bsy	drdy	b5	dsc	drq	corr	0	check
39h	w	ASERR	0	0	0	0	0	sabrt	0	0
39h	r	ATERR	b7	b6	b5	b4	mcr	abrt	eom	ili
3Ah	r	LDDBL	latched DDBL							
3Bh	r	LDDBH	latched DDBH							
3Dh	w	APKSTA	0	0	0	adsc	0	0	0	0
3Eh	w	ASCSTA	0	adrdy	0	0	0	acorr	0	acheck

3Fh	r/w	SHDCTL	0	shdrv	shdrvl	0	0	dasps2	dasps1	daspss
40h	r/w	CCSA0	b7	b6	b5	b4	b3	b2	b1	b0
41h	r/w	CCSA1	b7	b6	b5	b4	b3	b2	b1	b0
42h	r/w	CCSA2	b7	b6	b5	b4	b3	b2	b1	b0
43h	r/w	GLCTL1	rsto	x	x	up323s	x	ckostp	aclks	dclks
50h	r/w	DTRBL	b7	b6	b5	b4	b3	b2	b1	b0
51h	r/w	DTRBH	data unused							b8
52h	r/w	DTRCL	b7	b6	b5	b4	b3	b2	b1	b0
53h	r/w	DTRCH	data unused							b8
54h	r/w	WBRBL	b7	b6	b5	b4	b3	b2	b1	b0
55h	r/w	WBRBH	data unused							b8
56h	r/w	WBRCL	b7	b6	b5	b4	b3	b2	b1	b0
57h	r/w	WBRCH	data unused							b8
58h	r/w	TCCCTL	x	x	x	x	tccctl3	tccctl2	tccctl1	tccctl0
59h	r	PSKSTA	locked	onlock	psk5	psk4	psk3	psk2	psk1	psk0
59h	w	PSKCTL	psksel	locksel	psk5	psk4	psk3	psk2	psk1	psk0
5Ah	w	SCTC	d7	d6	d5	d4	d3	d2	d1	d0
5Bh	r/w	ENCTL1	asdma	obsolete	dsp1stb	b4	alectl	dspdw	dra	b0
5Ch	r/w	ENCTL2	x	x	x	x	obsolete	syncp	b1	rmsri
5Dh	r/w	GIOCF	g4cf3	g4cf2	g4cf1	g4cf0	g2cf	g3cf2	g3cf1	g3cf0
5Eh	r/w	PSKCNT	x	x	x	pskcnt4	pskcnt3	pskcnt2	pskcnt1	pskcnt0
5Fh	r/w	GIOCTL	g4oen	g3oen	g2oen	g1oen	gio4	gio3	gio2	gio1
80h 10h	w r	TARCTL	targen	dscen	qen	qmsf	astopb	ltten	tnfen	hceen
80h	r	TARSTA	targed	staerr	bin0	dsfuli	lastbk	ltti	tnfi	hcei
81h	w	DSTL	b7	b6	b5	b4	b3	b2	b1	b0
81h	r	DSCL	b7	b6	b5	b4	b3	b2	b1	b0
83h	w	TSL	b7	b6	b5	b4	b3	b2	b1	b0
83h	r	TSC	b7	b6	b5	b4	b3	b2	b1	b0
84h	r/w	TARGET0	target minute (bcd)							
85h	r/w	TARGET1	target second (bcd)							
86h	r/w	TARGET2	target fram (bcd)							
87h	r/w	DACTL	da0en	ctlsel	acu1	acu0	qctl3	qctl2	qctl1	qctl0
88h	r/w	FEACTL	lecas	lref	mrcd	sdbs	sbck	cas8b	frcdb	edoen
89h	r/w	DFFCNTL	1	1	ffht2	dffht1	dffht0	dfflt2	dfflt1	dfflt0
8Ah	r/w	ATCTL	dxoff	udta	udt1	udt0	uclks	reft1	reft1	reft0
8Ch	w	STA0M	crcokm	ilsynm	nosynm	lblkm	wshortm	sblkm	bin0m	uceblkm
8Dh	w	STA1M	0	0	0	hderam	0	0	0	shderam
8Eh	w	STA2M	0	0	0	0	0	nocorm	rferam	0
8Fh	w	STA3M	0	0	ecfm	0	0	0	c2dfm	0
90h	r/w	APCNF	apen	apien	demand	apins	apin1	apin0	apout1	apout0
91h	r/w	APFMT	apfmt7	apfm6	apfmt5	apfmt4	apfmt3	apfmt2	aptm1	apfmt0
92h	r/w	APBKL	b7	b6	b5	b4	b3	b2	b1	b0
93h	r/w	APBKH	test	test	apacenb	test	0	0	0	b8
94h	r/w	APWCL	97h							

95h	r/w	APWCH	04h							
96h	r/w	APVOL	lvol3	lvol2	lvol1	lvol0	rvol3	rvol2	rvol1	rvol0
97h	w	APACK	data unused							
98h	w	PUCTL	hip1	hip0	uip1	uip0	rip1	rip0	hd7upb	apipb
9Ah	r/w	BICCTL	bicen	atmsen	blimen	blims	rclim3	rclim2	rclim1	rclim0
9Bh	w	BUFLIM	b7	b6	b5	b4	b3	b2	b1	b0
9Bh	r	BUFC	b7	b6	b5	b4	b3	b2	b1	b0
9Ch	r/w	ACCTL	atten	acmen	tcincen	atlim4	atlim3	atlim2	atlim1	atlim0
9Dh	r/w	TCC	b7	b6	b5	b4	b3	b2	b1	b0
9Eh	r/w	SKIPC	b7	b6	b5	b4	b3	b2	b1	b0
9Fh	r/w	TTC	b7	b6	b5	b4	b3	b2	b1	b0

IR - Index Register

The Decoder Index Register is latched from uP Port-0 by the buillt-in 74373 at the falling edge of internal *ALE* signal. The high byte address of decoder register is defined by *CCSA0 (40h)* with default value 40h.

<example>: decoder register read (read VER)

```
MOV   DPTR,#0401Ah
MOVX  A,@DPTR
```

<example>: decoder register write (set CCSA1 as 0xC0h)

```
MOV   A,#0C0h
MOV   DPTR,#04041h
MOVX  @DPTR,A
```

PFAR - Packet FIFO Access Register - (read 00h)

While *SCoD (20h.2)* is high, the ATAPI Command Packet issued from host is received by the 12-byte Packet FIFO. Flag *TENDb (01h.r6)* and *FPKT (30h.r1)* are used to check if the Packet FIFO is full. The microprocessor can read the ATAPI Command Packet by repeatedly read register *PFAR (00h,r)*. Once the FIFO becomes empty, the value FFh will be returned if microprocessor read PFAR.

The Packet FIFO can also be used to receive command parameter less than 12 bytes. First, the control bit *SCoD (20h.2)* is set high to select the Packet FIFO to be addressed by the ATAPI Data port. When *DRQ (37h.3)* changes from 0 to 1, the lower 4 bits of *ATBLO (34h)* is latched as the FIFO threshold. Upon the number of bytes in the FIFO reaches the threshold, flag *TENDb (01h.r6)* becomes active-low and flag *FPKT (30h.r1)* becomes active-high. Once *FPKT* becomes high, any data writes to the ATAPI Data port is rejected.

INTCTL - Interrupt Control Register - (write 01h, read 11h)

Bit 7: PFNEEN - Packet FIFO Not Empty Interrupt Enable

If this bit is high, decoder interrupt activates when *PFNEb (01h.r7)* becomes active-low. This bit is clear to 0 after master reset, firmware reset.

Bit 6: TENDEN - Transfer End Interrupt Enable

If this bit is high, decoder interrupt activates when *TENDb (01h.r6)* becomes active-low. This bit is also automatically enabled if the host issues the PACKET Command (opcode A0h) while *HIIEN (2Eh.w7)* is high and drive is selected. This bit is clear to 0 after master reset, firmware reset.

Bit 5: SRIEN - Sector Ready Interrupt Enable

If this bit is high, decoder interrupt activates when *SRIb (01h.r5)* becomes active-low. This bit is clear to 0 after master reset, firmware reset and decoder reset.

Bit 4: reserved

Bit 3: PFFSCB - Packet FIFO Full Trigger Status Completion Enable

If this bit is low and *ASCEN (18h.5)* is high, the *autmatic status completion* is performed after the end of data transfer into Packet FIFO. This bit is clear to 0 after master reset, firmware reset.

Bit 2: reserved

Bit 1: DTEN - Data Transfer Enable

Set this bit high enables the data transfer logic. This bit should be set before trigger any data transfer. In order to reduce the interference of microprocessor, this bit is also automatically enabled during the following operation:

- Trigger *ADTT (17h.w2)*
- Host issues PACKET Command (opcode A0h) while *APKTEN (18h.7)* is enabled and drive is selected

In case of un-recoverable transfer error, setting this bit low will terminate the current data transfer immediately.

Bit 0: Reserved

INTREA - Interrupt Reason Register - (read 01h)

Bit 7: PFNEb - Packet FIFO Not Empty Interrupt Flag

This bit becomes active-low after Packet FIFOs receive any data issued by the host through ATAPI Data port. *Decoder interrupt* is activated when this bit becomes active-low if *PFNEEN (01h.w7)* is enabled. This flag and intterupt is deactivated after the last byte is read by microprocessor through register *PFAR (00h,r)*.

Bit 6: TENDb - Transfer End Interrupt Flag

This bit becomes active-low at the end of data transfers. Flag *TDIR (30h.r5)* and *FPKT (30h.r1)* can be used to determine which type of transfer end occurs. *Decoder interrupt* is activated when this bit becomes active-low if *TENDEN (01h.w6)* is enabled.

TENDb (01h.r6)	TDIR (30h.r5)	FPKT (30h.1)	Transfer End Reason	Interrupt Acknowledge register
0	1	0	data-in transfer	DHTACK (0Eh), TACK (07h)
0	1	x	data-out transfer	TACK (07h)
0	0	x	A0 command packet transfer	TACK (07h)

Bit 5: SRIb - Sector Ready Interrupt Flag

If *RMSRI (5Ch.0)* is low, this bit is used to indicate that one sector is ready to be accessed. If *RMSRI (5Ch.0)* is high, this bit is generated only by *STAERR (80h.r6)*, *BIN0 (80h.r5)*, *DSFULI (80h.r4)*, *LASTBK (80h.r3)*, *LTTI (80h.r2)*, *TNFI (80h.r1)* or *HCEI (80h.r0)*.

Reading register *STAT3 (0Fh,r)* or *TARSTA (80h,r)* deactivates this flag and its corresponding interrupt.

Bit 4: HCIb - Host Command Interrupt Flag

This bit is activated by the following events:

(1) Host set bit SRST in ATAPI Device Control Register, if *HIIEN(2Eh.7)* is enabled. This event also activates flag SRST (2Fh.r7). The interrupt is acknowledged by master reset, reading *ATCMD (37h)* or setting *CLRBSY (20h.4)* high.

(2) Host issues command other than PACKET and DEVICE RESET command to this drive, if drive is selected and *HIIEN(2Eh.7)* is enabled. This event also activates flag *ATAC (2Fh.6)*. This flag and interrupt is acknowledged by master reset, reading *ATCMD (37h)* or setting *CLRBSY (20h.4)* high.

(3) Host issues Execute Drive Diagnostics Command, if *HIIEN(2Eh.7)* is enabled. This event also activates flag *DIAG (2Fh.r6)*. This flag and interrupt is acknowledged by master reset, reading *ATCMD (37h)* or setting *CLRBSY (20h.4)* high.

(4) Host issues command to a non-exist slave drive, if *SHIEN(2Eh.2)* is enabled. This event also activates flag *SHDC (2Fh.r4)*. This flag and interrupt is acknowledged by master reset, reading *ATCMD (37h)* or setting *CLRBSY (20h.4)* high.

(5) Host issues DEVICE RESET Command, if *ARSTIEN(2Fh.1)* is enabled. This event also activates flag *ARST (2Fh.r3)*. This flag and interrup is acknowledged by writing any value to *ARSTACK (30h,w)*.

Bit 3: TBSYb - Transfer Busy Flag

This bit becomes active-low when the data transfer to host is triggered by the following events:

- Writing any value to register *THTRG (06h,w)*
- Setting bit *ADTT (17h.w2)* high

After host read the last byte to be transferred, this flag is deactivated.

Bit 2: APIb - Audio Playback Interrupt Flag

If *APOUT (90h,1-0)* are not zero, this bit is used as audio-playback-interrupt flag. If *APIEN (90h.6)* is high, this bit activats whenever the playback of one block is finished, The corresponding interrupt is acknowledged by writing any value to *APACK (97h,w)*.

Bit 1: DFRDYb - Data FIFO Ready

After data transfer is triggered, the 32-byte Data FIFOs is automatically filled. This bit is used to indicate that the Data FIFOs is ready to be read by the host for debugging. The Data FIFO is automatically cleared in any of the following conditions:

- Chip reset, host reset and firmware reset
- *DTEN (01h.w1)* is 0
- *DINB (1Fh.w1)* is 1
- *DFRST (2Bh.w3)* is 1
- The end of data-in transfer

Bit 0: SCIb - Subcode Interrupt Flag

If *SCIEN (2Ch.w4)* is enabled, this bit becomes active-low when one of the following events occurs:

- *ISS (22h.r0)* becomes active-high
- *NESBK (22h.r1)* becomes active-high
- *MSS (22h.r2)* becomes active-high

When Subcode Interrupt is activated, the microprocessor can read register *SUBSTA (22h,r)* to determine the reason of interrupt. Writing register *SCIACK (22h,w)* deactivates this flag and its corresponding interrupt.

TWCL - Transfer Word Counter Low- (read/write 02h)

Before triggering data transfer, the number of words to be transferred should be set through 12-bit Transfer Word Counter (TWC). The number of **words** minus 1 should be written to this counter while using standard ATAPI 16-bit data transfer. After host read one word, the counter is decreased by one. *Transfer End Interrupt Flag, TENDb (01h.r6)*, is activated when this counter becomes zero.

Bit 7-0: TWCH[7:0] - Transfer Word Count Low

TWCH - Transfer Word Counter High - (read/write 03h)

Bit 7: LATXF - Linear Address Transfer Enable

If this bit is high, the Linear Address Transfer is enabled. In this case, the data stored from the ddress specified by *RAC (2Dh,1Dh,1Ch)* are transferred to host after trigger. The size of transfer data is limited by *TWC (03h/02h)*.

If this bit is low, the Block-Offset Transfer is enabled. In this case, the data stored from the address specified by *TBH/L (25h/24h)* and *TACH/L (05h/04h)* are transferred to host after trigger. The address of data warps around at the block boundary, so the size of transfer data is limited by block size.

Bit 3-0: TWCH[3:0] - Transfer Word Count High

TACL/TACH - Transfer Address Counter - (write 04h/05h)

Before triggering block-offset data transfer, the external RAM address of data to be transferred should be set through *TACH/L (05h/04h,w)*. This number in this counter specifies the first available data address relative to the beginning of the block. The block number should also be specified through Transfer Block registers *TBH/L (25h/24h)*. After one word is read by host, *TACH/L* are incremented to the next available data address. The following equation illustrates the relation between block-offset and linear address:

```
linear address = (block number × block size) + address offset
```

THTRG - Transfer to Host Trigger Register - (write 06h)

This register is used to trigger data transfer regardless of what value is written. If *DINB (1Fh.1)* is low, triggering this register automatically fills the Data FIFO and then flag *DFRDYb (01h.r1)* becomes active-low when the Data FIFO becomes ready. If *DINB (1Fh.1)* is high, data-out transfer is enabled, e.g., parameter of mode-select command. A more convenient way is set *ADTT (17h.w2)* high and then trigger hardware data transfer sequence.

TACK - Transfer Acknowledge - (write 07h)

Writing any value to this register deactivates flag *TENDb (01h.r6)* and its corresponding interrupt.

HEAD0 to HEAD3 - Header Registers - (read 03h to 07h)

These four registers are used to hold the information of Header Bytes of each sector. Header Registers should be read soon after *STAVAb (0Fh.r7)* becomes active-low. Note that the header bytes are distrustful if wrong mode is set while ECC is enabled. If bit *SHDEN (0Bh.w0)* is enabled, registers *HEAD0-3* are used to hold subheader bytes instead.

If control bit *QMSF (80h.w4)* is set high, the corresponding MSF bytes in Q-channel information would be automatically loaded into *HEAD0-2 (04h-06h,r)* when each byte is ready from DSP. The register *HEAD3 (07h,r)* hold first byte of Q-channel (CONTROL and ADR) or 0xFFh if CRC checking of Q-code is erroneous.

BIAL/BIAH - Buffering Initial Address - (write 08h/09h)

The rule for configuration is that the first byte of the sector is stored at

```
BIAH/L(09h/08h) - 0Ch
```

Before enabling the external RAM buffering through *CTRL0 (0Ah,w)*, *BIAH/L* should be set to control the location of the first byte follows data sync for each data sector. The RAM block for buffering is controlled by the number in registers *DDBH/L(29h/28h)* plus one.

BACL, BACH - Buffering Address Counter - (read 0Ah/0Bh) - Obsolete

EIAL/EIAH - ECC Initial Address - (read 08h/09h, write 0Ch/0Dh) - Obsolete

CTRL0 - Control Register 0 - (read/write 0Ah)

This register is 0 after chip reset, host reset, firmware reset and decoder reset.

Bit 7: DECEN - Decoding Logic Enable

Setting this bit high enables the decoding logic.

Bit 6: RTEDC - Real Time EDC Checking Enable

Setting this bit high enables the real-time-EDC-checking logic. The RSPC error correction is performed only when the result of real time EDC check is error.

Bit 5: EDCEN - Error Detect and Correct Enable

Setting this bit high enables the ECC and EDC logic. Change of this bit takes effect after next sync.

Bit 4: ACEN - Automatic Correction Enable

If both *M2RQ (0Bh.w3)* and this bit is high, the type of error correction is automatically determined by FORM bit in the subheader byte. If only *M2RQ (0Bh.w3)* is high, the type of error correction is controlled by *F2RQ (0Bh.w2).* If *M2RQ (0Bh.w3)* is low, this bit does not affect the correction of mode 1 data.

Bit 3: PKTINH - obsolete

Bit 2: BUFEN - Buffering Enable

Setting this bit high enables incoming DSP data buffering. When this bit is high, the values of register *HEAD (04h-07h)* and *SUBH (14h-17h)* are retrieved from external RAM rather than from incoming serial data. When *BUFEN* is low, any setting of *QCEN* or *PCEN* is meaningless. Change of this bit takes effect after next sync.

Bit 1: QCEN - Q-codeword Correction Enable

When this bit is high, Q-codeword RSPC correction logic is enabled. Change of this bit takes effect after next sync.

Bit 0: PCEN - P-codeword Correction Enable

When this bit is high, P-codeword RSPC correction logic is enabled. Change of this bit takes effect after next sync.

DECEN 0Ah.7	BUFEN 0Ah.2	EDCEN 0Ah.5	QCEN 0Ah.1	PCEN 0Ah.0	Decoder Mode	Operation Flow	Remark
1	1	1	1	1	Q-P correction	Q → P → CRC	
1	1	1	1	0	Q-correction	Q → CRC	
1	1	1	0	1	P-correction	P → CRC	
1	1	1	0	0	Buffer-only	CRC	
1	1	0	0	0	Buffer-only	no CRC check	for M2F2 data without EDC
1	0	0	0	0	Disk-monitor	no buffering	
0	X	X	X	X	Decoder disable	no operation	

Note that if *ATMSEN (9Ah.6)* is high, the decoder logic will operate in Disk-monitor mode before the target is found. When the target is found, the setting of register *CTRL1 (0Bh,w)* will be automatically loaded into decoder logic.

CTRL1 - Control Register 1 - (read/write 0Bh)

This register is 0 after chip reset, host reset, firmware reset and decoder reset.

Bit 7: SIEN - Sync Insertion Enable

When this bit is high, the sector boundary is determined by internal sync insertion logic.

Bit 6: SDEN - Sync Detection Enable

When this bit is high, the sector boundary is determined by sync bytes of incoming serial data. This bit should not set for reading CD-DA data.

Bit 5: DSCREN - Descramble Enable

Setting this bit is high enables the descramble logic. This bit should not set for reading CD-DA data.

Bit 4: CWEN - Corrected Data Write Enable

Setting this bit high enables corrected data to be written to the external RAM. This bit is normally set when correction is enabled by *QCEN (0Ah.w1)* or *PCEN (0AH.w0)*.

Bit 3: M2RQ - Mode 2 ECC Request

Setting this bit to high enables the CD-ROM XA mode 2 correction logic. Yellow book Mode 1 correction will be performed if this bit is low.

Bit 2: F2RQ - Form 2 Request

Setting this bit high request the data to be processed by the CD-ROM XA mode-2 form-2 format if *M2RQ (0Bh.3)* is high. If *M2RQ (0Bh.3)* is high and this bit is low, the CD-ROM X1 mode-2 form-1 correction will be performed. This bit is not effective if *ACEN (0Ah.w4)* is high.

Bit 1: MCRQ - Mode Byte Check Request

When this bit is high, ECC logic will check the 4th header byte with the setting of *M2RQ (0Bh.3)* to determine if ECC correction to be performed.

Bit 0: SHDEN - Subheader Switch Enable

When this bit is high, registers *HEAD (04h-07h,r)* are used to provide subheader bytes.

disc format	SIEN (0Bh.7)	SDEN (0Bh.6)	DESCREN (0Bh.5)	CWEN (0Bh.4)	M2RQ (0Bh.3)	F2RQ (0Bh.2)
CD-DA	1	0	0	0	0	0
yellow book Mode 1	1	1	1	1	0	0
yellow book Mode 2	1	1	1	0	0	0
CD-ROM XA M2F1	1	1	1	1	1	0
CD-ROM XA M2F2	1	1	1	x	1	1

STAT0 - Status Register 0 - (read 0Ch)

Bit 7: CRCOK - Cyclic Redundancy Check OK

This bit is used to indicate that the Cyclic Redundancy Check of the latest available sector is passed.

Bit 6: ILSYN - Illegal Sync Pattern

If *SDEN (0Bh.w6)* is high, this bit becomes high when a sync pattern is detected less than 2352 bytes after last sync pattern was detected/inserted.

Bit 5: NOSYN - No Sync Pattern

If *SIEN (0Bh.w7)* is high, this bit becomes high when a sync pattern is not detected at 2352 bytes after last sync pattern was detected/inserted.

Bit 4: LBKF - Long Block Flag

If *SIEN (0Bh.w7)* is low, this bit becomes high when a sync pattern is not detected at 2352 bytes after last sync pattern was detected/inserted.

Bit 3: WSHORT - Word Short

This bit becomes high when the incoming serial data rate is too high to be processed.

Bit 2: SBKF - Short Block Flag

If *SDEN (0Bh.w6)* is low, this bit becomes high when a sync pattern is detected less than 2352 bytes after last sync pattern was detected/inserted.

Status Flag	SIEN (0Bh.7)	SDEN (0Bh.6)	Internal Operation
ILSYN(0Ch.6)	x	1	re-synchronize internal sync logic
NOSYN(0Ch.5)	1	x	internal sync logic provide internal sector boundary
LBKF(0Ch.4)	0	x	internal sync logic do not provide internal sector boundary
SBKF(0Ch.2)	x	0	do not re-synchronize internal sync logic

Bit 1: reserved

Bit 0: UEBK - Uncorrectable Errors in Block

This bit is used to indicate that at least one data is corrected in the latest available data block.

STAT1 - Status Register 1 - (read 0Dh)

Bit 7-5: BI[2:0] - Raw Block Indicator

Bit 4: HDERA - Header Erasure

This bit is high if there is at least one erasure flag detected in header bytes excluding mode byte. Erasure in mode byte will cause *RMOD (0Eh.r7-4)* all become high.

Bit 0: SHDERA - Subheader Erasure

This bit is high if erasure flags are detected for both bytes in at least one subheader byte-pairs. Erasures are latched from pin C2PO it *BUFEN (0Ah.w2)* is disabled. Otherwise, header and subheader bytes are retrieved from external RAM while the following sector is being buffered.

DHTACK - DRAM to Host Transfer Acknowledge - (write 0Eh)

Writing DHTACK, regardless of what data is written, deactivates *TENDb (01h.r6)* that caused by data-in transfer.

STAT2 - Status Register 2 - (read 0Eh)

Bit 7-4: RMOD[3:0] - Raw Mode Bit

RMOD2-0 are directly latched from bit 2-0 from the 4th header byte and RMOD3 is high if any one of the other 5 bits in the mode byte is high. RMOD3 is also high if a mode byte erasure is detected.

Bit 3: MODE2 - Mode 2 Selected Flag

This bit reflects the setting of *M2RQ (0Bh.w3).*

Bit 2: NOCOR - No Correction

If ECC logic is enabled by bit *EDCEN (0Ah.w5)*, and *QCEN (0Ah.w1)* or *PCEN (0Ah.w0)*, this bit becomes high if ECC logic is interrupted the followings:

- *CWEN (0Bh.w4)* is disabled.
- Mode mismatch is detected while *MCRQ (0Bh.w1)* is enabled.
- Mode erasure is detected while *MCRQ (0Bh.w1)* is enabled. A mode erasure occurs if the incoming C2PO flag is set for the fourth header byte, indicating unreliable mode data.
- Form 2 enabled while ECC logic is set to mode 2. Form 2 blocks should not be corrected. Form 2 can be enabled by control bit *F2RQ (0Bh.w2)*, or by the Form bit in the Subheader byte if *ACEN (0Ah.w4)* is enabled.
- Form bit erasure while ECC logic is set to mode 2 and ACEN is enabled. A form bit erasure is detected if the incoming C2PO flags are set for both Form bits in the Subheader bytes.
- *ILSYN (0Ch.r6)* becomes high while *SDEN (0Bh.w6)* is enabled

Bit 1: RFERA - Raw Form Erasure

This bit becomes high when a form bit erasure was detected. A form bit erasure is detected if the incoming C2PO flags are set for both Form bits in the Submode bytes (bit 5 in byte 18 and 22). RFERA becomes valid when *SRIb (01h.r5)* becomes active-low, and remains valid until the next block sync.

Bit 0: RFORM - Raw Form Bit

This bit is high if the Form bit is high in the Submode bytes of the incoming serial data. This bit becomes valid when flag *SRIb (01h.r5)* becomes active-low, and remains valid until the next block sync.

FRST - Firmware Reset Register - (write 0Fh)

Writing this register, regardless of what value is written, trigger a firmware reset. Flag *FRST (2Fh.r1)* is set by firmware reset.

STAT3 - Status Register 3 - (read 0Fh)

Bit 7: STAVAb - obsolete, may return 0 or 1

Bit 5: ECF - Error Corrected Flag

This bit is used to indicate that there is at least one byte was corrected in the latest available block.

Bit 1: C2DF - C2 Detected in Block Flag

If *C2WEN (10h.w2)* is high, C2DF becomes high when there is at least one C2PO flag was detected in the previous block.

Bit 6,4,3,2,0: Reserved

CTRLW - Control-Write Register - (write 10h)

This register is 0 after chip reset, host reset, firmware reset and decoder reset.

Bit 7: reserved

Bit 6: SWEN - Synchronized Write Enable

If this bit is high, the change of *BUFEN (0Ah.w2)* will be synchronized to the end of next sector sync. The buffering of C2PO flags is also controlled by this bit if *C2WEN (10h.w2)* and *BUFEN (0AH.w2)* are both enabled. This function prevents buffering of an incomplete block.

Bit 5: SDSS - Subcode and DSP Sync Synchronization

This bit provides synchronization of CD-DA format data. If this bit is high, the writing of incoming serial data to the external RAM will start at the first left-channel lower-byte following the end of subcode block. Note that this bit should not be used when subcode logic is not enabled.

Bit 4: DCKEN - DSP Clock Enable

If this bit is high, clock from DSP is used by internal decoder logic. DCKEN should be set high before *DECEN (0Ah.w7)* is set high.

Bit 3,0: reserved

Bit 2: C2WEN - C2 Flag Write Enable

If this bit and *BUFEN (0Ah.w2)* are both high, the C2 flags of incoming serial data will be latched into the external RAM. This operation is synchronized to the end of sync if *SWEN (10h.w6)* is high.

Bit 1: ECCRST - ECC logic reset trigger

Setting this bit to high resets decoding logic, including:

- *SRIEN (01h.w5)* ← 0
- *CTRL0 (0Ah,w)* ← 00h
- *CTRL1 (0Bh,w)* ← 00h
- *STAT0-2 (0Ch-0Eh,r)* ← 00h
- *STAT3 (0Fh,r)* ← 80h
- *TARSTA (80h,r)* ← 00h

ECCRST is automatically cleared by itself.

Bit 0: DSPRST - DSP interface reset trigger

Setting this bit to high resets dsp interface. DSPRST is automatically cleared by itself.

CRTRG - Correction Retry Trigger - (write 11h)

Writing register CRTRG, regardless of what data is written, triggers the decoding logic to perform another correction sequence to the same block.

Bit 7-1: reserved

Bit 0: CRRL - Correction Retry Register Load

Setting this bit high while writing register *CRTRG (11h,w)* re-loads the setting of *EDCEN (0Ah.w5)*, *QCEN (0Ah.w1)*, or *PCEN (0Ah.w0)* to decoding logic.

Decoder Parameter	Updated at the end of sync	Updated by writing CRRL
EDCEN (0Ah.w5)	yes	yes
QCEN (0Ah.w1)	yes	yes
PCEN (0Ah.w0)	yes	yes
ACEN (0Ah.w4)	yes	no
BUFEN (0Ah.w2)	yes	no
M2RQ (0Bh.w3)	yes	no
F2RQ (0Bh.w2)	yes	no
MCRQ (0Bh.w1)	yes	no

MBTC0 - Multi-Block Transfer Control 0 - (read/write 12h)

The host interface supports multi-block transfer without microprocessor intervention by following sequence:

- *MBC (12h.4-0)* ← the number of block to be transferred minus 1 (ex. 3)
- *TWCH/L (03h/-2h)* ← the number of words to be transferred in each block minus 1 (ex. 1175)
- *TACH/L (05h/04h)* ← the starting point of the block (ex. F4h, FFh)
- *TBH/L (25h/24h)* ← the RAM block number of the first block to be transferred (ex. 5)
- *ATBHI/LO (35h/34h)* ← the total bytes to be transferred (ex. 9408)
- *ADTT (17h.w4)* ← 1

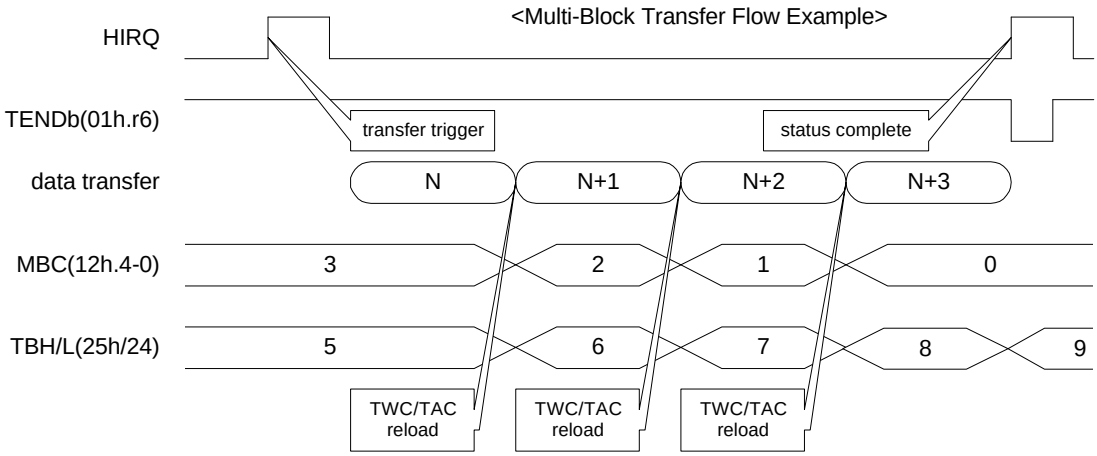
PS: *STWCEN (18h.3)* should not be set in multi-block transfer operation.

When *ADTT* is set, host will receive HIRQ, check status, and then start to read data.

After the last word of one block (except the last one) is read by the host, the following hardware sequence is executed:

- *TWCH/L (03h/02h)* ← reload
- *TACH/L (05h/04h)* ← reload
- *TBH/L (25h/24h)* ← auto-increment
- *MBC0 (12h.4-0)* ← auto-decrement

Flag *TENDb (01h.r6)* only becomes active at the end of data transfer of the last block. This register is 0 after chip reset, host reset and firmware reset.



Bit 7: MBVAb - Multi-Block Counter Valid Flag

This bit is used to indicate that *MBC (12h.4-0)* is stable enough to be monitored by microprocessor. There is no need to monitor this bit in normal operation.

Bit 6: MBINC - Multi-Block Increment Flag

This bit becomes active-high if microprocessor sets *INCMBC (13h.w0)* and multi-block number increment has not completed. There is no need to monitor this bit in normal operation.

Bit 4-0: MBC[4:0] - Multi-Block Counter

Before triggering multi-block transfer, the number of blocks to be transferred minus 1 should be written to *MBC (12h.4-0)*. Single block transfer is performed if *MBC (12h.4-0)* is zero. There is no need to monitor this counter normal operation.

MBTC1 - Multi-Block Transfer Control 1 - (read/write 13h)

This register is for debug only. This register is 0 after chip reset, host reset and firmware reset.

Bit 7-3: Reserved

Bit 2: MBTIEN - Multi-Block Transfer Interrupt Enable

If *MBTIEN* and *MBTFEN* are both enabled, *Decoder interrupt* will activate at the end of data transfer of each block if the block count in *MBC (12h.4-0)* is not zero. There is no need to set this bit in normal operation.

Bit 1: MBTFEN - Multi-Block Transfer Interrupt Flag Enable

If this bit is high, *MBTI (30h.r4)* will be activated at the end of data transfer of each block if the block count in *MBC (12h.4-0)* is not zero. There is no need to set this bit in normal operation.

Bit 0: INCMBC - Increment Multi-Block Counter

Setting this bit high increments *MBC (12h.4-0)*. This function is useful in data transfer to host by DMA mode. Because data byte count is not specified in DMA mode transfer, the number of block to be transferred can be incremented when a new block becomes available before the transfer is completed.

ECTRL - Enhanced Control Register - (write 14h)

Bit 7-2: Reserved

Bit 1: IR7F - Provide Flag UTBY at IR7

When this bit is high, flag *UTBY (1Fh.r7)* can be monitored by read bit-7 of the Index Register.

Bit 0: DISAI - Disable Auto-Increment of Microprocessor-RAM Address Counter

When this bit is high, the automatic increment of the *RAC (2Dh/1Dh/1Ch)* address counter is disabled. Note that DISAI should be 0 before *RFTRG (2Ah.w6)* is triggered.

SUBH0 to SUBH3 - Subheader Registers - (read 14h to 17h)

These registers are used to hold the information of subheader bytes. If *BUFEN (0Ah.w2)* is disabled, subheader bytes are latched from incoming serial data. If *BUFEN (0Ah.w2)* is enabled, subheader bytes are retrieved from the external RAM.

EVTRG - Event Trigger Register (write 16h)

The following bits will clear themselves after the triggered operation are completed. These bits should not be set while *DECEN (0Ah.7)* is high to avoid conflict with normal Target increment on end of CRC-checking.

Bit 7-2: Reserved

Bit 2: TARINC7 - Target Registers Increment 7 Trigger

Setting this bit high increments the *TARGET (84h-86h)* by 7.

Bit 1: TARINC - Target Registers Increment Trigger

Setting this bit high increments the *TARGET (84h-86h)* by 1.

Bit 0: TARDEC - Target Registers Decrement Trigger

Setting this bit high decrements the *TARGET (84h-86h).*

ASTRG - Automatic Sequence Trigger Register (write 17h)

The following bits will clear themselves after the triggered operation are completed.

Bit 7: Reserved

Bit 6: CSRT - Clear Soft Reset Trigger

Setting this bit high clears bit SRST in the ATAPI Device Control Register.

Bit 5: DSCT - Disk Seek Complete Trigger

If *ABYEN (18h.1)* is high, setting *DSCT* high triggers the following operations:

- Set BSY
- DSC (37h.4) ← 1
- Clear BSY

If *ABYEN (18h.1)* is low, setting *DSCT* high sets DSC(37h.4) to 1.

Bit 4: SIGT - ATAPI Signature Trigger

Setting this bit high initialize the Task Registers with ATAPI signature.

- ATFEA (31h) ← 00h
- ATERR (31h) ← 01h
- ATINT (32h) ← 01h
- ATSPA (33h) ← 01h
- ATBLO (34h) ← 14h
- ATBHI (35h) ← EBh
- ATSTA (37h) ← x00x0000b

Note that register ATDRS (36h) is not cleared by triggering SIGT to abide by the ATAPI protocol.

Bit 3: CPFT - Clear Packet FIFO Trigger

Setting this bit high clears the Packet FIFO.

Bit 2: ADTT - Automatic Data Transfer Trigger

If *PIO (1Fh.2)* is high, setting ADTT high triggers the following PIO Data Transfer sequence:

- Set BSY
- *DTEN (01h.w2)* ← 1
- *SCoD (20h.2)* ← 0 if *DINB (1Fh.1)* is 0; otherwise, 1
- ATINT (32h) ← 02h if *DINB (1Fh.1)* is 0; otherwise, 00h
- If *STWCEN (18h.w3)* is enabled, then ATBHI/LO ← (TWCH/L + 1) × 2

The data transfer logic will start to fill the Data FIFO automatically. The following sequence will be executed when *DFRDYb (01h.r1)* become active-low:

- DRQ (37h.3) ← 1
- Clear BSY
- *HIRQ (2Eh.3)* ← 1

After detecting the interrupt, the host will check the status and then read the data.

STWCEN (18h.3) should not be used for Automatic Multiple Block Transfer. Instead, ATBLO, ATBHI should be set by firmware to: `(MBC + 1) × ((TWC + 1) × 2)`

If *PIO (1Fh.2)* is low, setting ADRTG high triggers the following DMA Data Read sequence:

- Set BSY
- *DTEN (01h.w1)* ← 1
- *SCoD (20h.2)* ← 0 if *DINB (1Fh.1)* is 0; otherwise, 1
- ATINT (32h) ← 02h if *DINB (1Fh.1)* is 0; otherwise, 00h

Bit 1: DRQT - DRQ Trigger

If bit PIO (1Fh.2) is high, setting this bit high triggers the following hardware sequence:

- DRQ (37h.3) ← 1
- BSY ← 0
- *HIRQ (2Eh.3)* ← 1

When bit PIO is low (DMA mode), this bit should not be triggered.

Bit 0: SCT - Status Completion Trigger

Setting this bit high triggers the following hardware sequence:

- CHECK (37h.0) ← ACHECK (3Eh.0)
- CORR (37h.2) ← ACORR (3Eh.2)
- DRDY (37h.6) ← ADRDY (3EH.6)
- ATINT (32h) ← 03h
- Clear BSY
- *HIRQ (2Eh.3)* ← 1
- *APKTEN (18h.7)* ← 1, if *AUTOEN (18h.4)* is high
- *ASCEN (18h.5)* ← 0

After detecting the interrupt, the host reads the ATAPI Status Register and if necessary, the Error Register for the command completion status.

ASCTRL - Automatic Sequence Control register - (read/write 18h)

Bit 7: APKTEN - Automatic Packet Transfer Enable

Setting this bit high enables Automatic Packet Transfer logic. When APKTEN is high, the following hardware sequence is performed if host issues opcode A0h to the ATA Command Register if drive has been selected:

- Set BSY (37h.7)
- *APKT (30h.r0)* ← 1
- Clear Packet FIFO
- ATERR (31h) ← 00h
- ATINT (32h) ← 01h
- *DTEN (01h.w1)* ← 1
- *TENDEN (01h.w6)* ← 1, if *HIIEN (2Eh.7)* is high
- *SCoD (20h.2)* ← 1
- CHECK (37h.0) ← 0
- CORR (37h.2) ← 0
- DRQ(37h.3) ← 1
- DSC (37h.4) ← 1, if ASDSC (3Dh.4) is high
- DRDY (37h.6) ← 1
- HIRQ (2Eh.3) ← 1, if *A0IEN (18h.0)* is high
- APKTEN ← 0
- Clear BSY (37h.7)

ATAC (2Fh.w6) will not be activated during Automatic Packet Transfers.

When the drive becomes ready after BSY is cleared, the host starts to issue 12-byte ATAPI Command Packet. Reception of the 6th packet word activates the following events.

- *FPKT (30h.r1)* ← 1
- *TENDb (01h.r6)* ← 0
- Pin UINTb activate if *TENDEN (01h.w6)* has been enabled

Writing any value to register TACK (07h) deactivates APKT, TENDb, and corresponding interrupt.

Bit 6: ADCEN - Automatic DRQ Clearing Enable

When this bit is high, DRQ (37h.3) is cleared to 0 and BSY (37h.7) is set to 1 after the end of following transfers:

- Host reads from external RAM
- Host writes to Command Packet FIFO

Bit 5: ASCEN - Automatic Status Completion Enable

When this bit is high, Status Completion is performed after the end of the following transfers:

- Host reads from external RAM
- Host write data to Packet FIFO, if *PFFSCB (01h.w3)* is low

ADCEN (18h.6) should be enabled when ASCEN is enabled to provide clearing of DRQ (37h.3) and setting of BSY (37h.7). If both ADCEN and ASCEN are enabled, the following hardware sequence is executed at the end of one of the above data transfers:

- Set BSY
- DRQ (37h.3) ← 0
- CHECK (37h.0) ← ACHECK (3Eh.0)
- CORR (37h.2) ← ACORR (3Eh.2)
- DRDY (37h.6) ← ADRDY (3Eh.6)
- ATINT (32h) ← 03h
- Clear BSY
- HIRQ (2Eh.3) ← 1
- APKTEN (18h.7) ← 1, if AUTOEN (18h.4) is high
- ASCEN (18h.5) ← 0

After detecting the interrupt, the host reads the ATAPI Status Register and if necessary, the Error Register for the command completion status.

This bit is also cleared by setting *SCT (17h.w0)* high.

Bit 4: AUTOEN - Automatic APKTEN Set After Status Completion Enable

When this bit is high, APKTEN (18h.7) will be set after Automatic Status Completion sequence triggered by either SCT (17h.0) or ASCEN (18h.5).

Bit 3: STWCEN - Set Transfer Word Count Enable

When this bit is high, the value (TWCH/L + 1) × 2 is loaded into ATBLO and ATBHI when ADTT (17h.2) is triggered and PIO (1Fh.2) has been set high. If *ACMEN (9Ch.6)* is not enabled, control bit *STWCEN* should not be set for Multiple Block Transfer. Instead, ATBHI/LO should be set by firmware to: (MBC4-0 + 1) × (TWCH/L + 1) × 2.

Bit 2: AUCRCEN - Automatic Ultra DMA CRC Error Logic Enable

If *AUCRCEN (18h.2)* is set high, the automatic status complete logic would be stopped if *UCRCOKB (30h.r3)* is high. If no CRC error has occurred in last Ultra DMA burst, status complete sequence would be automatically executed. This bit should be set high only if *ASCEN (18h.5)* is set high as well. This bit is automatically clear when: (1) automatic status complete sequence is triggered or (2) *SCT (17h.w0)* is set high.

Bit 1: ABYEN - Automatic BSY Set Enable

When this bit is high, the following sequence is executed when Disk Seek Complete is triggered by *DSCT (17h.w5)*:

- Set BSY
- DSC (37h.4) ← 1
- Clear BSY
- DSCT ← 0

Bit 0: A0IEN - A0h Command Interrupt Enable

If this bit is high and *APKTEN (18h.7)* has been enabled, *HIRQ (2Eh.3)* becomes active-high after an opcode A0h is issued to ATA Command Register.

CCTL0 - Clock Control Register 0 - (write 19h)

This register is 0 after chip reset.

Bit 7: CKSTP - Clock Stop

Setting his bit high stops the internal clock. CKSTP is de-activated by the following events:

- Master reset or firmware reset
- Command write from the host while the drive is selected
- Host issues Diagnostic Command, regardless of drive selection
- Host issues command to shadow drive if SHDRV (3Fh.6) is enabled
- Host set bit SRST in ATAPI Device Control Register high, regardless of drive selection

Bit 6-4: reserved

Bit 3-0: CKS[3:0] - Clock Skew Control

CKS3-0 are used to control the duty cycle of the internal clock. The low period of cycle increases as the skew value increments.

CCTL1 - Clock Control Register 1 - (write 1Ah)

This register is 0 after chip reset.

Bit 7,6: obsolete

Bit 5: XININV - Inverted XIN as System Clock

When this bit is high, the internal system clock is inverted from crystal input.

Bit 4: PSKEN - Programmable System Clock Enable

When this bit is high, the frequency of internal system clock is controlled by register *PSKCTL (59h).*

Bit 3,2: CLK[1:0] - obsolete

Bit 1: Reserved

Bit 0: XTALD2 - Crystal Divided by 2

The internal clock frequency is half of crystal frequency if this bit is high.

VER - Version Register - (read 1Ah)

This register is used to hold the version number.

DSPSL - DSP Selection Register - (write 1Bh)

Bit 7: C2ML - C2 MSB to LSB

When this bit is high, the sequence of erasures via *pin C2PO/SDATA2* is from MSB to LSB.

Bit 6: S16O - Select 16 Offset

The incoming serial data is latched one clock after *pin LRCK* changes if this bit is high.

Bit 5: LCHP - Left Channel Polarity

The incoming serial data is latched as left channel when *pin LRCK* is high if this bit is high.

Bit 4: SFT8 - Shift 8 Clocks

The incoming serial data is latched by delay 8 clocks if this bit is high.

Bit 3: D2EN - SDATA2 Enable

Setting this bit high configures *pin C2PO/SDATA2* as second serial data input.

Bit 2: SEL16 - Select 16 Bits Per Channel

The incoming serial data is latched 16 times per channel if this bit is high.

Bit 1: DIR - Data Direction

Setting this bit high selects the direction of data from *pin SDATA* from MSB to LSB.

Bit 0: EDGE - Latching Edge Select

Setting this bit high selects the rising edge of BCK for latching data from *pin SDATA* .

C2BEB - C2 Block Error Byte - (read 1Bh)

The Block Error Byte is the OR of all the C2 Error Flag bytes.

RACL, RACH, and RACU - RAM Address Counter - (write 1Ch, 1Dh, 2Dh)

These three registers are used to set linear address of the external RAM. Before accessing registers RAMRD/RAMWR or triggering linear-address transfer, microprocessor should set these registers. The microprocessor should write the RAM starting address into the counter while busy flag *UTBY (1Fh.r7)* is low. Then this counter increases automatically each time when a byte is read or written.

RAMWR - RAM Write Register - (write 1Eh)

To gain access to external RAM, the microprocessor should first wait for flag *UTBY (1Fh.r7)* to become low, then set the address through *RACLU/H/L(2Dh/1Dh/1Ch)*.

Writing data into register RAMWR triggers the following sequence:

- Data is transferred from the microprocessor to register RAMWR.
- Data is transferred from RAMWR to the RAM located by the address counter.
- Increments RACL, RACH, and RACU increments by one
- Clear flag UTBY

RAMRD - RAM Read Register - (read 1Eh)

To gain access to external RAM, the microprocessor should first wait for flag *UTBY (1Fh.r7)* to become low, then set the address through *RACLU/H/L (2Dh/1Dh/1Ch)*.

Writing data into register RAMRD triggers the following sequence:

- Data previously stored in RAMRD is transferred to the microprocessor.
- RAM data located by the address counter is transferred to the RAMRD register.
- Increments RACL, RACH, and RACU increments by one
- Clear flag UTBY

Note that the first data read from RAMRD is invalid.

HICTL0 - Host Interface Control Register - (write 1Fh)

Bit 7-6: reserved

Bit 5: H16S - (obsolete)

No matter what value is set, the data transfer between host and decoder is using 16-bit protocol.

Bit 4: LAEN - Latch Enable

If this bit is high, host address and chip-select signals will be latched when pins nHRD or nHWR change from high to low.

Bit 3: MDMA - Multi-word DMA mode

Setting this bit to high enables multi-word DMA mode if *PIO (1Fh.2)* is low.

Bit 2: PIO - PIO/DMA mode select

Setting this bit high causes data transfer to/from host using PIO mode. This bit is also controlled by bit-0 of ATFEA (1F1h/171h) if *ASMDA (5Bh.7)* is high.

Bit 1: DINB - Data-In Transfer Enable

Setting this bit low select data-in transfer. Otherwise, the data-out transfer is enabled.

Bit 0: UDMA - Ultra DMA Enable

Setting this bit high selects data transfer protocol as Ultra DMA. The bandwidth of Ultra DMA depends on the system frequency and the setting of *UDT1-0 (8Ah.5-4)*.

	HICTL0 (1Fh,w)	
	data-in	data-out
PIO mode	xxxx x10xb	xxxx x11xb
MDMA mode	x8h	xAh
UDMA mode	x9h	xBh

STAT5 - Status Register 5 - (read 1Fh)

Bit 7: UTBY - Microprocessor to RAM Transfer Busy

When the microprocessor-to-RAM transfer is not complete, this bit is high.

Bit 6-4: Reserved

Bit 3: MDMA - Multi-word DMA mode

Bit 2: PIO - PIO/DMA mode select

Bit 1: DINB - Data-In Transfer Enable

Bit 0: UDMA - Ultra DMA Enable

HICTL1 - Host Interface Control Register - (write/read 20h)

The value in this register is 26h after chip reset.

Bit 7 : reserved

Bit 6: PDIAGEN - Pin NPDIAG Enable

Setting this bit high causes pin NPDIAG to the active-low state. PDIAGEN is automatically de-activated, causing pin NPDIAG to be high-impedance, by the following events:

- Reception of Execute Drive Diagnostics Command (ATA opcode 90h)
- Reception of ATA Soft Reset (SRST)
- Master reset

Bit 5: DASPEN - Pin NDASP Enable

Setting this bit high activates pin NDASP. DASPEN is automatically de-activated, causing pin NDASP to be high-impedance, by the following events:

- Reception of Execute Drive Diagnostics Command (ATA opcode 90h)
- Reception of ATA Soft Reset (SRST)
- Master reset

This bit is also controlled by DASPS2 (3Fh.2), DASPS1 (3Fh.1) and DASPSS (3Fh.0).

Bit 4: CLRBSY - Clear BSY

Setting this bit high causes the flag BSY in the ATAPI Status Register to become low if *APKT (30h.r0)* is not high. This bit is self-clear after the BSY is clear.

Bit 3: SETBSY - Set BSY

Setting this bit high causes the flag BSY in the ATAPI Status Register to become high if *APKT (30h.r0)* is not high. This bit is self-clear after the BSY is set.

Bit 2: SCoD - Select Command-Packet-FIFO or Data

The data received from ATAPI Data port is stored in Packet FIFO if this bit is high. This bit is also controlled by *ADTT (17h.w2)* and *APKTEN (18h.7)*.

Bit 1: RDYEN - Pin IORDY Enable

Setting this bit high enables IORDY (pin 49) to work with HRDb (pin 50).

Bit 0: IO16EN - Pin IOCS16b Enable

Setting this bit high allows pin IOCS16b to become active-low when 16-bit data access is in use. This bit should be enabled in normal operation.

SICTL0 - Subcode Interface Control Register 0- (read/write 21h)

Bit 7-6: Reserved

Bit 5: ASCEND - Alternative Subcode End Timing

If this bit is high, the timing of subcode end interrupt is delayed to end of subcode sync. Otherwise, the subcode end interrupt is generated at start of subcode sync. This bit is 0 after reset.

Bit 4: QSIGEN - Signature On QCRCOK Enable

If this bit is high, the signature 0xFFh is written to DRAM with block offset 9E0h if CRC checking of Q-code is erroneous. This bit is 0 after reset.

Bit 3: PQENB - P-data or Q-data Enable

Bits 7 and 6 of subcode data are written to the external RAM if this bit is low.

Bit 2-0: SUBCS[2:0] - Subcode Clock Select

If *SBCK (88h.3)* is low and *SCTC (5Ah.w)* is zero, these bits are used to select subcode clock rate.

SCIACK - Subcode Interrupt Acknowledge - (write 22h)

Writing any value to this register de-activates *SCIb (01h.r0)* if *SCIEN (2CH.w4)* is enabled.

SUBSTA - Subcode Status Register - (read 22h)

When *SCIb (01h.r0)* is activated, the microprocessor can read this register to determine the reason of interrupt. These register is clear to 0 by reading *SUBSTA (22h.r).*

Bits 7-5: reserved

Bit 4: QCRCOK - Q-channel CRC OK flag

If Q-channel extraction is enabled, this bit reflects the status of CRC checking of Q-channel information.

Bit 3: reserved

Bit 2: MSS - Missing Subcode Sync

A missing-subcode-sync sets MSS high and negates *SCIb (01h.r0).* A microprocessor interrupt is activated also if *SCIEN (2Ch.w4)* is enabled.

Bit 1: NESBK - Normal End of Subcode Block

A normal-subcode-block-end sets NESBK high and negates *SCIb (01h.r0).* A microprocessor interrupt is activated also if *SCIEN (2Ch.w4)* is enabled.

Bit 0: ISS - Illegal Subcode Sync

An illegal-subcode-sync sets ISS high and negates *SCIb (01h.r0).* A microprocessor interrupt is activated also if *SCIEN (2Ch.w4)* is enabled.

TBH/L - Transfer Block Register - (read/write 25h/24h)

If *LATXF (03h.7)* is low, *TBH/L* form a 9-bit counter that is used to specify the first RAM block to be transferred, while registers *TACH/L (05h/04h,w)* specify the starting address relative to the beginning of this RAM block. The block-offset transfer is carried within a ***transfer ring*** that is controlled by *DTRCH/L (53h/52h)* and *DTRBH/L (51h/50h)*. The buffer ring and transfer ring are usually defined in the same range.

Note that *TBH/L (25h/24h)* do not increment automatically at the end of each transfer unless:

- *DINB (1Fh.1)* is low (data-in transfer is enabled)
- *LATXF (03h.7)* is low (block-offset transfer is used)

If *ACMEN (9Ch.6)* is high, *TCC (9Dh)* minus ***N*** and *TBH/L (25h/24h)* plus ***N*** right after *SKIPC (9Eh)* is set ***N***.

If *BICEN (9Ah.7)* is high and *BCFSEL (9Ah.5)* is low, the DSP buffering stop when buffering block (internal) reach *TBK (9Bh,w)*.

SCBH/L - Subcode Block Register - (read/write 27h/26h)

SCBH/L (27h/26h) form a 9-bit counter that contains the block number of the latest available subcode data that can be read by the host. The number in *SCBH/L (27h/26h)* plus 1 points to the RAM block that is buffering incoming subcode. The number in *SCBH/L (27h/26h)* increments at the end of subcode block buffering. If *SDBS (88h.4)* is high, the buffering of subcode is controlled by *DDBH/L (29h/28h)* rather than *SCBH/L (27h/26h)*.

DDBH/L - Decoded Data Block Register - (read/write 29h/28h)

DDBH/L(29h/28h) form a 9-bit counter that contains the number of the latest available decoded data block after decoder interrupt occurs. CD-ROM sector data buffering is a block-based ring operation.

In *Real-Time-Correction (RTC)* mode, i.e., *BICEN (9Ah.7)* is low, if the number in *DDBH/L (29h/28h)* is *N - 1*, then the current sector is buffered into block with number *N*. The *DDBH/L (29h/28h)* increments at each sync. When the decoded-block-number equals the value in *WBRCH/L (57h/56h)*, the sector is buffered into the block with number specified by *WBRBH/L (55h/54h)*.

In *Buffer-Independent-Correction (BIC)* mode, i.e., *BICEN (9Ah.7)* is low, *DDBH/L (29h/28h)* increments at the end of EDC-checking if there is no *STAERR (80h.r6)* or *HCEI (80h.r0)* error.

RAMCF - RAM Configuration Register - (read/write 2Ah)

This register is 0 after chip reset.

Bit 7: RFTYP - Refresh Type

The refresh mode of DRAM is CAS-before-RAS if this bit is high. The refresh mode of DRAM is RAS-only if this bit is low.

Bit 6: RFTRG - RAM Filling Trigger

Setting this bit high triggers the DRAM filling. All locations in the external RAM will be filled with the value in register *RAMWR (1Eh,w).* The value (ex:00h) should be written to registers RACL, RACU, and RACH before triggering RFTRG. Flag *RFC (2Ah.r5)* will change from 0 to 1 when all RAM locations have been filled. After RAM Filling has completed, the microprocessor should clear RFTRG to 0.

Bit 5: RFC - RAM Fill Completion Flag (read only)

This flag will change from 0 to 1 when all RAM locations have been filled with the value in register *RAMWR (1Eh,w).* This flag is clear when RFTRG is disabled.

Bit 5: Reserved (write only)

Bit 4: SWAP - Host High-Low Swap

Setting this bit high causes the host access of high/low byte to be swapped.

Bit 3: TWES - Two WE/CAS Select

If this bit is low, pin CASH/nRWEH is used as Column Address Strobe for high byte. If this bit is high, pin CASH/nRWEH is used as Write Enable Strobe for high byte..

Bit 2-0: RTC[2:0] - External RAM Type Configuration Bits

The external RAM should be appropriately configured by these three bits according to its specification. RTC[2:0] are de-activated by master reset, but are not changed by firmware reset.

RTC[2:0]	RAM Configuration
0,1, 4, 7	Reserved
2	256K x 4-bit x 2, 256K x 8-bit x 1, 128K x 8-bit x 1, 8-Row 9-Column
3	128K x 8-bit x 1, 9-Row 8-Column
4	64K x 16-bit x 1, (8-row 8-Column) 128K x 16-bit x 1 (9-Row 8-Column) 128K x 8-bit x 2 (9-Row 8-Column)
5	256K x 16-bit x 1 128K x 16-bit x 1 (8-Row 9-Column) 128K x 8-bit x 2, (8-Row 9-Column)

MEMCF - Memory Layout Configuration Register - (write 2Bh)

Bits 7-6: Reserved

Bits 5-4: DBAF[1:0] – Obsolete

These two bits must be set 0.

Bit 3: DFRST - Data FIFO Reset

Setting this bit high resets Data FIFO. This bit is not self-clear.

Bit 2: FRDY - Fast Pin IORDY Enable

Setting this bit high accelerates the de-assertion of *pin IORDY* without referring *pin nHRD*.

Bit 1-0: RLC[1:0] - External RAM Layout Configuration Bits

The memory layout configuration should be set as shown in the following table:

RLC[1:0]	Block Size
0,1	--
2	C00h
3	A00h

The block size should be set as C00h if *C2WEN (10h.w2)* is enabled.

SICTL1 - Subcode Interface Control Register 1 - (write 2Ch)

Bit 7: SBXCK - Subcode External Clock

The external clock from *pin EXCK* is used by the subcode logic if this bit is high.

Bit 6: SCEN - Subcode Enable

Setting this bit high enables the subcode logic.

Bit 5: CD2SC - Clock Divided By 2 For Subcode Logic

The subcode clock is divided by two if this bit is high.

Bit 4: SCIEN - Subcode Interrupt Enable

Setting this bit high enables subcode interrupts.

Bit 3: EXINV - External Clock Invert Select

If *EXOP (2Ch.w2)* is high, setting this bit high selects an inverted clock output at *pin EXCK*.

Bit 2: EXOP - Pin EXCK Operation

Setting this bit high sets *pin EXCK* as an output.

Bit 1-0: SCF[1:0] - Subcode Format Select

SCF[1:0]	Subcode Format
0	SMD0 (Philips)
1	SMD1 (EIAJ-1)
2	SMD2 (EIAJ-2)
3	Reserved

RASTA - DRAM Address Status Register - (read 2Dh)

Pin RA7-0 are input with weak pull-up during master reset or when *RTC (2Ah.2-0)* is 000b. RA7-4 are used as power-on setting and RA3-0 can be used as general input when *RTC (2Ah.2-0)* is 000b. The status of RA7-0 can be read from *RASTA (2Dh,r)*.

MISC0 - Miscellaneous Control Register 0 - (write 2Eh)

Bit 7: HIIEN - Host Interface Interrupt Enable

Setting this bit high enables the microprocessor interrupt of the host interface. Host interface interrupt occurs at the following conditions:

- SRST (Device Control Register) is written as 1 after 0 to either master or slave drive.
- Execute Drive Diagnostics Command is written to either master or slave drive.
- Any opcode is written to the ATAPI Command Register while the drive is selected except: (1) command opcode is 08h, (2) command opcode is A0h and *APKTEN (18h.7)* is high.

IDE interface interrupt is cleared by the following:

- Master reset
- Reading register 37h
- Writing 1 to *CLRBSY (20h.4)*

Bit 6: Reserved

Bit 5: DRVEb - Drive Selection Enable

Setting this bit low enables selection of the drive if bit DRV in ATAPI Drive Select Register matches the setting of *MDRV (2Eh.4)*.

Bit 4: MDRV - Master Drive

Setting this bit high sets the drive to be selected when bit DRV in the ATAPI Drive Select Register is set to 0 (Master Drive).

Bit 3 : HIRQ - Host Interrupt Request

Set this bit high asserts interrupt at pin HIRQ if the drive is selected and nIEN is enabled in the ATAPI Device Control Register. HIRQ is also automatically set by the following:

- Automatic Packet Transfer sequence, enabled by *APKTEN (18h.7)*
- Automatic Status Completion sequence, enabled by *SCT (17h.w0)* or *ASCEN (18h.5)*

HIRQ is automatically de-activated by the following:

- Master reset
- Set bit SRST in the ATAPI Device Control Register high
- Host issue ATA command while the drive is selected
- Host read ATAPI Status Register while the drive is selected

Bit 2: SHIEN - Shadow Command Interrupt Enable

Setting this bit high enables the microprocessor interrupt for the shadow command. Signal *UINTb* becomes low-active when *SHDC (2Fh.r5)* becomes high-active if this bit is enabled.

Bit 1, 0: Reserved

MISS0 - Miscellaneous Status Register 0 - (read 2Eh)

Bit 5: SRUb - Status Register Updated Flag

This bit becomes high when the ATAPI Status Register is updated by the following:

- Microprocessor writes to 37h
- Microprocessor triggers *DSCT (17h.w5)*
- Microprocessor triggers *SCT (17h.w0)*
- Automatic Status Completion occurs if *ASCEN (18h.5)* is enabled
- Reception of A0h command if *APKTEN (18h.7)* is enabled
- Master reset

Bit 4: MDRVF - Master Drive Flag

This bit is high if the drive is configured as Master. This bit is low if the drive is configured as Slave.

Bit 3: HINTF - Host Interrupt Flag

This bit reflects the status of the source of *pin HIRQ* .

Bit 2: nIEN - Bit nIEN in Device Control Register

This bit reflects the value of bit nIEN in ATAPI Device Control Register.

Bit 1: NPDIAG - Pin NPDIAG Flag

This bit reflects the status of *pin NPDIAG*.

Bit 0: NDASP - Pin NDASP Flag

This bit reflects the status of *pin NDASP*.

MISC1 - Miscellaneous Control Register 1 - (write 2Fh)

This register is 0 after chip reset.

Bit 7: ARRC - ATAPI Register Read Control

When this bit is high, the ATAPI registers can be read regardless of the value of BSY if the drive is selected.

Bit 6: SARRC - Shadow Drive ATAPI Register Read Control

When this bit is high, the Shadow ATAPI registers can be read regardless of the value of BSY if the shadow drive is selected.

Bit 5-4: HRSTS[1:0] - obsolete

Bit 3: ARSTEN - ARST Enable

When *ARSTEN* is high, internal signal ARSTB becomes active-low if host writes an DEVICE RESET Command (opcode 08h) and reset the chip.

Bit 2: ARSTS - ARSTb timing select

ARSTEN	ARSTS	type	function of ARSTB	remark
1	0	OD	ARSTb (reset-mode)	
1	1	OD	ARSTb (interrupt-mode)	

In interrupt-mode, writing any value to register *ARSTACK (30h,w)* de-activates ARSTB. In reset-mode, ARSTB automatically de-activates itself after 256 system clocks.

Bit 1: ARSTIEN - ATAPI Soft Reset Interrupt Enable

When this bit is high, *UINTb* becomes active-low whenever host writes an DEVICE RESET Command (opcode is 08h).

Bit 0: ARWC - ATAPI Register Write Control

Host writes to ATAPI registers (except Device Control Register) will not take effect when ARWC and BSY are high, if BSY is not set by the following commands:

- Opcode 90h is written to ATA Command Register while the drive is selected.
- Opcode 90h is written to ATA Command Register while the shadow drive is selected if *SHDRV (3Fh.6)* if high.

MISS1 - Miscellaneous Status Register 0 - (read 2Fh)

Bit 7: SRST - Soft Reset Flag

This bit becomes high when host writes 1 to bit SRST in the ATAPI Device Control Register if either master or slave drive is selected. When SRST becomes high, the following events will be executed:

- BSY (37h.7) ← 1
- Initialize ATAPI signature
- *PDIAGEN (20h.w6)* ← 0 and disables *pin NPDIAG (43)* to high-impedance state
- Disable *pin NDASP (37)* to high-impedance state if *DASPSS (3Fh.0)* is low. Negates *pin NDASP* (37) if *DASPSS (3Fh.0)* is high.
- *CKSTP (19h.7)* ← 0
- Activates host interrupt to the microprocessor if *HIIEN (2Eh.w7)* is high.
- *HIRQ (2Eh.w3)* ← 0

Host interrupt is cleared by read register ATCMD (37h) or write *CLRBSY (20h.4)*. SRST is de-activated by read register *MISS1 (2Fh,r)* after SRST is set to low by host.

Bit 6: ATAC - ATAPI Command

If the drive is selected, this bit becomes high when any command is written to the ATAPI Command register except the following opcode are received.

- opcode is 90h
- opcode is 08h and either *ARST1 (2Fh.w3)* or *ARSTIEN (2Fh.w1)* is enabled
- opcode is A0h and *APKTEN (18h.w7)* is high

ATAC is de-activated by the following:

- Master reset
- Reading register ATCMD (37h)
- Writing 1 to *CLRBSY (20h.4)*

Bit 5: DIAG - Execute Drive Diagnostics Command

This bit becomes high if Execute Drive Diagnostics Command (opcode 90h) has been written to either master or slave drive. Meanwhile, the following events will be executed:

- BSY(37h.7) ← 1
- *PDIAGEN (20h.w6)* ← 0 and disables pin NPDIAG to high-impedance state
- *CKSTP (19h.7)* ← 0
- ATAPI Error Register ← 01h
- ATAPI Feature Register ← 00h
- ATAPI Interrupt Reason Register ← 01h
- ATAPI SAM Tag Byte ← 01h
- ATAPI Byte Counter Register Low/High ← 00h
- ATAPI Drive Select Register ← 00h
- Clear ATAPI Status Register except bit BSY and SERVICE
- Activates host interrupt to the microprocessor if *HIIEN (2Eh.w7)* is enabled

Bit 4: SHDC - Shadow Command Flag

This bit becomes high when the host writes a command to a non-existent slave drive. Meanwhile, *Decoder interrupt* becomes low-active if *SHIEN (2Eh.w2)* is enabled. ATAC is de-activated by the following:

- Master reset
- Reading register ATCMD (37h)
- Writing 1 to *CLRBSY (20h.4)*

Bit 3: ARST - ATAPI Soft Reset Flag

This bit becomes high when DEVICE RESET Command (opcode 08h) is written to either master or slave drive. ARST is de-activated by writing any value to register *ARSTACK (30h,w).*

Bit 2: RST - Reset Flag

This bit is high when the chip is currently being reset by chip reset, host reset, or firmware reset.

Bit 1: FRST - Firmware Reset Flag

This bit is high if the current or most recent reset was firmware reset. The first read of register *MISS1 (2Fh,r)* following the end of the firmware reset clears this flag to 0.

Bit 0: MRST - Master reset Flag

This bit is high if the current or most recent reset was activated by master reset. The BSY flag is set whenever master reset is activated. The first read of register *MISS1 (2Fh,r)* following the end of the master reset clears this flag to 0.

ARSTACK - ATAPI Soft Reset Acknowledge (write 30h)

Writing any value to this register triggers the following events:

- Clears flag *ARST (2Fh.r3)*
- Deactivates ARSTb signal if *ARSTEN (2Fh.w3)* and *ARSTS(2F.w2)* are both high
- Deactivates pin UINTb if *ARSTIEN (2Fh.w1)* is enabled

MISS2 - Miscellaneous Status Register 0 (read 30h)

Bit 7: SRSTD - Soft Reset with DRQ

This bit becomes high if host activates SRST in the ATAPI Device Control Register while DRQ is high and the drive is selected. This bit is updated at rising edge of SRST.

Bit 6: CMDC - Command Conflict

This bit becomes high if one of the following events occurs while BSY is high:

- Host writes any opcode to ATAPI Command Register while drive is selected.
- Host writes any opcode to ATAPI Command Register while shadow drive is selected and *SHDRV (3Fh.6)* is enabled.
- Host writes opcode 90h (Execute Drive Diagnostics) to ATAPI Command Register.

CMDC is updated each time the host writes the ATAPI Command Register.

Bit 5: TDIR - Data Transfer Direction

TENDb (01h.r6)	TDIR (30h.r5)	FPKT (30h.1)	Transfer End Reason	Acknowledge register	Acknowledge Result
0	1	0	data-in transfer	DHTACK (0Eh)	TDIR is clear to 0
0	1	x	data-out transfer	TACK (07h)	TDIR is celar to 0 and FPKT is unchanged
0	0	x	A0 command packet transfer	TACK (07h)	

This flag is cleared by writing *DHTACK (0Eh)* or writing *TACK (07h)*.

Bit 4: MBTI - Obsolete

Bit 3: UCRCOKB - Ultra DMA CRCOK/RAM Parity Interrupt Flag

This bit becomes high if an Ultra DMA CRC error is detected at the end of Ultra DMA burst. This flag is clear to low by reading *MISS2 (30h.r)*.

Bit 2: CRST - Chip Reset Flag

This bit is set high by chip reset. The first read of register *MISS2 (30h,r)* following the end of the chip reset clears this flag to 0.

Bit 1: FPKT -Full Packet Flag

This bit becomes high if the host has written the number of data bytes indicated in register ATBLO (less than 12 bytes), or the host has written a 12-byte command packet. If CoD (32h.0) is low when DRQ (37h.3) change from 0 to 1, the count in ATBLO is latched as a threshold value for FPKT logic. If CoD is high when DRQ (37h.3) change from 0 to 1, the threshold value of FPKT logic is set as 12. Whenever the number of bytes in the Packet FIFO equals the threshold value, flag FPKT becomes high. To receive data from host using Packet FIFO, CoD (32h.0) and ATBLO (32h) should be updated at rising edge of DRQ.

Bit 0: APKT - Automatic Packet Transfer Flag

This bit is set to 1 when host writes opcode A0h to ATA Command Register if drive is selected and *APKTEN (18h.7)* has been enabled. When this flag is high, BSY is controlled by the Automatic Packet Transfer logic. Hence, setting of *CLRBSY (20h.4)* and *SETBSY (20h.4)* is of no effect. APKT is de-activated by writing any value to register *TACK (07h,w)*. APKT is de-activated by master reset but is not changed by firmware reset.

ATERR - ATAPI Error Register (write 31h/read 39h)

This register is set as 01h by the following events:

- Master reset
- SRST
- Execute Drive Diagnostics Command
- Triggering *SIGT (17h.w4)*

ATFEA - ATAPI Feature Register (read 31h)

This register is de-activated by the following events:

- Master reset
- SRST
- Execute Drive Diagnostics Command
- Triggering *SIGT (17h.w4)*

ATINT - ATAPI Interrupt Reason Register (read/write 32h)

This register is set as 01h by the following events:

- Master reset
- SRST
- Execute Drive Diagnostics Command
- Triggering *SIGT (17h.w4)*

ATSPA - ATAPI SAM Tag Bytes Register (read/write 33h)

This register is set as 01h by the following events:

- Master reset
- SRST
- Execute Drive Diagnostics Command
- Triggering *SIGT (17h.w4)*

ATBLO - ATAPI Byte Count Low (read/write 34h)

This register is set as 14h by chip reset, host reset, SRST or triggering *SIGT (17h.w4)*. This register is set as 00h by Execute Drive Diagnostics Command.

ATBHI - ATAPI Byte Count High (read/write 35h)

This register is set as EBh by chip reset, host reset, SRST or triggering *SIGT (17h.w4)*. This register is set as 00h by Execute Drive Diagnostics Command.

ATDRS - ATAPI Drive Select (read/write 36h)

This register is set as 00h by the following:

- Master reset
- SRST
- Execute Drive Diagnostics Command

Note that this register is not changed by triggering *SIGT (17h.w4)*.

ATSTA - ATAPI Status Register (write 37h/read 38h)

This register is set as x0000000b by chip reset, host reset. This register is set as x00x0000b by SRST, Execute Drive Diagnostics Command, or triggering *SIGT (17h.w4)*.Note that BSY is not changed by writing register ATSTA (37h).

ATCMD - ATAPI Command Register (read 37h)

This register is used to latched the command opcode written from host without default value.

ASSTA - ATAPI Shadow Status Register - (write 38h)

Bit 0: SCHECK - Shadow Check Bit

If configured as a Master drive, the firmware should set SCHECK following each host write to ATCMD to comply with ATAPI specification. Bit-7 of Shadow Status Register is the same as BSY of Status Register. Bit 6-1 of Shadow Status Register are all 0s. SCHECK is de-activated by chip reset, host reset, or host writes to Command Register regardless of which drive is selected.

ASERR - ATAPI Shadow Error Register - (write 39h)

Bit 2: SABRT - Shadow ABRT Bit

The microprocessor should set SABRT following each host write to ATCMD to comply with ATAPI specification if configured as a master drive. The other bits of Shadow Error Register are all 0s..

LDDBL/LDDBH - Latched Decoded Data Block Register - (read 3Ah/3Bh)

The decoded data block number in DDBH/L is latched into LDDBH/L at the end of EDC check. This number is available to the end of next EDC check. The LDDBH/L should not be used if *BICEN (9Ah.7)* is enabled.

APKSTA - Status Register for Automatic Packet Transfer - (write 3Dh)

Bit 4: ADSC - Disk Seek Complete for Automatic Packet Transfer

The value of ADSC is the value of bit DSC in ATAPI Status Register during Automatic Packet Command Transfers.

ASCSTA - Status Register for Automatic Status Completion - (write 3Eh)

Bit 6: ADRDY - Drive Ready for Automatic Status Completion

The value of ADRDY is the value of bit DRDY in the ATAPI Status Register during Automatic Status Completion.

Bit 2: ACORR - Correctable Error for Automatic Status Completion

The value of ACORR is the value of bit CORR in the ATAPI Status Register during Automatic Status Completion. CORR is de-activated by chip reset, host reset, or firmware reset.

Bit 0: ACHECK - Check for Automatic Status Completion

The value of ACHECK is the value of bit CHECK in the ATAPI Status Register during Automatic Status Completion. CHECK is de-activated by chip reset, host reset, or firmware reset.

SHDCTL - Shadow Drive Control Register (read/write 3Fh)

Bit 7, 4, 3: Reserved

Bit 6: SHDRV - Shadow Drive Enable

If *MDRV (2Fh.4)* is high, the bit reflects the level on *pin NDASP* until *SHDRVL (3Fh.5)* is set high. If this bit is high, Shadow Register support for the non-existent Slave Drive is enabled..

Bit 5: SHDRVL - Shadow Drive Enable Latch

Microprocessor should set this bit high at least 450 milliseconds after master reset to latch the setting of *SHDRV (3Fh.6)* from *pin NDASP* if configured as a master drive. This bit is 0 after chip reset and host reset.

Bit 2: DASPS2 - DASP Select 2

Setting this bit high enables *DASPEN (20h.w5)* during host reset. DASPS2 should normally be 0 to comply with ATAPI specification. This bit is 0 after chip reset.

Bit 1: DASPS1 - DASP Select 1

Setting this bit high enables *DASPEN (20h.w5)* following end of host reset. This bit is 0 after chip reset.

Bit 0: DASPSS - DASP SRST Select

Setting this bit high enables *DASPEN (20h.w5)* following the end of soft reset (SRST). This bit is 0 after chip reset and host reset.

CCSA0 - Configurable Chip Select Base Address Register 0 (read/write 40h)

The content of this register is used as the base address of Decoder Chip Select. The default of this register after hardware reset is 0x40h.

CCSA1 - Configurable Chip Select Base Address Register 1 (read/write 41h)

The content of this register is used as the base address of CCS1. The default of this register after hardware reset is 0x00h.

CCSA2 - Configurable Chip Select Base Address Register 2 (read/write 42h)

The content of this register is used as the base address of CCS2. The default of this register after hardware reset is 0x00h.

GLCTL1 - Global Control Register 1 (read/write 43h)

The default of this register after hardware reset is 0x00h.

Bit 7: RSTO - Pin RSTO output control

The state of *pin nRSTO* is the inverse value of this control bit. This bit is 0 after chip reset.

Bit 4: UP323S - Pin UP323 Selection

UP323S (43h.4)	pin UP32/UP33	internal Decoder Interrupt	Remark
0b	INT0	INT1	(default)
1b	INT1	INT0	

Bit 2: CKOSTP: Pin CKO Output Stop

Setting this bit high immediately puts the output of *Pin CKO* at a steady "high" state. This bit is low after master reset.

Bit 1: ACLKS - ACLK Source Selection

Setting this bit high select pin DXI as ACLK input source. Setting this bit low select pin UXI as ACLK input source. This bit is 0 after chip reset.

Bit 0: DCLKS - DCLK Source Selection

Setting this bit high select pin DXI as DCLK input source. Setting this bit low select pin UXI as DCLK input source. This bit is 0 after chip reset.

LSTA0-3 (read 48h-4Bh) - obsolete

LHD0-3 (read 4Ch-4Fh) - obsolete

Ring Control Registers - (read/write 50h to 57h)

These eight registers add flexibility to the block control of external memory that is controlled by *RTC2-0 (2Ah.2-0)* initially. Once one of these eight registers is set, all eight registers should be set to take full control of block configuration of the external memory. The data-transfer-ring and write-buffer-ring are normally set the same value.

DTRBL/DTRBH - Data Transfer Ring Base Register - (read/write 50h/51h)

Data Transfer Ring Base Register and Data Transfer Ring Ceiling Register treat the external memory as a ring while transferring data to the host. Data Transfer Ring Base Register specifies the base block number of this ring.

DTRCL/DTRCH - Data Transfer Ring Ceiling Register - (read/write 52h/53h)

Data Transfer Ring Base Register and Data Transfer Ring Ceiling Register treat the external memory as a ring while transferring data to the host. Data Transfer Ring Base Register specifies the ceiling block number of this ring. The first block to be transferred is specified by registers *TBH/L (25h/24h)*. The further data transfer after the end of Data Transfer Ceiling block will access data in Data Transfer Base block.

WBRBL/WBRBH - Write Buffer Ring Base Register - (read/write 54h/55h)

Write Buffer Ring Base Register and Write Buffer Ring Ceiling Register treats the external memory as a ring while buffering the serial data from DSP. Write Buffer Ring Base Register specifies the base block number of this ring.

WBRCL/WBRCH - Write Buffer Ring Ceiling Register - (read/write 56h/57h)

Write Buffer Ring Base Register and Write Buffer Ring Ceiling Register treats the external memory as a ring while buffering the serial data from DSP. Write Buffer Ring Base Register specifies the base block number of this ring. The first block to be buffered is specified by registers *DDBH/L (29h/28h)*. Further serial data buffering after the end of Write Buffer Ceiling block will buffer serial data into the Write Buffer Base block.

TCCCTL - TCC Source Control Register (read/write 58h)

This register is 00h after mater reset. This register controls the increment/decrement source of *TCC (9Dh)*.

Bit 7-4: reserved

Bit 3-2: TCCCTL[3:2]

TCCCTL[3:2]	Function	
00h	TCC increment by CBK increment	default
01h	TCC increment by APBK increment	

Bit 1-0: TCCCTL[1:0]

TCCCTL[1:0]	Function	
00h	TCC decrement by TBK increment	default
01h	TCC decrement by APBK increment	

PSKCTL - Programmable System Clock Control Register - (read/write 59h)

This register should be set before the programmable system clock is enabled by setting *PSKEN (1Ah.w4)* high. This register is 0 after master reset.

Bit 7: PSKTEST (write only) - Programmable System Clock Test Enable

This bit is low after master reset and should be set low in normal operation. Setting this bit high is only used for factory test.

Bit 7: LOCKED (read) - Programmable System Clock Locked

This bit is high once the internal system clock is ever on lock with the programmed frequency.

Bit 6: LOCKSEL (write) - Programmable System Clock Lock Select

If this bit is high, the internal system clock will keep the same delay path once the programmed frequency is locked. This function keeps system clock at steady frequency, but the frequency may be affected by temperature. If this bit is low, the internal system clock will be continuously adjusted to fit the programmed frequency according to Crystal input and result in a various frequency.

Bit 6: PSKEXE (read only) - Programmable System Clock Extreme Condition

This bit is low after master reset. The bit is high when the programmable system clock is at its lowest or highest frequency. This indicates that the frequency equation, according to *PSK (59h.5-0)*, may not effective in this case.

Bit 5-0: PSK[5:0] - Programmable System Clock Factor

If *PSKEN (1Ah.w4)* and *PSKSEL (59h.w7)* are high, these six bits are used to controlled the internal system frequency. The equation is:

```
frequency of system clock  = frequency of XIN  × (PSK[5:0] + 2) ÷ 16
```

SCTC - Subcode Timer Control Register - (write 5Ah)

If *SBXCK (2Ch.w7)* and *CD2SC (2Ch.w5)* are both low, the clock used by subcode logic clock is controlled by *SUBCS2-0 (21h.w2-0)* unless any non-zero value is written into this register. The value of this register should be calculated as follows:

```
( N + 2 ) × tc × dsf = 11.3 / 2
```

where ***tc*** is the internal clock period(ex: 50nS for 20MHz crystal),

dsf is the disk speed factor(ex: 4 for 4-fold speed drive).

There is no need to set this register if *SBCK (88h.w3)* is set high.

EFCTL - Enhanced Feature Control Register - (read/write 5Bh)

Bit 7: ASDMA - Automatic Set DMA

If this bit is high, the inverted value of DMA bit of ATFEA (1F1h,w) will be automatically loaded to *PIO (1Fh.2).* This bit is 0 after chip reset, host reset and firmware reset.

Bit 6: obsolete

Bit 5: DSP1STB

Bit 4: reserved

Bit 3: ALECTL - ALE Input Control

If this bit is high, the ALE input is gated with internal chip select signal. If this bit is low, the ALE input latch the Index Register directly.

Bit 2: DSPDW - DSP buffer double words enable

If this bit is high, the DSP buffer is double-word-based; otherwise, it is word-based. This bit is 0 after chip reset, host reset and firmware reset.

Bit 1: DRA - Direct Register Addressing Enable

This bit must be set high.. If this bit is set high, the Direct Register Addressing function is enabled. This bit is 1 after chip reset in normal condition.

Bit 0: Reserved

EFCTL2 - Enhanced Feature Control Register 2- (read/write 5Ch)

Bit 7-4: Reserved

Bit 3: ALE2 - obsolete

Bit 2: SYNCP - Sync Bytes Patch Enable

If this bit is high, the sync bytes of the following sector are patched to the previous sector. This bit must be disabled when reading CD-DA data.

Bit 1: reserved

Bit 0: RMSRI - Remove Frequent SRIb

If *RMSRI (5Ch.0)* is high, flag *SRIb (01h.r5)* is generated only by flags *STAERR (80h.r6), DSFULI (80h.r4), LASTBK (80h.r3), LTTI (80h.r2), TNFI (80h.r1)* or *HCEI (80h.r0).* Setting this bit high can reduce the overhead of microcontroller while the automatic cache management is used. This bit is 0 after chip reset, host reset and firmware reset.

GIOCF - General Purpose I/O Port Configuration Register (read/write 5Dh)

G4CF (5Dh.7-4)	function	nCCS2 active (low) condition	remark
0xxxb	RA8	output is tri-state after master reset and is enabled when RTC (2Ah.2-0) ≠ 000b	default
10xxb	GPIO4	n/a	
1100b	nCCS2	(P2 = CCSA2)	
1101b	nCCS2	(P2 = CCSA2) & (P36 = "L")	
1110b	nCCS2	(P2 = CCSA2) & (P37 = "L")	
1111b	nCCS2	(P2 = CCSA2) & (P36 = "L" or P37 = "L")	

G2CF (5Dh.3)	DAOEN (87h.7)	pin function	Remark
0b	0b	nFCE	(default)
1b	0b	GPIO2	
x	1b	DAOUT	

G3CF (5Dh.2-0)	function	nCCS1 active (low) condition	remark
0xxb	GPIO3	n/a	default
100b	nCCS1	(P2 = CCSA1)	
101b	nCCS1	(P2 = CCSA1) & (P36 = "L")	
110b	nCCS1	(P2 = CCSA1) & (P37 = "L")	
111b	nCCS1	(P2 = CCSA1) & (P36 = "L" or P37 = "L")	

PSKCNT - Programmable System Clock Counter (read/write 5Eh)

This register is used for factory test.

GIOCTL - General I/O Port Control Register - (read/write 5Fh)

This register is 0 after chip reset.

Bit 5: G4OEN - General I/O Port 4 Output Enable

Setting this bit high configure GIO4 as output. Otherwise, it is an input pin.

Bit 5: G3OEN - General I/O Port 3 Output Enable

Setting this bit high configure GIO3 as output. Otherwise, it is an input pin.

Bit 5: G2OEN - General I/O Port 2 Output Enable

Setting this bit high configure GIO2 as output. Otherwise, it is an input pin.

Bit 4: G1OEN - General I/O Port 1 Output Enable

Setting this bit high configure GIO1 as output. Otherwise, it is an input pin.

Bit 3: GIO4 - General Purpose I/O Port 4

If GIO4 is configured as an input pin, the pin state can be read back from this bit. If GIO4 is configured as an output pin, set this bit low drive GIO4 low and set this bit high cause a weak pull-up.

Bit 2: GIO3 - General Purpose I/O Port 3

If GIO3 is configured as an input pin, the pin state can be read back from this bit. If GIO3 is configured as an output pin, set this bit low drive GIO2 low and set this bit high cause a weak pull-up.

Bit 1: GIO2 - General Purpose I/O Port 2

If GIO2 is configured as an input pin, the pin state can be read back from this bit. If GIO2 is configured as an output pin, set this bit low drive GIO2 low and set this bit high cause a weak pull-up.

Bit 0: GIO1 - General Purpose I/O Port 1

If GIO1 is configured as an input pin, the pin state can be read back from this bit. If GIO1 is configured as an output pin, set this bit low drive GIO1 low and set this bit high cause a weak pull-up.

TARCTL - Target Control Register - (write 80h)

This register is used to control the automatic target search and header comparison.

Bit 7: TARGEN - Target Function Enable

Setting this bit high enables target search function but does not enable decoder simultaneously. The operation of target search is triggered by setting *DECEN (0Ah.w7)* high. Then the decoder generates first interrupt after the target sector, specified by *TARGET (84h-86h)*, is found.

Bit 6: DSCEN - Decoding Sector Counting Enable

If *DSCEN (80h.6)* is enabled, flag *DSFULI (80h.r4)* becomes high if *DSCL (81h,r)* is equal to *DSTL (81h,w)* at the end of EDC-checking.

Bit 5: QEN - Q-channel extraction enable

Setting this bit high enables Q-channel extraction logic. This pin should be set high only when *SCEN (2Ch.w6)* is high. Once decoder and Q-channel extraction are both enabled, the extracted Q-channel bytes are written into the DRAM starting from offset 9E0h of each block regardless of what mode of data is set.

Bit 4: QMSF - Q-channel MSF auto-load enable

If Q-channel extraction logic is enabled, setting this bit high enables the MSF bytes of Q-channel to be automatically loaded to *HEAD0-2 (04h-06h,r)*. The register *HEAD3 (07h,r)* hold first byte of *DATA-Q*, (CONTROL and ADR) or 0xFFh if CRC checking of Q-channel is erroneous.

Bit 3: ASTOPB - Automatic Decoder Stop on Error

If this bit is low, decoder would automatically stop on the following conditions:

- *HCEI (80h.r0)* activates if *HCEEN (80h.w0)* is enabled.
- *TNFI (80h.r1)* activates if *TNFEN (80h.w1)* is enabled.
- *LTTI (80h.r2)* activates if *LTTEN (80h.w2)* is enabled.
- *LASTBK (80h.r3)* activates if *BLIMEN (9Ah.5)* is enabled
- *DSFULI (80h.r4)* activates if *DSCEN (80h.w6)* is enabled.
- *STAERR (80h.r6)* activates if any Status Mask Bit is enabled

If this bit is low, the consistency of f/w and h/w should be carefully maintained. If this bit is high, the decoder is controlled by microprocessor. This bit is default low after chip reset.

Bit 2: LTTEN - Larger Than Target Interrupt Enable

Setting this bit high enables *LTTI (80h.r2)* to be reflected on *SRIb (01h.r5)*.

Bit 1: TNFEN - Target Not Found Interrupt Enable

Setting this bit high enables *TNFI (80h.r1)* to be reflected on *SRIb (01h.r5)*.

Bit 0: HCEEN - Header Compare Error Interrupt Enable

Setting this bit high enables *HCEI (80h.r0)* to be reflected on *SRIb (01h.r5)*.

TARSTA - Target Status Register - (read 80h)

This register is 0 after chip reset, host reset, firmware reset and decoder reset. Reading this register deactivates *SRIb (01h.r5)*.

Bit 7: TARGED - Target Is Found

This bit is high after the target is found.

Bit 6: STAERR - Status Error Flag

This bit becomes high if any status bit error, enabled by its corresponding mask bit, occurs at the end of EDC-checking. This flag is deactivated after reading register *TARSTA (80h,r)*.

Bit5: BIN0 - Block Indicator Is Not Zero Flag

If *BIN0M (8Ch.w1)* is high, this bit becomes high if the block indicator in *HEAD3 (07h.7-5)* is not zero. This flag also activates *STAERR (80h.r5)* high.

Bit 4: DSFULI - Decoding Sector Full Interrupt Flag

If *DSCEN (80h.6)* is enabled, this flag becomes high if *DSCL (81h,r)* is equal to *DSTL (81h,w)* at the end of EDC-checking.

Bit 3: LASTBK - Last Decoded Block

If *BLIMEN (9Ah.5)* is high, this bit is set when the last pre-buffered block is decoded. Firmware should disable decoder when detect this flag. The DSP buffering stop when buffer-cache full.

Bit 2: LTTI - Larger Than Target Interrupt Flag

If *LTTEN (80h.w2)* and *TARGEN (80h.w7)* are high, this flag becomes high if the header larger than target when *HEAD0-2 (04h-06h)* are available. This flag is deactivated after reading register *TARSTA (80h,r).*

Bit 1: TNFI - Target Not Founded Interrupt Flag

This bit becomes high if the headers in *HEAD0-2 (04h-06h)* never match the target after ***N*** successive comparisons. Where ***N*** is the search limit number specified by *TSL (83h,w*). If *TNFEN (80h.w1)* is high, *SRIb (01h.r5)* activates when this bit becomes high. If *ASTOPb (80h.w3)* is low, this event also clears *DECEN (0AH.w7)* and stop the decoder automatically. This flag is deactivated after reading register *TARSTA (80h,r).* The microprocessor could read out the header after event occurs to determine the distance from target.

Bit 0: HCEI - Header Compare Error Interrupt Flag

After target is founded, the number in *TARGET (84h-86h)* will automatically increment after *HEAD0-2 (04h-06h)* are available. If the headers of following sector do not match the target, this bit becomes high and activates *SRIb (01h.r5)* if *HCEEN (80h.w0)* is enabled. It also clears *DECEN (0AH.w7)* and stop the decoder automatically if *ASTOPb (80h.w3)* is low. This flag is deactivated after reading register *TARSTA (80h,r).*

DSTL - Decoding Sector Threshold Register - (write 81h)

If *DSCEN (80h.w6)* is enabled, this register specified the threshold number of successive sectors minus one to be decoded after header is targeted. Flag *DSFULI (80h.r4)* becomes high when value in *DSCL (81h,r)* is equal to *DSTL (81h,w)* at the end of EDC-checking. The initial value of *DSTL (81h,w)* is FFh after chip reset, firmware reset and decoder reset. Note that threshold value should not be set as 00h if *DSCEN (80h.w6)* is enabled.

DSTH - Obsolete (write 82h)

DSCL - Decoding Sector Counter - (read 81h)

Once the target header is found, this counter increments when a sector is completely decoded. This counter is incremental-only, and the value follows FFh is 0. If *DSCEN (80h.6)* is high, flag *DSFULI (80h.r4)* becomes high if *DSCL (81h,r)* is equal to *DSTL (81h,w)* at the end of EDC-checking. Meanwhile, the decoder stops if *ASTOPB (80h.w3)* is low. This register is cleared to 00h at the falling edge of *DECEN (0Ah,w7)*. The initial value of DSCL after chip reset, firmware reset and decoder reset is 00h.

DSCH - Obsolete (read 82h)

TSL - Target Search Limit Register - (write 83h)

This register specified the limited number of target search. If ***N*** is the number specified by this register, *TNFI (80h.r1)* becomes high if the headers have not match the target after ***N*** successive sectors. Since this register will not be changed by decoding operation, there is no need to writing it before every decoding operation. The initial value of TSL after chip reset, host reset and firmware reset is FFh.

TSC - Target Search Counter - (read 83h)

After the decoder is enabled, the number of sectors has been searched can be monitored by reading TSC. This register is cleared to 00h at the falling edge of *DECEN (0Ah,w7)*. The initial value of TSC after chip reset, firmware reset and decoder reset is 00h.

TARGET0 - Target Minute Register - (read/write 84h)

TARGET1 - Target Second Register - (read/write 85h)

TARGET2 - Target Frame Register - (read/write 86h)

DACTL - Digital Audio Control Register - (read/write 87h)

This register is 00h after chip reset and host reset.

Bit 7: DAOEN - Digital Output Enable

If this bit is high, the digital audio data output through *pin DAOUT*.

Bit 6: CTLSEL - Control Bit Source Select

If this bit is high, the 4 control bits of Q channel are defined by *QCTL3-0 (87h,3-0)*. Otherwise, these 4 control bits are extracted from external RAM. This bit is normal set low if the Q-channel extraction work properly.

Bit 5-4: ACCU [1:0] - Clock Accuracy

These two bits are used as clock accuracy bits in digital audio output. These two bits are usually set 00b.

Bit 3:0: QCTL [3:0] - Control Bits for Q Channel

If *CTLSEL (87h.6)* is high, these four bits are used as Q channel control bits in digital audio output.

FEACTL - Feature Control Register - (read/write 88h)

This register is 00h after chip reset and host reset.

Bit 7: LECAS - Latch Data with External CAS Signal

If this bit is high, input DRAM data is latched by external CASH/L signal instead of rising edge of internal clock. This function can eliminate the timing difference between DRAM data and its latch signal caused by various internal chip delays, depending on circumstances. This bit should not be used if *EDOEN (88h.1)* is high.

Bit 6: LREF - Long Refresh Cycle

If this bit is high, the tRAS is 2.5 clocks instead 1.5 clocks for refresh cycle.

Bit 5: MRCD - Medium RAS to CAS Delay

The bit controls the timing of tRCD and tRP. If this bit is high the tRAS for RAS-only refresh is 2 clocks and CAS-Before-RAS is not affected (1.5 clocks).

Bit 4: SDBS - Subcode and DSP Block Synchronization

This bit provides block synchronization of CD-DA format data. If this bit is high, the buffering of incoming serial data and subcode to the external RAM will synchronize to the same block defined by *DDBH/L (29h/28h)*.

Bit 3: SBCK - Select BCK as subcode clock

When this bit is high, the *pin BCK* is selected as subcode reference clock instead of system clock. This setting is suitable for drive using CAV subcode.

Bit 2: CAS8B - Eight CAS in One RAS Enable

When this bit is set low, maximum the number of Column Address Strobe is 8 instead of 4 in one DRAM FPM cycle.

Bit 1: FRCDB - Fast RAS to CAS Delay

The bit controls the timing of tRCD and tRP.

Bit 0: EDOEN - EDO DRAM Support Enable

Setting this bit enables EDO DRAM support and the data latch timing of DRAM changes to falling edge instead of rising edge of internal clock. This bit should not be used if *LECAS (88h.7)* is high.

DFFCNTL - Data FIFO Threshold Control Register - (read/write 89h)

Bit 7,6: Reserved

Bit 5-3:`DFFHT[2:0] - Data FIFO High Threshold

When the number of bytes in Data FIFO larger than DFFHT, device stops pre-fetch to prevent FIFO overrun. Since the default setting of *CAS8B (88h.2)* is low, the default value of DFFHT is 001b.

DFFHT[2:0]	Threshold	
000b	28	
001b	24	default
011b	16	

Bit 2-0:`DFFLT[2:0] - Data FIFO Low Threshold

When the number of bytes in Data FIFO less than DFFLT, device de-activates DMARQ to prevent FIFO underrun in traditional DMA mode. When the number of bytes in Data FIFO less than DFFLT, device would stop issuing DSTROBE to prevent FIFO underrun in Ultra DMA data-in mode.

DFFLT[2:0]	Threshold	
000b	4	default
001b	8	
011b	16	

ATCTL - Auxiliary Timing Control Register - (read/write 8Ah)

This register is set 00h after chip reset, host reset and firmware reset.

Bit 7: DXOFF - DX Crystal Loop Off

Setting his bit high can turn off the feedback loop beteween DXI and DXO and save power consumption.

Bit 6: UDTA - Ultra DMA Timing Acceleration

If this bit is high, the internal Ultra DMA base frequency is doubled from the clock sourxe that is selected by *UCLKS (8Ah.3)*.

Bit 5-4: UDT[1:0] - Ultra DMA Timing Control

These two bits define the Ultra DMA Timing Factor, ***udtf***, which control the timing of Ultra DMA transfer.

$Tcyc = (2 + udtf) \times Tudma$

where Tudma is clock period depends on setting of *UDTA (8Ah.6)* and *UCLKS (8Ah.3)*

and Tcyc is Ultra DMA cycle time (from DSTROBE edge to DSTROBE edge)

Device firmware should set ***udtf*** according to the clock source and the assigned Ultra DMA transfer mode after host issues SET FEATURE command.

Bit 3: UCLKS - Ultra DMA Clock Select

If this bit is high, the clock source for UDMA is from *pin ACLK*. If this bit is low, the clock source is system clock.

Bit 2-0: REFT[2:0] - Refresh Timing Control

The frequency of refresh is controlled by *REFT2-0 (8Ah.2-0)* to support long refresh. The value after chip reset is 0. The refresh cycle defaults to be issued once after 256 system clocks.

refresh period = 256×2reft system clock periods

STA0M - Status 0 Mask Register - (write 8Ch)

If any following bit is enabled, the flag *STAERR (80h.r6)* becomes high when the corresponding status bit becomes active.

Bit 7 - CRCOK Mask

Bit 6 - ILSYNC Mask

Bit 5 - NOSYNC Mask

Bit 4 - LBLK Mask

Bit 3 - WSHORT Mask

Bit 2 - SBLK Mask

Bit 1 - BIN0 Mask

Bit 0 - UCEBLK Mask

STA1M - Status 1 Mask Register - (write 8Dh)

If any following bit is enabled, the flag *STAERR (80h.r6)* becomes high when the corresponding status bit becomes active.

Bit 4: HDERA Mask

Bit 0: SHDER Mask

STA2M - Status 2 Mask Register - (write 8Eh)

If any following bit is enabled, the flag *STAERR (80h.r6)* becomes high when the corresponding status bit becomes active.

Bit 2: NOCOR Mask

Bit 1: RFOMR1 Mask

STA3M - Status 3 Mask Register - (write 8Fh)

If any following bit is enabled, the flag *STAERR (80h.r6)* becomes high when the corresponding status bit becomes active.

Bit 5: ECF Mask

Bit 1: C2DF Mask

APCNF - Audio Playback Configuration Register - (read/write 90h)

The default value of this register is 00h after chip reset, host reset and firmware reset.

Bit 7: APEN - Audio Playback Enable

Setting this bit high enables audio playback logic. Once audio playback logic is enabled, the buffered data will be sent out block after block starting from the setting of *APBK (92h/93h)*. The playback stops immediately and keeps "mute" once this bit is set low.

Bit 6: APIEN - Audio Playback Interrupt Enable

Setting this bit high enables audio-playback-interrupt to be reflected on internal signal *UINTb* whenever each block playback is finished. Audio-playback-interrupt flag is reflected on *APIb (01h.r2)* if *APOUT1-0 (90h,1-0)* is not zero.

Bit 5: DEMAND - Demand Mode Enable

Setting this bit high enable the demand mode. In demand mode, *pin ALRCK* is used as Demand input. The ABCK clock is enabled only when Demand is high.

Bit 4: APINS - Audio Reference Input Select

If this bit is set low, signal *ACLK* is used as audio-playback reference clock. If this bit is high, *SCLK* is used as audio-playback reference block.

Bit 3,2: APIN[1:0] - Audio Input Reference Clock Setting

APIN[1]	APIN[0]	Input Reference Clock
0	0	8.4672MHz
0	1	16.9344MHz
1	0	33.8688MHz
1	1	67.7376MHz

The value in these registers should be properly set according to the audio-playback reference clock before enable *APEN (90h.7)*.

Bit 1,0: APOUT[1:0] - Audio Data Output Setting

APOUT[1]	APOUT[0]	Audio Data Output Pin	Pin 6	Pin 13
0	0	No Output	tri-state	tri-state
0	1	nROE/ASD	ABCK	ALRCK

When *APOUT* are set zero, no output is generated from *pin ABCK* and pin *ALRCK* is used as left-right clock output. When *APOUT* are set not zero, flag *APIb (01h.r2)* becomes low whenever one block audio-playback is finished.

APFMT - Audio Playback Format Register - (read/write 91h)

APFMT7-0	Audio Data Format
000xx111h	Toshiba
001xx000h	Sanyo
101xx011h	Sony 48-bit slot
110xx011h	Philip

APFMT4	APFMT3	Functions
0	0	Normal Stereo
0	1	Mono Left
1	0	Mono Right
1	1	Left/Right Swap

APBKL/H - Audio Playback Block Register - (read/write 92h/93h)

The bit-0 of *APBKH (93h)* and bit7-0 of *APBKL (92h)* form a 9-bit counter. The value in this 9-bit counter defines the first block to be playbacked when *APEN (90h.7)* is enabled. The value in these registers is incremented by 1 after one block playback is finished.

93h.Bit-7: test control - should be 0

93h.Bit-6: test control - should be 0

93h.Bit-5: APACENB - Audio Playback Initial Address Counter Latch Enable

If this bit is low, the value of *WAC (08h,09h)* is loaded into internal register *APAC*. The vaule of *APAC* minus 12 is the starting address of audio playback.

93h.Bit-4: test control - should be 0

APWCL/H - Audio Playback Word Count Register - (read/write 94h/95h)

The number in this counter plus one is the word count to be playbacked for each memory block. The default value of these registers is **0497**h after chip reset, host reset and firmware reset. No need to change this value for normal usage.

APVOL - Audio Playback Volume Register - (write 96h)

Bit 7-4: LVOL[3:0] - Left Channel Volume Control

Bit 3:0: RVOL[3:0] - Right Channel Volume Control

LVOL3-0/RVOL3-0	Binary Number	Attenuation (dB)
Fh ~ Ch	FFh	0 (On)
Bh	80h	-6.00
Ah	40h	-12.0
9h	20h	-18.0
8h ~ 5h	10h	-24.0
4h	08h	-30.0
3h	04h	-36.0
2h	02h	-42.1
1h	01h	-48.0
0h	00h	Mute (Off)

APACK - Audio Playback Interrupt Acknowledge - (write 97h)

Writing any value to this register deactivates flag *APIb (01h.r2)* and its corresponding interrupt.

PUCTL - Pull Up Resistor Control Register - (write 98h)

This register is used to control the utilization of two pull-up resistors on IO cells. Default value is 0.

Bit 7-6: HIP[1:0] - Host Interface Pull-up Control

Setting these two bits low control two pull-up resistors of host interface I/O cells respectively. If these two bits are both high, no pull-up resistors exist. Note that DD7 is controlled by *DD7UPB (98h.1)* separately,

Bit 5-4: UIP[1:0] - Microprocessor Interface Pull-up Control

Setting these two bits low control two pull-up resistors of uP interface I/O cells respectively. If these two bits are both high, no pull-up resistors exist.

Bit 3-2: RIP[1:0] - RAM Interface Pull-up Control

Setting these two bits low control two pull-up resistors of RAM interface I/O cells respectively. If these two bits are both high, no pull-up resistors exist.

Bit 1: DD7UPB - DD7 Pull-up Enable

Setting this bit low enable the internal pull-up resister on the *pin DD7*.

Bit 0: APIPB - Audio Playback Interface Pull-up Control

Setting this bit low enable the internal pull-up of the audio-playback output pin, including ALRCK, ABCK and ASD.

SICTL - Sink Current Control Register - (write 99h) - obsolete

BICCTL - Buffer Independent Correction Control Register - (read/write 9Ah)

This register is 0 after chip reset, host reset and firmware reset.

Bit 7: BICEN - Buffer Independent Correction Enable

If this bit is high, the buffer-independent-correction (BIC mode) is enabled. Otherwise, the real-time-correction (RTC mode) is enabled.

Bit 6: ATMSEN - Automatic Mode Switch

If this bit is high, the decoder automatically change from Disk-Monitor Mode to the pre-set Buffer-Mode after the target is found.

Bit 5: BLIMEN - Buffer Limit Enable

If *BLIMEN (9Ah.5)* is high, the buffering of DSP data stops when the condition defined by *BLIMS (9Ah.4)* is met. This function should be enabled if *BICEN (9Ah.7)* is set high.

Bit 4: BLIMS - Buffer Limit Source Select

If *BLIMS (9Ah.4)* is high, the buffering stop when *BUFC (9Bh,r)* reach *BUFLIM (9Bh,w)*. If *BLIMS (9Ah.4)* is low, the buffering stops when buffering block (internal) reach *TBH/L (24h/25h,r)* minus 1.

Bit 3-0: RCLIM[3:0] - Repeat Correction Limit

If *BICEN (9Ah.7)* is high, these four bits specify the maximum number of repeat correction.

BUFLIM - Buffer Limit Register - (write 9Bh)

This register is used as buffer limit when *BLIMS (9Ah.4)* is high. This register can be set the buffer-ring size minus *n*, where *n* is larger than 1. This register is 0 after master reset and firmware reset. In normal operation, this register only needs to be set once after power-on.

BUFC - Buffer Counter - (read 9Bh)

This counter increments when a sector is buffered into external RAM. If *ACMEN (9Ch.6)* is high, *BUFC (9Bh,r)* decrements at the end of each data-in block transfer unless the value is zero. The value follows 0 is 0. The transfer of working area data should be implemented as linear transfer to prevent extra decrement of this counter.

If *ACMEN (9Ch.6)* is high, *BUFC (9Bh,r)* minus ***N*** right after *SKIPC (9Eh)* is set ***N***. This function can be used to implement the cache-partial-hit event.

If both *BLIMEN (9Ah.5)* and *BLIMS (9Ah.4)* is high, the buffering stop when this count reaches *BUFLIM (9Bh,w)*. The value in BUFC (9Bh,r) may exceed *BUFLIM (9Bh,w)* by one.

This counter is synchronized to *TCC (9Dh)* whenever *DECEN (0Ah.w7)* is low.

This counter is 0 after master reset and firmware reset.

ACCTL - Automatic Cache Control Register - (read/write 9Ch)

This register is 0 after chip reset, host reset and firmware reset.

Bit 7: ATTEN - Automatic Transfer Trigger Enable

The control bit *ADTT (17h.w2)* is automatically set high if all the following conditions are met:

- *ATTEN (9Ch.7)* is high
- *TCC (9Dh)* is not zero
- *TTC (9Fh)* is not zero

Bit 6: ACMEN - Automatic Cache Management Enable

If *ACMEN (9Ch.6)* is high, the following functions are enabled:

- *TBKH/L (25h/24h)* increments at the end of each data-in block transfer
- *TCC (9Dh)* and *TTC (9Fh)* decrements at the end of each data-in block transfer
- *TCC (9Dh)* minus ***N*** and *TBKH/L (25h/24h)* plus ***N*** right after *SKIPC (9Eh)* is set ***N***

If *ACMEN (9Ch.6)* is high and *TTC (9Fh)* is not zero, the following functions are executed when *ADTT (17h.w2)* is triggered:

- *MBC4-0 (12h.4-0)* ← min{ *ATLIM (9Ch.4-0), TCC (9Dh), TTC (9Fh)* } minus 1
- *ATBHI/LO (35h/34h)* ← (MBC4-0 + 1) × (TWCH/L + 1) x 2 if *STWCEN (18h.3)* is high

Registers SKIPC (9Eh) and TTC (9Fh) are stuck at 0 if *ACMEN (9Ch.6)* is low.

Bit 5: TCINCEN - Transfer Cache Increment Enable

When this bit is high, the *TCC (9Dh)* increments at the end of EDC-checking if there is no *STAERR (80h.r6)* or *HCEI (80h.r0)* error. This bit should be high if *TCC (9Dh)* is used to implement cache management.

Bit 4-0: ATLIM[4:0] - Automatic Transfer Block Limit

If *ACMEN (9Ch.6)* is high and *TCC (9Fh)* is not zero, these five bits specify the maximum number of blocks that can be transferred to host in one trigger. The minimum limit is 1. Setting 0 to these bits specify limit as 32 blocks.

TCC - Transfer Cache Counter - (read/write 9Dh)

This counter can be used to implement cache management if *RMSRI (5Ch.0)* is high. If *TCINCEN (9Ch.5)* is high, *TCC (9Dh)* increments at the end of EDC-checking if there is no *STAERR (80h.r6)* or *HCEI (80h.r0)* error. If *ACMEN (9Ch.6)* is high, *TCC (9Dh)* decrements at the end of each data-in block transfer unless the value is zero. The value follows 0 is 0. The transfer of working area data should be implemented as linear transfer to prevent extra decrement of this counter.

If *ACMEN (9Ch.6)* is high, *TCC (9Dh)* minus ***N*** right after *SKIPC (9Eh)* is set ***N***. This function can be used to implement the cache-partial-hit event.

This register is 0 after chip reset, host reset and firmware reset. This counter should be set 0 in cache-miss case. Writing this register should be prevented when the decoder is on or the data-in transfer is in progress.

SKIPC - Skip Count - (read/write 9Eh)

This register is used as skip count to implement a partial-hit event of transfer cache. If *ACMEN (9Ch.6)* is high, the following functions are executed right after *SKIPC (9Eh)* is set ***N***:

- *BUFC (9Bh,r)* minus ***N***
- *TCC (9Dh)* minus ***N***
- *TBH/L (25h/24h)* plus ***N***
- *SKIPC (9Eh) minus* ***N***

After execution of the above operations, the value in *SKIPC (9Eh)* is 0.

This register is 0 after chip reset, host reset and firmware reset. This register is stuck at 0 if *ACMEN (9Ch.6)* is low.

TTC - Total Transfer Count - (read/write 9Fh)

This register is used as total transfer count. If *ACMEN (9Ch.6)* is high, *TTC (9Fh)* decrements at the end of each data-in block transfer unless the value is zero. The value follows 0 is 0. The following events are generated at the end of data-in transfer only if *TCC (9Fh)* is zero:

- *TENDb (01h.r6)* ← 0
- Automatic Status Complete Sequence if *ASCEN (18h.5)* is enabled

This register is 0 after chip reset, host reset and firmware reset. This register is stuck at 0 if *ACMEN (9Ch.6)* is low.

2.3 uP8032 Function

The uP8032 architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, 512 bytes of RAM, three timer/counters, a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64 K data storage space.

2.3.1 Data Memory

The uP8032 can access up to 64K bytes of external Data Memory. This memory region is accessed by the MOVX instructions. If the addressed external RAM bank is assigned to AUX_RAM, the MOVX instruction is directed to the on-chip AUX_RAM without affecting Port 0 and 2. In addition, the uP8032 has the standard 256 bytes of on-chip RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing.

2.3.2 RAM and AUX_RAM

The size of internal data RAM is 512x 8 bytes. It is divided into two banks: 256 bytes of RAM and 256 bytes of AUX_RAM.

RAM 0 ~127 can be addressed directly and indirectly. Address pointers are R0 and R1 of the selected register bank.

RAM 128~255 can only be addressed indirectly. Address pointers are R0 and R1 of the selected registers bank.

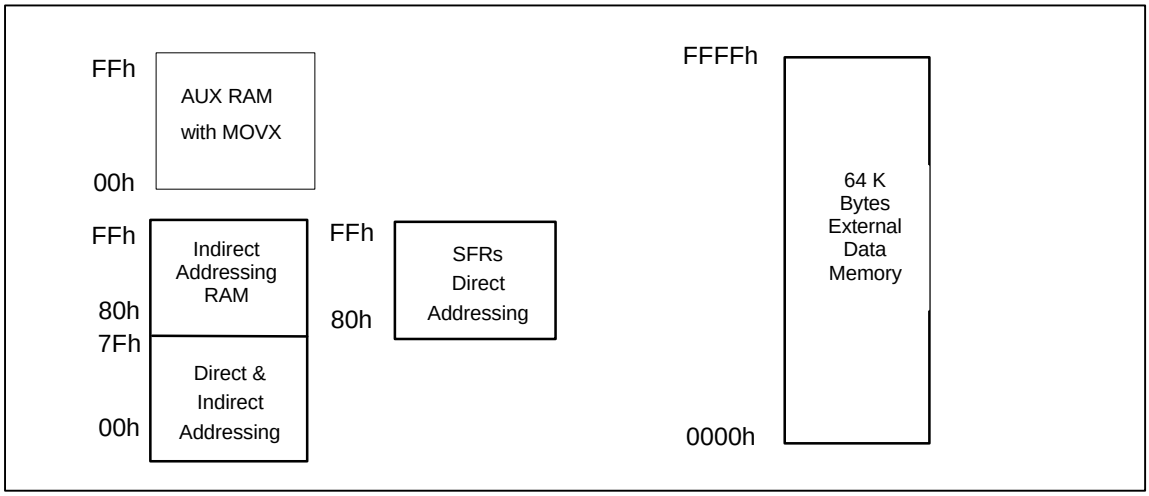
AUX_RAM 0~255 is addressed indirectly as the same way as external data memory with the MOVX instruction if the following conditions are satisfied:

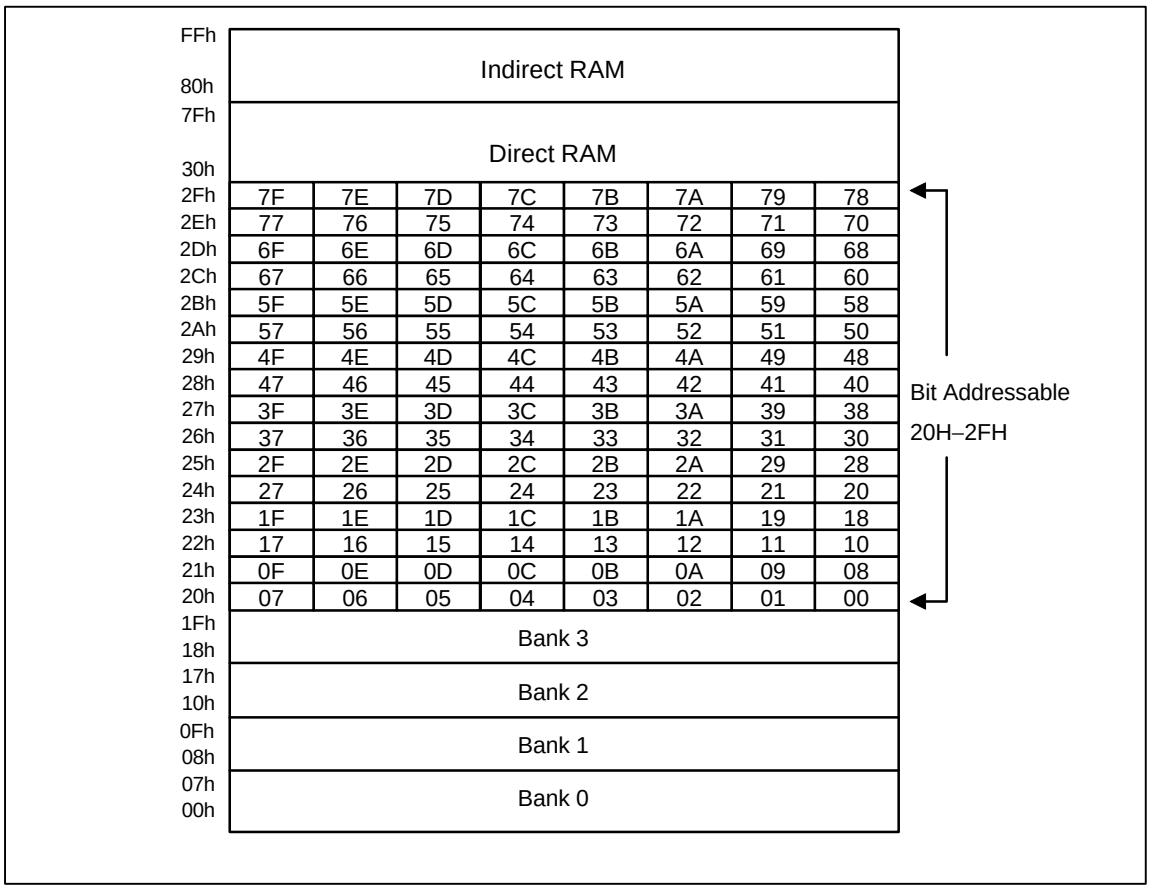
1. *EARAM (CHPCON.4)* is set high and
2. *DPH* or *P2* equals to *XRBANK (8Fh)*

Notice that AUX_RAM can be allocated to address other than 0000h ~ 00ffh by setting *XRBANK (8Fh)*. Address pointer are R0 and R1 of the selected register bank and DPTR. The following is an example to show how to access AUX_RAM by MOVX instruction.

```
MOV     CHPCON, #10h        ; set EARAM to 1.
MOV     XRBANK, #12h        ; allocate AUX_RAM to address 1200h to 12FFh.
MOV     DPTR, #1234h        ; address AUX_RAM with offset 34h
MOV     A, #55h
MOVX    @DPTR,A     ; access AUX-RAM
```

If *EAROM (CHPCON.5)* is set high, the AUX_RAM is programmed as AUX_ROM Mode that can be fetched and executed like an internal ROM.


FFh
AUX RAM
with MOVX
00h
FFh
Indirect
Addressing
RAM
80h
7Fh
Direct &
Indirect
Addressing
00h
FFh
SFRs
Direct
Addressing
80h
FFFFh
64 K
Bytes
External
Data
Memory
0000h


FFh
80h
Indirect RAM
7Fh
Direct RAM
30h
2Fh 7F 7E 7D 7C 7B 7A 79 78
2Eh 77 76 75 74 73 72 71 70
2Dh 6F 6E 6D 6C 6B 6A 69 68
2Ch 67 66 65 64 63 62 61 60
2Bh 5F 5E 5D 5C 5B 5A 59 58
2Ah 57 56 55 54 53 52 51 50
29h 4F 4E 4D 4C 4B 4A 49 48
28h 47 46 45 44 43 42 41 40
27h 3F 3E 3D 3C 3B 3A 39 38
26h 37 36 35 34 33 32 31 30
25h 2F 2E 2D 2C 2B 2A 29 28
24h 27 26 25 24 23 22 21 20
23h 1F 1E 1D 1C 1B 1A 19 18
22h 17 16 15 14 13 12 11 10
21h 0F 0E 0D 0C 0B 0A 09 08
20h 07 06 05 04 03 02 01 00
Bit Addressable
20H–2FH
1Fh
18h
Bank 3
17h
10h
Bank 2
0Fh
08h
Bank 1
07h
00h
Bank 0

2.3.3 AUX_ROM Mode and uP Programming Flash

If *EAROM (CHPCON.5)* is set high, the AUX_RAM is programmed as AUX_ROM Mode that can be fetched and executed like an internal ROM. It can be used as a self-programming ROM code source to program external Flash Memory. In this mode, the following pins are directly controlled by its corresponding registers to implement the flash programming function.

Pin Name	Register	Function
A7-A0	*SFRFAL (C4h)*	Flash low address
UP27-UP20	*SFRFAH (C5h)*	Flash high address
UP07-UP00	*SFRFD (C6h)*	Flash data
GPIO2/DAO/nFCE	*UFCE (SFRCN.2)*	Flash chip enable
PSEN	*UFOE (SFRCN.1)*	Flash output enable
GPIO1/nFWE	*UFWE (SFRCN.0)*	Flash write enable

Note 1: The control bits in *SFRCN (C7h)* should be set the inverse value of its corresponding pins.

Note 2: In the switch period from external flash memory to AUX_ROM, the Program Counter will be reset to Zero, and uC will fetch and execute the ROM code from address 00H of AUX_ROM. Because the uP will prefetch the ROM code before switch, for sake of the system operating smoothly, the instruction MOV CHPCON,EAROM should will be followed by the instruction NOP to avoid the danger caused by compulsive PC reset.

2.3.4 Special Function Register (SFR)

The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing. And the AUX_RAM is only accessed by MOVX instruction with selected external RAM address range.

Address spaces 20H to 2FH to internal RAM are bit-addressable and can be used by the Boolean Variable Manipulation instructions. For example, bit 0 of address 20H has a Boolean address 00H, and bit 7 of address 2FH has a Boolean address 7FH. The higher Boolean addresses (80H–FFH) are mapped into the SFR address space. To determine a Boolean address in a particular bit-addressable SFR, one can combine the higher 5 bits of the SFR address with 3 lower bits that specify the desired bit in the SFR.

Special Function Registers (SFRs)

F8									FF
F0	+B						**CHPENR**		F7
E8									EF
E0	+ACC								E7
D8									DF
D0	+PSW								D7
C8	+T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0					**SFRAL**	**SFRAH**	**SFRFD**	**SFRCN**	C7
B8	+IP							**CHPCON**	BF
B0	+P3								B7
A8	+IE								AF
A0	+P2								A7
98	+SCON	SBUF							9F
90	+P1								97
88	+TCON	TMOD	TL0	TL1	TH0	TH1	**WKCTL**	**XRBANK**	8F
80	+P0	SP	DPL	DPH				PCON	87

Note: 1.The SFRs marked with a plus sign(+) are both byte- and bit-addressable.

2. The text of SFR with bold type characters are extension function registers.

WKCTL (8Eh) - Wake Up Control Register

The chip enters power-down mode by setting *PD (PCON.1)* high,. In this mode, the crystal feedback loop between UXI and UXO is closed. This register controls the wake up mechanism.

Bit 7: EIWK - Enable Interrupt Wake Up

If this bit is high, this chip wakes up from power-down mode on INT0 or INT1.

Bit 4: EHWK - Enable Host Wake Up

If this bit is high, the chip wake up from power-down mode when:

(1) SRST is set high if *HIITEN (2Eh,w7)* is high, or

(2) reception of DEVICE RESET command (opcode 08h) if *ARSTEN (2Fh.w3)* is high.

Bit 2-0: CSC[2:0] - Crystal Stabilization Counter

These bits define the time needed to release the clock into the chip.

DSC	No. of Clocks	Remrak
000b	176	
001b	352	
010b	704	
011b	1408	default
100b	2816	
101b	5632	
110b	11264	
111b	22528	

XRBANK (8Fh) - AUX_RAM Bank Selection Register

AUX_RAM can be allocated to address start from (***N*** × 0100h) by setting *XRBANK (8Fh)* as ***N***. AUX_RAM is addressed indirectly as the same way as external data memory with the MOVX instruction if *EARAM (CHPCON.4)* is set high and DPH or P2 equals to *XRBANK (8Fh).*

CHPCON (BFh) - Chip Control Register

The *CHPCON (BFh)* is read only by default. You must write #87, #59H sequentially to *CHPENR (F6h)* to enable the *CHPCON* write attribute, and write any other value to *CHPENR* disable *CHPCON* write attribute.

Bit 7, 0: SWRST - Software Reset

Setting both of these bits high forces the uP to the initial conditions after master reset.

Bit 5: EAROM - Enable AUX_ROM Mode

Setting this bit high enables AUX_ROM Mode.

Bit 4: EARAM - Enable AUX_RAM Mode

Setting this bit high enables AUX_RAM Mode.

SFRFAL (C4h) - Flash Low Byte Address Register

If *EAROM (CHPCON.5)* is set high, the value of this register controls pin A7-A0.

SFRFAH (C5h) - Flash High Byte Address Register

If *EAROM (CHPCON.5)* is set high, the value of this register controls pin UP27-UP20.

SFRFD (C6h) - Flash Data Register

If *EAROM (CHPCON.5)* is set high, this register controls and reflect the status of UP07-UP00.

SFRCN (C7h) - Flash Control Register

Bit 2: UFCE - Flash Chip Enable

If *EAROM (CHPCON.5)* is set high, the inverse status of this bit controls pin GPIO2/DAO/nFCE.

Bit 1: UFOE - Flash Output Enable

If *EAROM (CHPCON.5)* is set high, the inverse status of this bit controls pin PSEN.

Bit 0: UFWE - Flash Write Enable

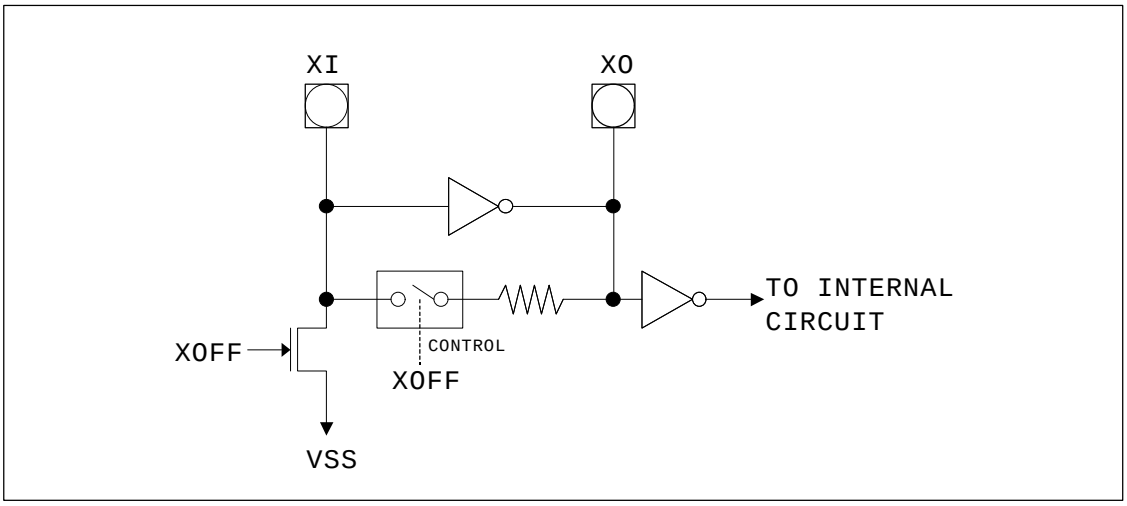
If *EAROM (CHPCON.5)* is set high, the inverse status of this bit controls pin GPIO1/nFWE.

CHPENR (F6h) - Chip Control Register Write Enable Register

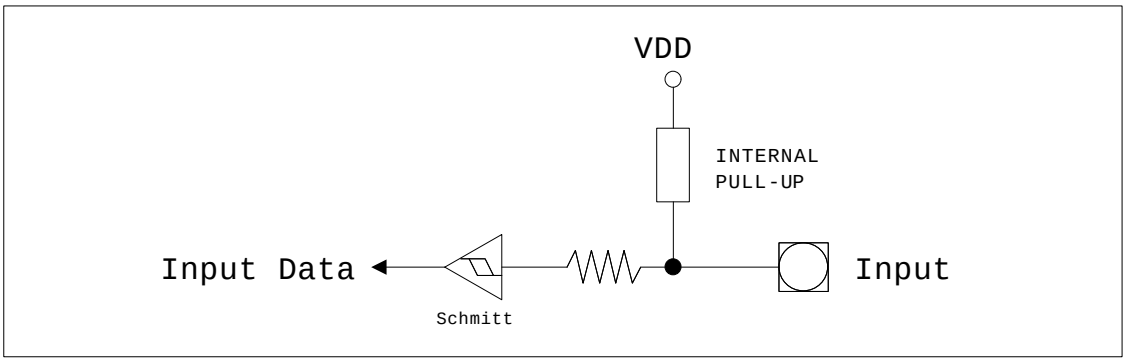
The *CHPCON (BFh)* is read only by default. You must write #87,#59H sequentially to *CHPENR (F6h)* to enable the *CHPCON* write attribute, and write any other value to *CHPENR* disable *CHPCON* write attribute.

3. Diagram of Equivalent Circuit in Input/Output Port

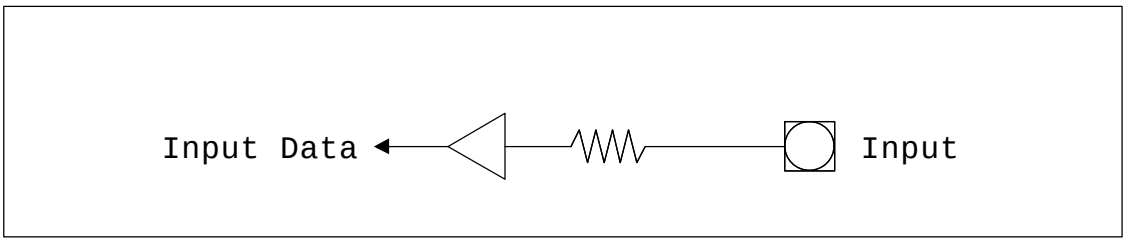
◆ **DXI/DXO and UXI/UXO**



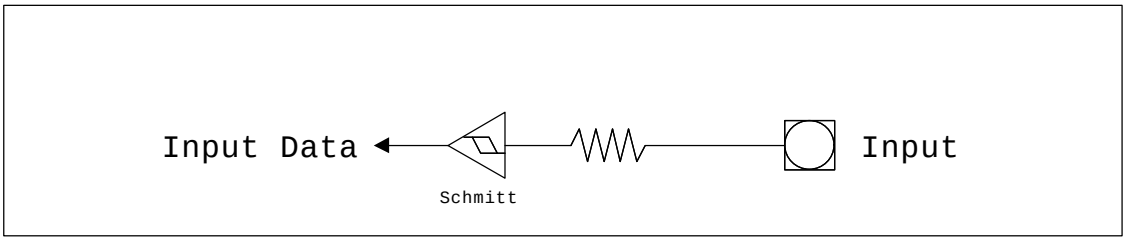
◆ **nPOR, nHRST**



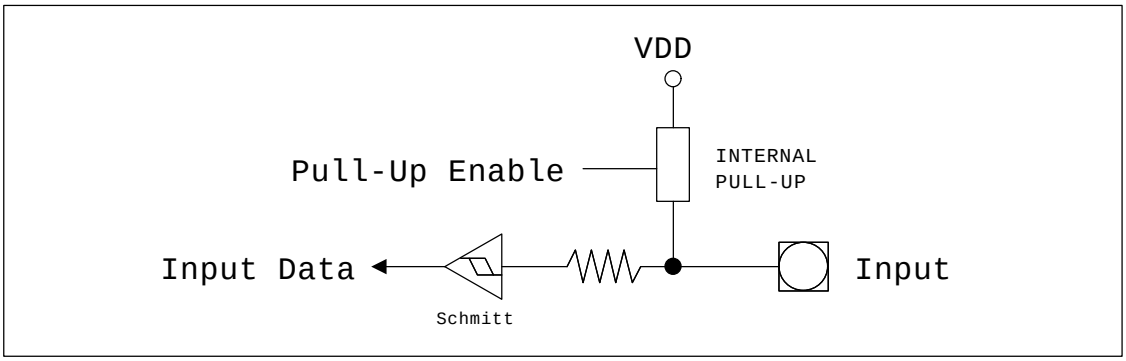
◆ **LRCK, BCK, SDATA, C2PO**



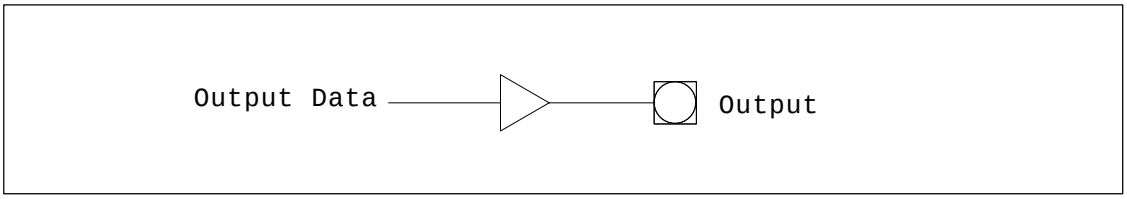
◆ **SCSD, WFCK, SCSYN**



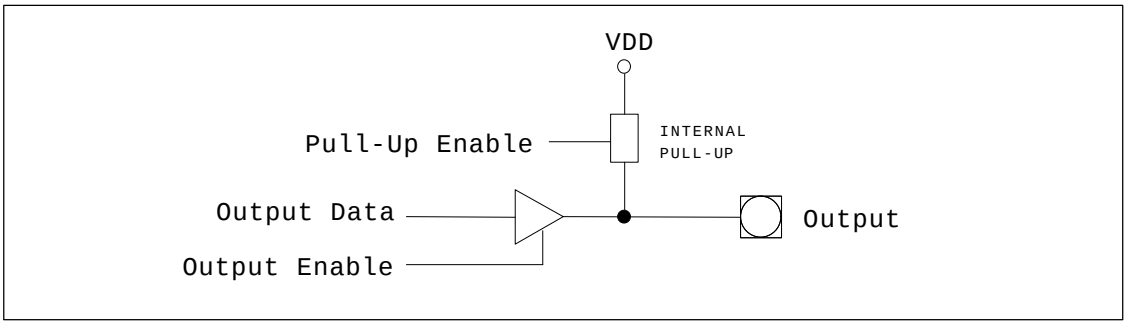
◆ **nHRD, nHWR, nCS1, nCS3, DA2-0, nDMACK**



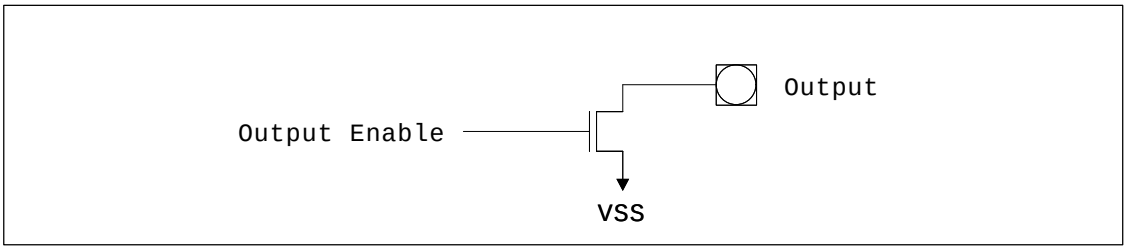
◆ **nRSTO, CKO**



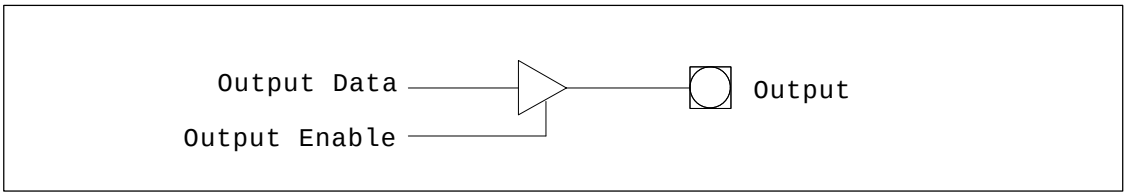
◆ **ALRCK, ABCK**



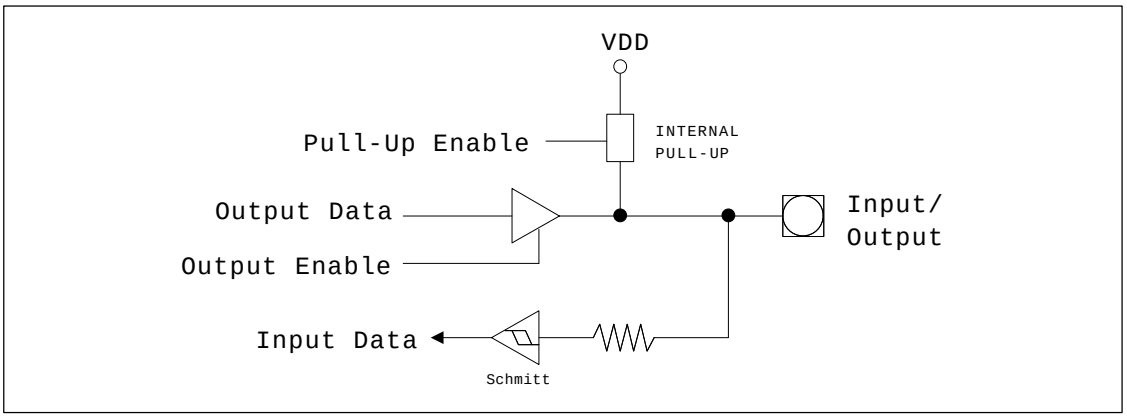
◆ **nCS16**



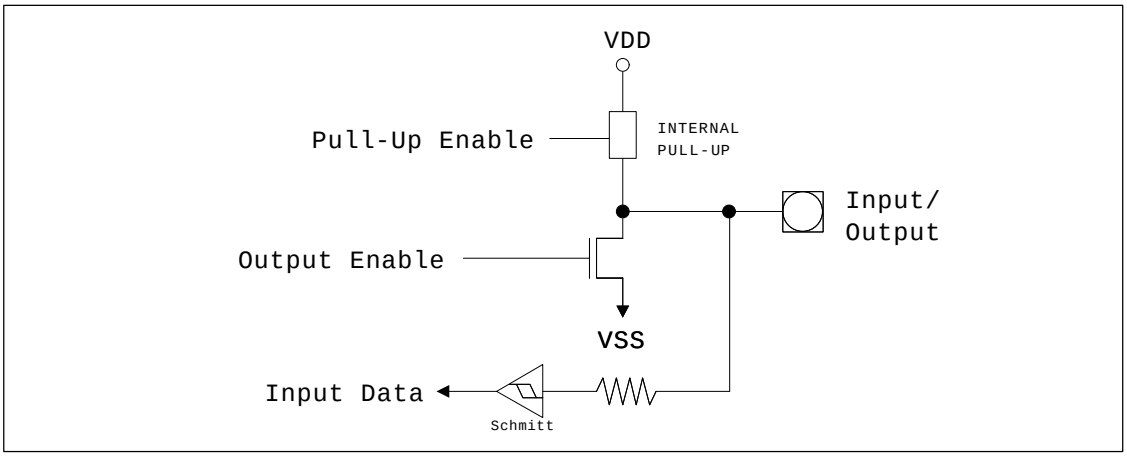
◆ **HIRQ, IORDY, DMARQ, A7-0**



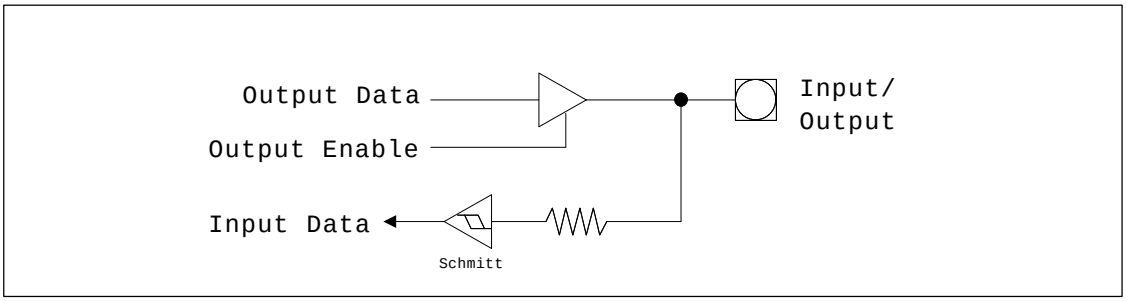
◆ **GPIO1-4, RA7-0, RD15-0, DD15-0, EXCK, ASD/nROE**



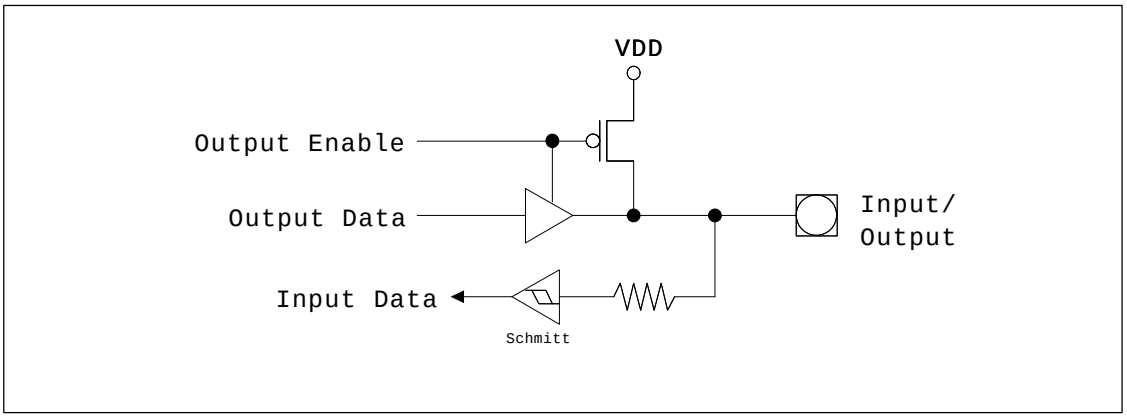
◆ **nDASP, nPDIAG**



◆ **P0**



◆ **P1, P2, P3, PSEN**



4. Electronic Characteristics

4.1 Absolute Maximum Ratings

SYM	PARAMETER	MIN	MAX	UNIT
V_{DD}	Power Supply Voltage	-0.3	6.5	V
V_{IN}	Input Voltage	-0.3	V_{DD} + 0.3	V
T_{OP}	Operation Temperature	0	70	°C
T_{ST}	Storage Temperature	-55	150	°C

4.2 DC Characteristics

(T_A = 0°C TO 70°C, V_{DD} = 5V±5%, V_{ss} = 0V)

SYM	PARAMETER	MIN	MAX	UNIT	CONDITION
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH}=400µA
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} (Note 1)
V_{IH1}	Input HIGH Voltage	0.7×V_{DD}	V_{DD}+0.5	V	DXI, UXI, LRCK,
V_{IL1}	Input LOW Voltage	-0.5	0.3×V_{DD}	V	BCK, SDATA, C2PO
V_{IH2}	Input HIGH Voltage	2	V_{DD}+0.5	V	Others
V_{IL2}	Input LOW Voltage	-0.5	0.8	V	
I_{LI1}	(1) Input Leakage Current	-140	-400	µA	Pins with Pull-up Resistor at PAD = 0V (Notes 3)
I_{LI2}	(2) Input Leakage Current	-80	-200	µA	
I_{LI3}	(3) Input Leakage Current	-40	-100	µA	
I_{LI4}	(4) Input Leakage Current	-10	-40	µA	
I_{LI5}	Input Leakage Current	-10	10	µA	Others

Note (1): Output current (IOL) Capabilities:

4mA: UP10-17, UP20-27, UP30-37, A0-7

6mA: GPIO1-4, CKO, EXCK, RA7-RA0, RD0-15, ALRCK, ABCK, ASD

8mA: UP00-07, CAS, CASH, RAS, nWRE

12mA: DD0-15, nDASP, nPDIAG, HIRQ, DMARQ

24mA: nCS16, IORDY

Note (2): The chip contains internal resistance between UXI/UXO and DXI/DXO

Note (3): The chip contains internal pull-up resistance between VDD and the following pins:

Type (1): DA0-2, nHRD, nHWR, nCS1, nCS3, nDMACK, nPOR, nHRST, PSEN

Type (2): DD0-15, RD0-15, nDASP, nPDIAG, EXCK

Type (3): ALRCK, ABCK, ASD, RA0-7, GPIO1-4

Type (4): UP10-17, UP20-27, UP30-37, A7, A6

4.3 AC Characteristics

◆ **Reset Timing**

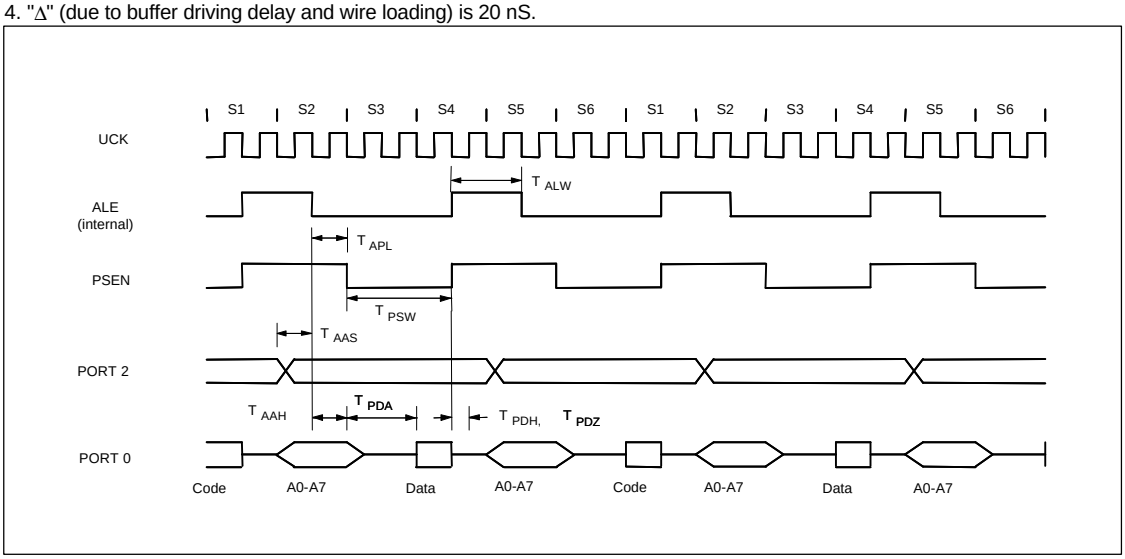
Item	Symbol	Description	Min. (ns)	Max. (ns)	Notes
1	T_{RST}	Reset pulse width	$24 \times T_{UP}$		(1)

Note (1): T_{UP} = Cycle time of UCK (clock from pin UXI).

◆ uP Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TUP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TUP-Δ	-	-	nS	1, 4
ALE Low to PSEN Low	TAPL	1 TUP-Δ	-	-	nS	4
PSEN Low to Data Valid	TPDA	-	-	2 TUP	nS	2
Data Hold after PSEN High	TPDH	0	-	1 TUP	nS	3
Data Float after PSEN High	TPDZ	0	-	1 TUP	nS	
ALE Pulse Width	TALW	2 TUP-Δ	2 TUP	-	nS	4
PSEN Pulse Width	TPSW	3 TUP-Δ	3 TUP	-	nS	4

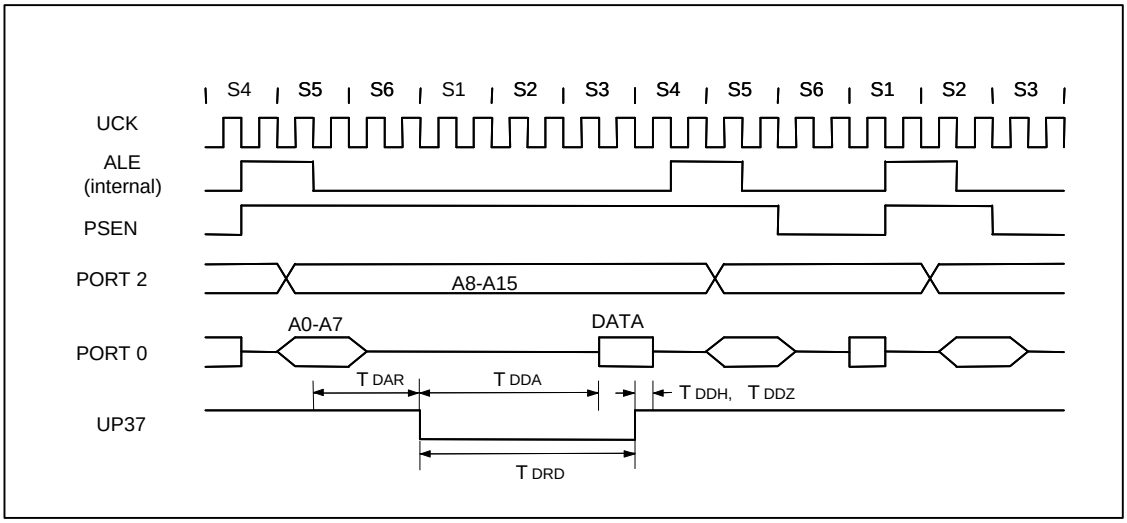
Notes:
1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TUP.
3. Data have been latched internally prior to PSEN rise.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.



◆uP Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to UP37 Low	TDAR	3 TUP-Δ	-	3 TUP+Δ	nS	1, 2
UP37 Low to Data Valid	TDDA	-	-	4 TUP	nS	1
Data Hold from UP37 High	TDDH	0	-	2 TUP	nS	
Data Float from UP37 High	TDDZ	0	-	2 TUP	nS	
UP37 Pulse Width	TDRD	6 TUP-Δ	6 TUP	-	nS	2

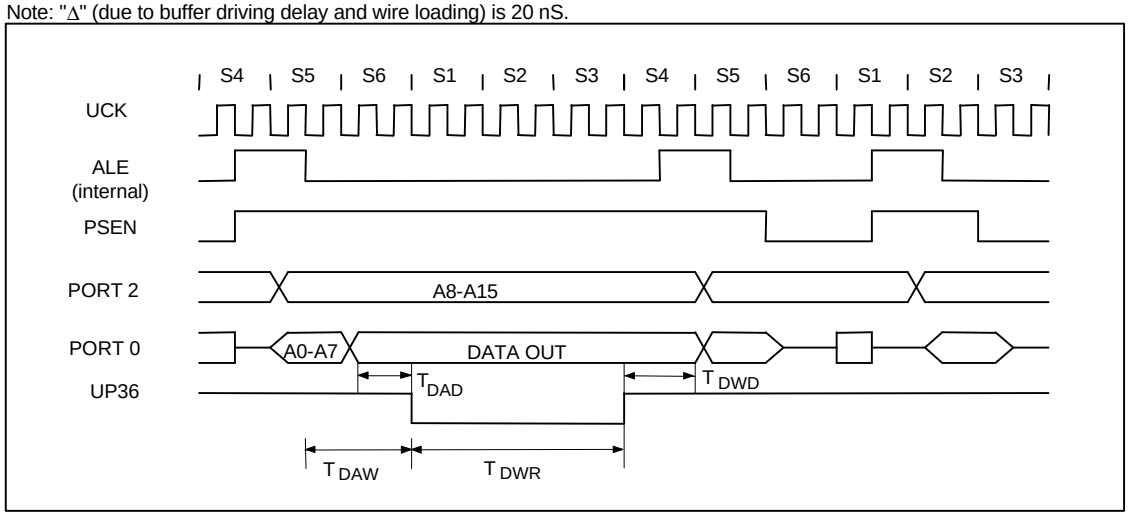
Notes:
1. Data memory access time is 8 TUP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.



◆uP Data Write Cycle

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to UP36 Low	TDAW	3 TUP-Δ	-	3 TUP+Δ	nS
Data Valid to UP36 Low	TDAD	1 TUP-Δ	-	-	nS
Data Hold from UP36 High	TDWD	1 TUP-Δ	-	-	nS
UP36 Pulse Width	TDWR	6 TUP-Δ	6 TUP	-	nS

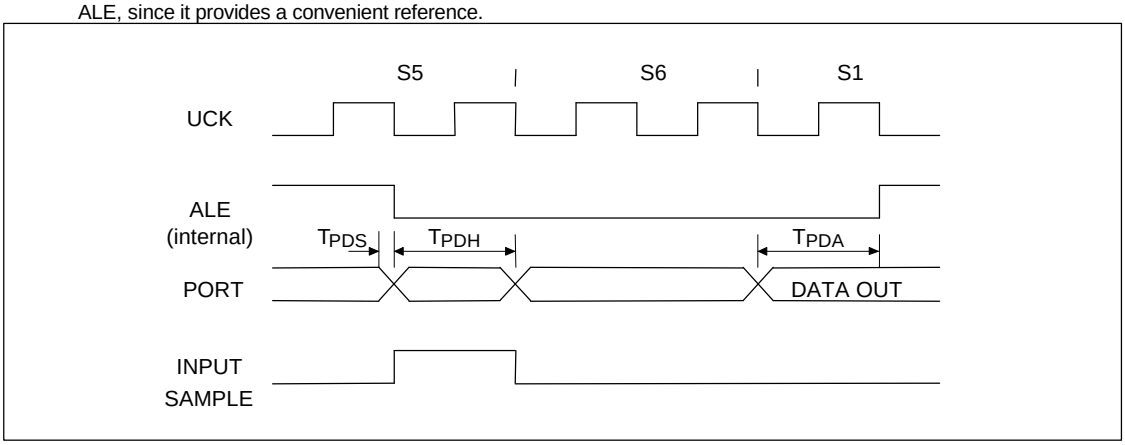
Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.



◆uP Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TUP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TUP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

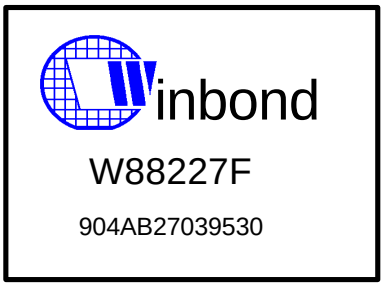


5. Ordering Instruction

Part No.	Package
W88227F	PQFP 128
W88227QD	LQFP 128

6. How to READ THE TOP MARKING

Example: The top marking of W88227F



1st line: Winbond logo

2nd line: the type number: W88227F or W88227QD

3rd line: Tracking code 904 A F 1 7039530

904: packages made in '99, week 4

A: assembly house ID; A means ASE, S means SPIL

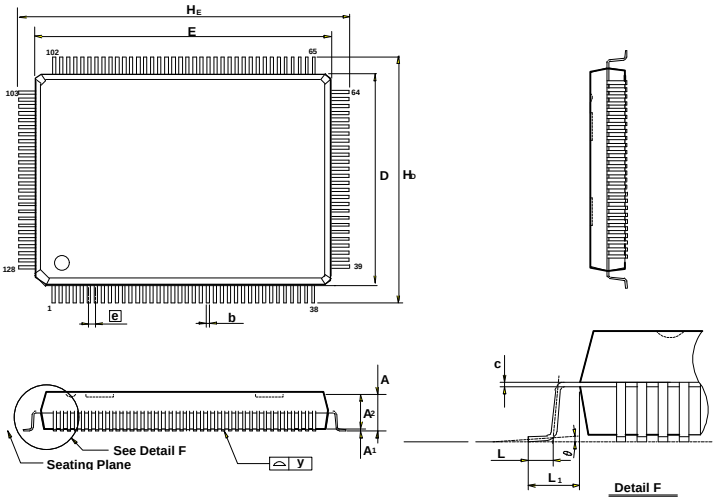
B: IC revision; A means version A, B means version B

2: wafers manufactured in Winbond FAB 2

7039530: wafer production series lot number

7. Package Dimension

(W88227F, 128-pin PQFP)

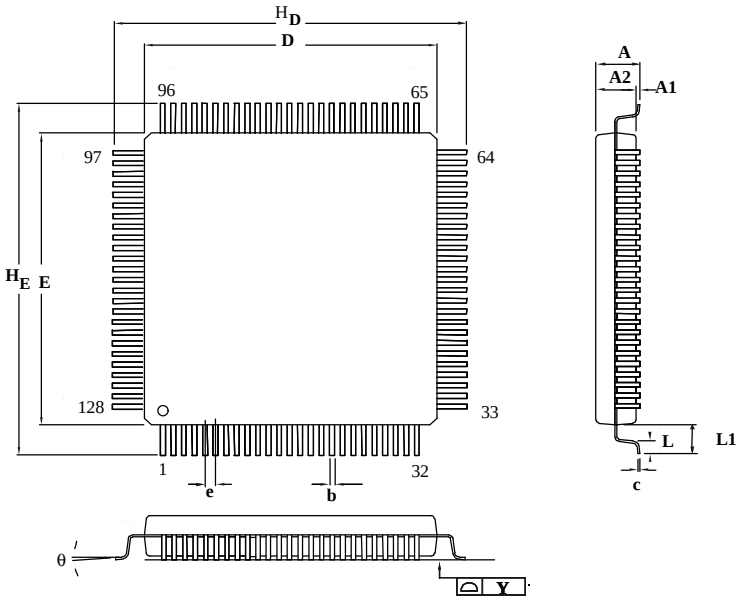


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

Note:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

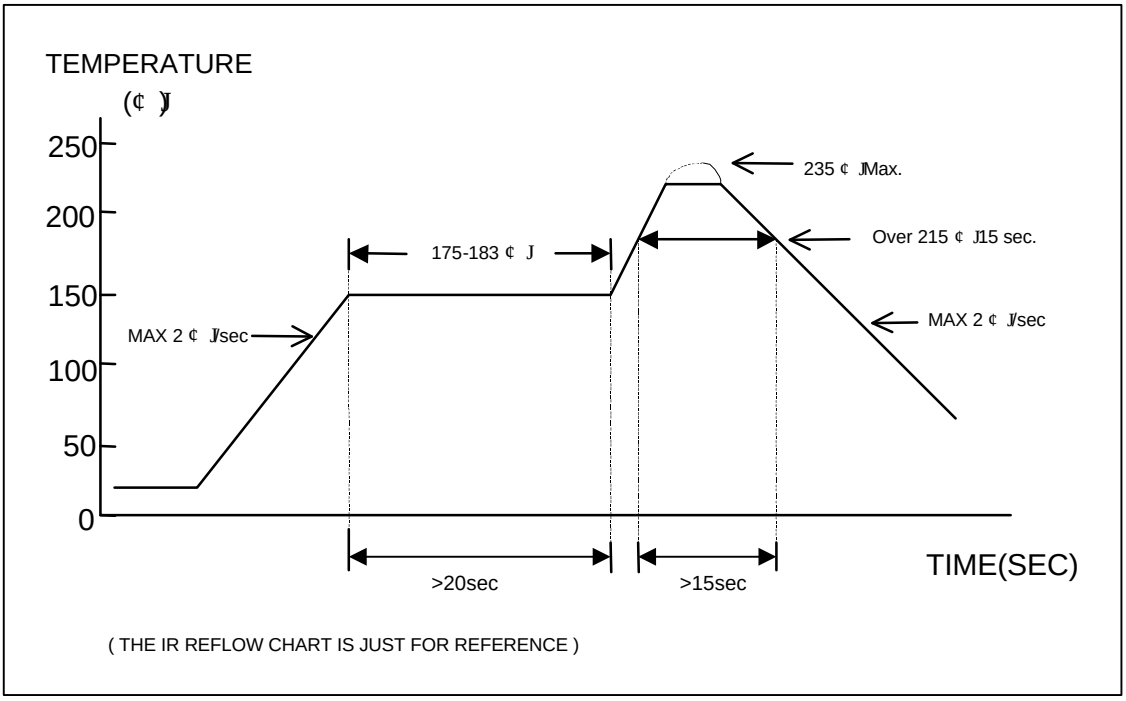
(W88227QD, 128-pin LQFP)



Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	0.006	0.05	—	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.006	0.009	0.13	0.16	0.23
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.016	—	—	0.40	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

8. Example Temperature Profile for Infrared Reflow



(THE IR REFLOW CHART IS JUST FOR REFERENCE)