

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUITS

μ PD16300GF

41bit DC • PDP driver

The μ PD16302 is a ROW driver utilized high Bi-CMOS process for DC plasma display panel. It consists of a 41bit bidirectional shift register and high voltage NPN Transistor.

It operates 5V (CMOS input level) and drives 150V and 500mA max. (Open collector output)

Features :

- High voltage Transistor + CMOS structure
- High voltage current output (150V, 500mA max.)
- Built-in 41bit bidirectional shift register
- Low power dissipation (1mA max., Ta = -40 ~ +85°C)
- Symmetry pin configuration by tridirectional lead quad flat package
: 100 pin Plastic flat package
- Wide operating temperature (-40 ~ +85°C)

• ORDERING INFORMATION :

μ PD16300GF-3L9 : 80pin Plastic QFP (tri directional lead)

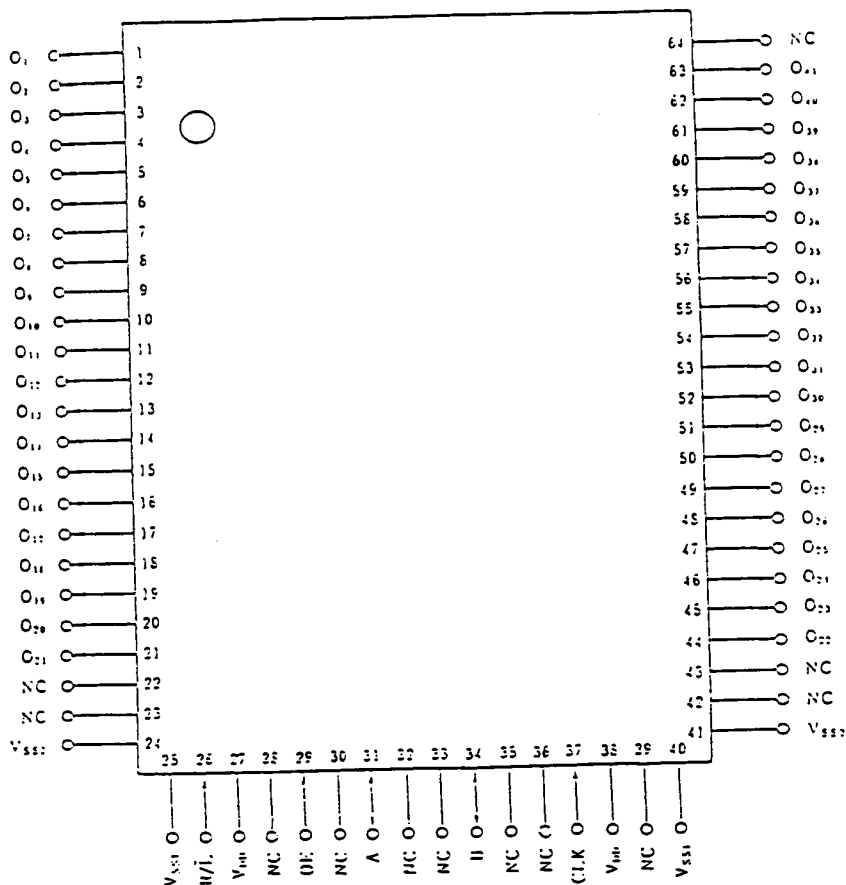
NEC reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.

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● PIN CONNECTION

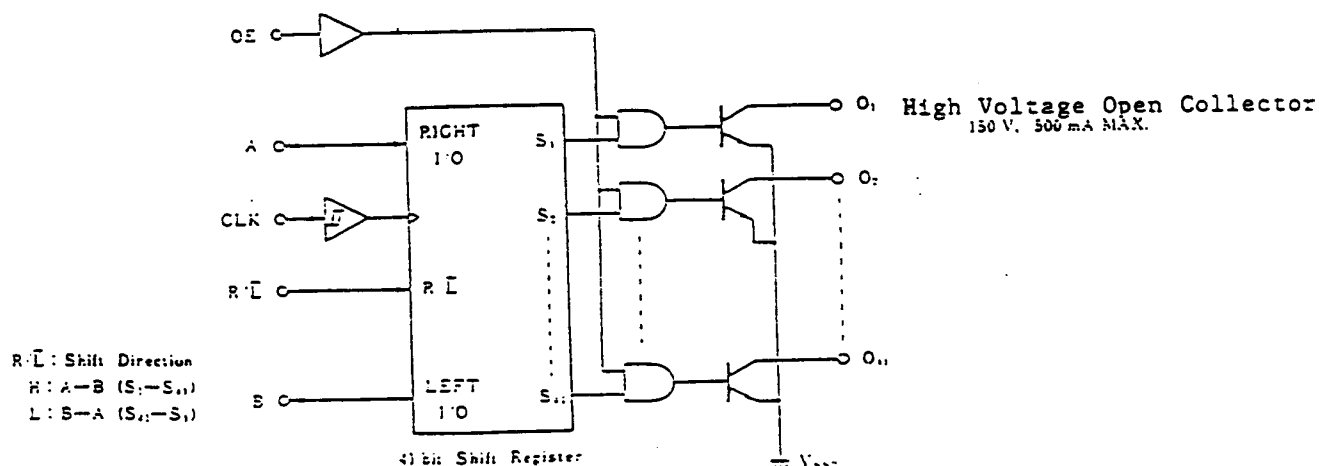
=== TOP VIEW ===



Please connect outside between the same power supply pins, such as VDDs and, Vss1 and Vss2.

Please open 33pin because of connecting lead frame.

=== Block Diagram ===



Pin Configuration

SYMBOL	Pin Name	Pin No.	Function
OE	Output Enable Input	29	H : 01-41 Data Output L : 01-41 High Impedance
A	Right Data I/O	31	Serial Data input/output R/L=H : A=IN, B=OUT R/L=L : B=IN, A=OUT
B	Left Data I/O	34	
CLK	Shift Clock Input	37	Positive edge active
R/ $\overline{L}$	Shift Direction Control Input	26	H : Right shift mode A $\rightarrow$ 01 $\sim$ 041 $\rightarrow$ B L : Left shift mode B $\rightarrow$ 041 $\sim$ 01 $\rightarrow$ A
O1 $\sim$ O41	High Voltage Output	1-21, 44-63	150V 500mA max.
VDD	Logic Power Supply	27, 38	5V $\pm$ 10%
VSS1	Ground (Logic)	25, 40	——
VSS2	Ground (Driver)	24, 41	——
NC	No Connection	22, 23, 28, 30, 32, 33, 35, 36, 39, 42, 43, 64	No connection Please open 33 pin.

Truth Table 1 (Shift Register)

R/L	CLK	A	B	SHIFT REGISTER
H	↑	S1 input	S40 output *1	Data shift (to Right)
H	H OR L		S41 output	No change
L	↑	S2 output *2	S41 input	Data shift (to Left)
L	H OR L	S1 output		No change

*1 When CLK is positive edge active, S40 shifts to S41 and appears to be B.

*2 When CLK is positive edge active, S2 shifts to S1 and appears to be A.

Truth Table 2 (Driver)

DATA	O E	O1-41
×	L	Z (all off)
L	H	Z
H	H	L

H = High level, L = Low level, × = H or L

Z = High Impedance (Driver off)

DATA = Contents of Shift Register

Absolute Maximum Ratings
($T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$)

ITEMS	SYMBOL	RATINGS	UNIT
Logic Power Supply	VDD	-0.5~+7.0	V
Input Voltage	V _I	-0.5~VDD+0.5	V
Logic Output Voltage	V _{O1}	-0.5~VDD+0.5	V
Driver Output Voltage	V _{O2}	-0.5~150	V
Driver Maximum current	I _{O2}	500 *1	mA
Power Dissipation/Package	P _D	1000	mW
Operating Temperature	T _{opt}	-40~+85	°C
Storage Temperature	T _{stg}	-65~+150	°C

*1 Duty $\leq$ 1/41

Recommended Operating Conditions
($T_a = -40 \sim +85^\circ\text{C}$, $V_{SS} = 0\text{V}$)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
Logic Power Supply	VDD1	4.5	5	5.5	V
High Level Input Voltage	V _{IH}	0.7 VDD		VDD	V
Low Level Input Voltage	V _{IL}	0		0.2 VDD	V
Driver Power Supply	V _{O2}	30		110	V
Driver Output Current	I _{O2}			300	mA

Electrical Characteristics
($T_a = 25^{\circ}\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Output Voltage	V_{OH1}	Logic $I_{OH1} = -1\text{mA}$	$0.9 V_{DD}$			V
Low Level Output Voltage	V_{OL1}	Logic $I_{OL1} = 1\text{mA}$			$0.1 V_{DD}$	V
Low Level Output Voltage	V_{OL2}	O1-41, $I_{OL2} = 300\text{mA}$		6	10	V
Output leak current	I_{TL}	$V_{O2} = 110\text{V}$, $O_E = V_{SS}$			10	μA
High level input current	I_I	$V_I = V_{DD}$ or V_{SS}			± 1	μA
High Level Input Voltage	V_{IH}		$0.7 V_{DD}$			V
Low Level Input Voltage	V_{IL}				$0.2 V_{DD}$	V
Stand by Current	I_{DD}	O1-41 1 output on $T_a = -40 \sim +85^{\circ}\text{C}$			1.0	mA
		O1-41, 1 output on, $T_a = 25^{\circ}\text{C}$			100	μA

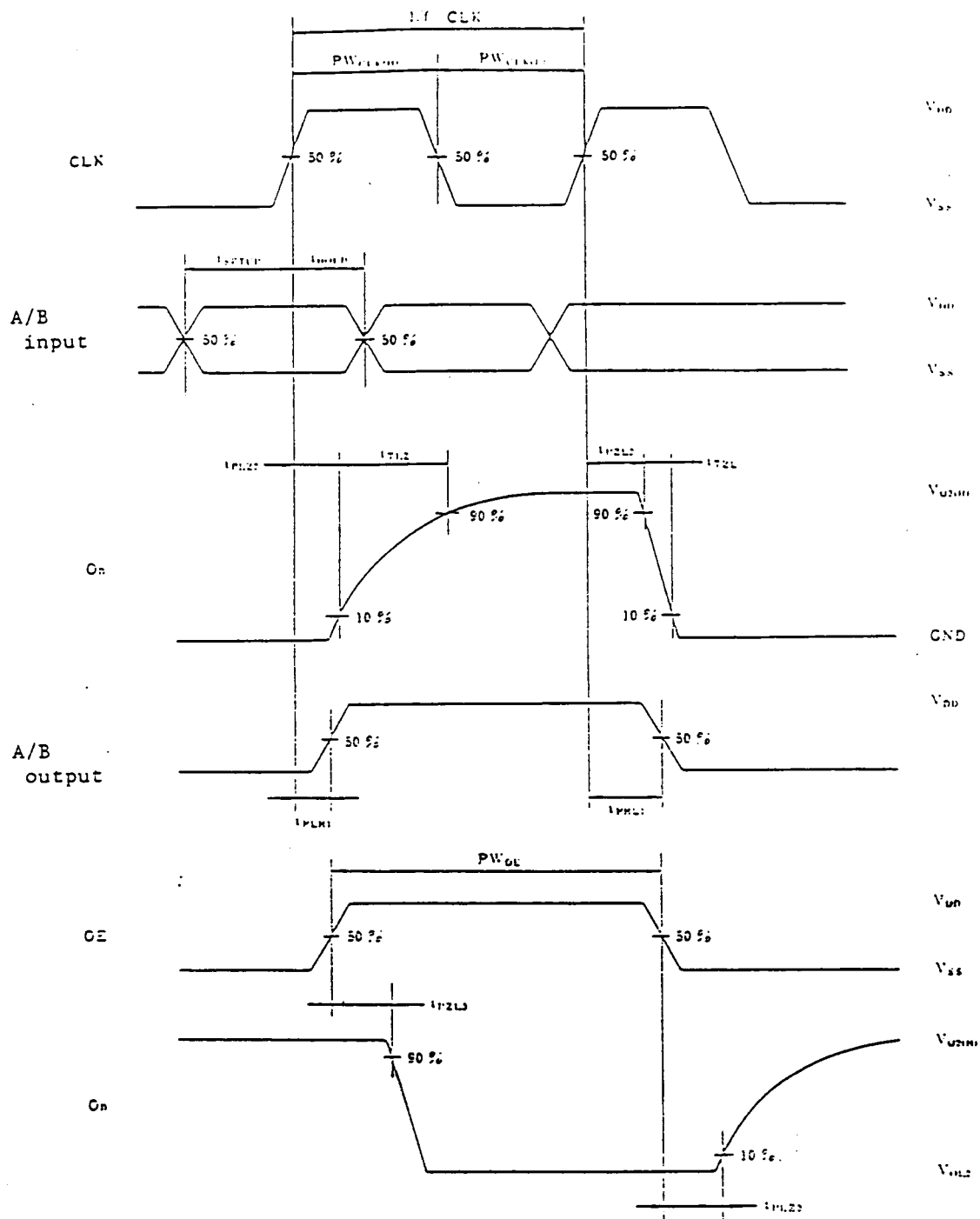
Switching Characteristics
 (Ta = 25°C, VDD = 4.5 ~ 5.5V, VO2(H) = 1.10V
 CL=150pF, RL=470Ω)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Delay time	t PHL1	CLK→A/B			100	ns
	t PLH1				100	ns
	t PZL2	CLK→O1~O41			100	ns
	t PLZ2				1.0	μs
	t PZL3	OE→O1~O41			100	ns
	t PLZ3				1.0	μs
Output Transient Time	t TLZ	O1-41			1.0	μs
	t TZL				0.1	μs
Maximum Clock Frequency	f MAX	Duty=50%	10			MHz
Input Capacitance	CI				10	pF

Timing Requirement Conditions
 (Ta = -40 ~ +85°C, VDD1 = 4.5 ~ 5.5V)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	PWCLK		50			ns
Enable Pulse Width	PWOE		1.2			μs
Data Setup Time	t SETUP		30			ns
Data Hold Time	t HOLD		10			ns

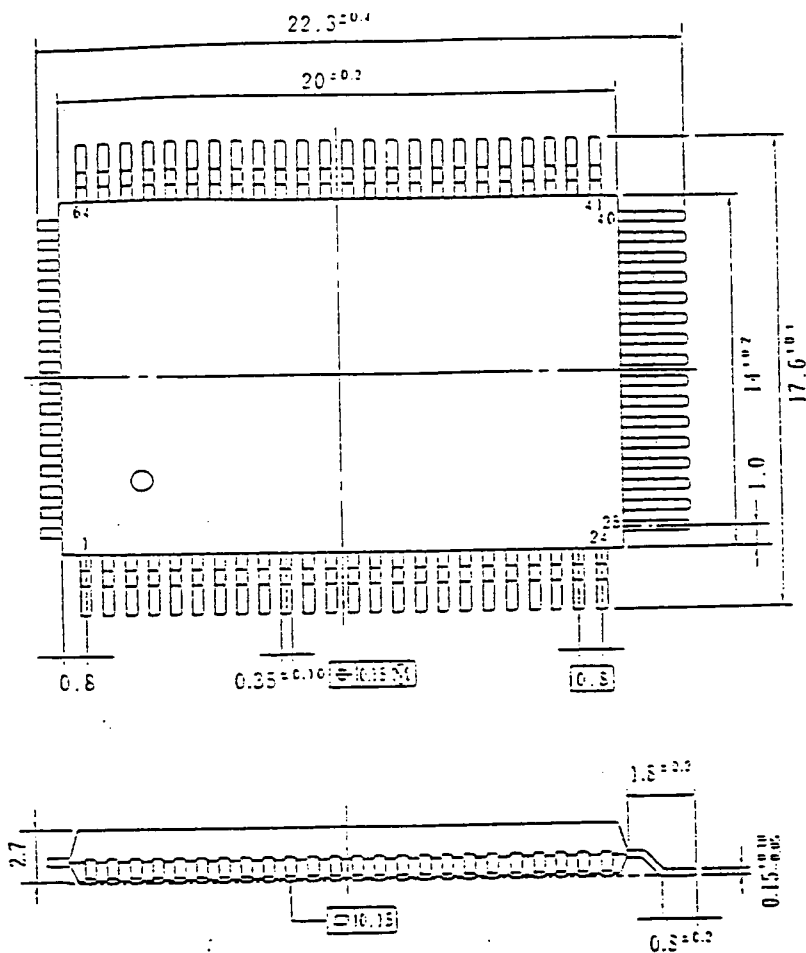
=== AC characteristics wave chart ===



=== Outline ===

80pin plastic QFP (Tri directional Lead)

unit:mm



P20CF-50-3L5