

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37754M6C-XXXGP

M37754M6C-XXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37754M6C-XXXGP and M37754M6C-XXXHP are single-chip microcomputers designed with high-performance CMOS silicon gate technology. This is housed in a 100-pin plastic molded QFP.

This microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing, and the bus interface unit enhances the memory access efficiency to execute instructions fast.

In addition to the 7700 Family basic instructions, the M37754M6C-XXXGP and M37754M6C-XXXHP has 6 special instructions which contain instructions for signed multiplication/division; these added instructions improve the servo arithmetic performance to control hard disk drives and so on.

This microcomputer also include the ROM, RAM, multiple-function timers, motor control function, serial I/O, A-D converter, D-A converter, and so on.

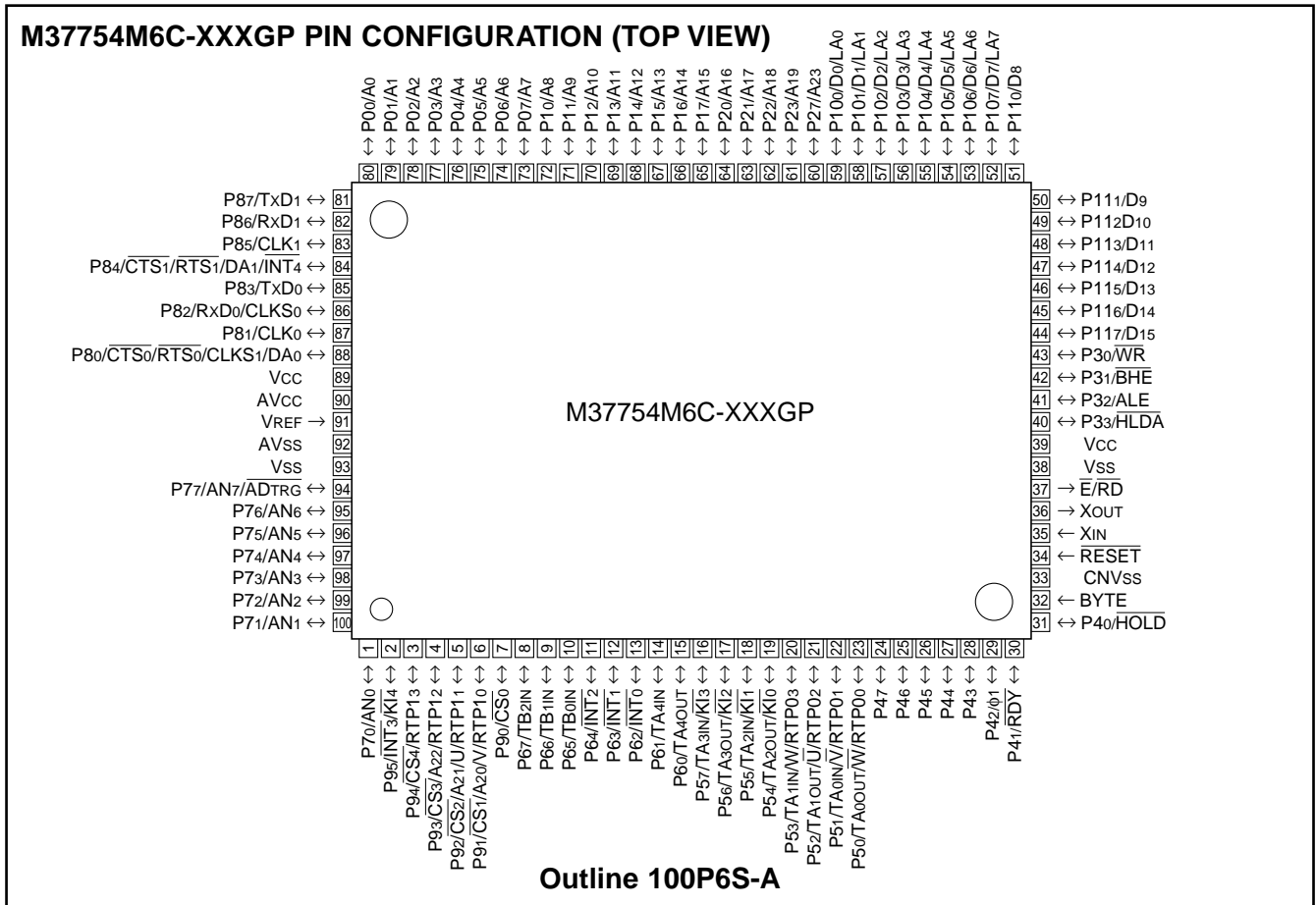
DISTINCTIVE FEATURES

- Number of basic machine instructions 109
 (103 basic instructions of 7700 Family + 6 special instructions)
- Memory size ROM 48 Kbytes
 RAM 2048 bytes
- Instruction execution time
 The fastest instruction at 40 MHz frequency 100 ns

- Single power supply 5V ±10 %
- Low power dissipation (at 40 MHz frequency) 125 mW (Typ.)
- Interrupts 21 types, 7 levels
- Multiple-function 16-bit timer 5+3
 (three-phase motor drive waveform or pulse motor control waveform output)
- Serial I/O (UART or clock synchronous) 2
- 10-bit A-D converter 8-channel inputs
- 8-bit D-A converter 2-channel outputs
- 12-bit watchdog timer
- Programmable input/output
 (ports P0—P11) 87
- Small package [M37754M6C-XXXHP]
 100-pin fine pitch QFP (read pitch : 0.5 mm)

APPLICATION

Control devices for personal computer peripheral equipment such as CD-ROM drives, hard disk drives, high density FDD, printers
 Control devices for office equipment such as copiers and facsimiles
 Control devices for industrial equipment such as communication and measuring instruments
 Control devices for equipment required for motor control such as inverter air conditioner and general purpose inverter



Outline 100P6S-A

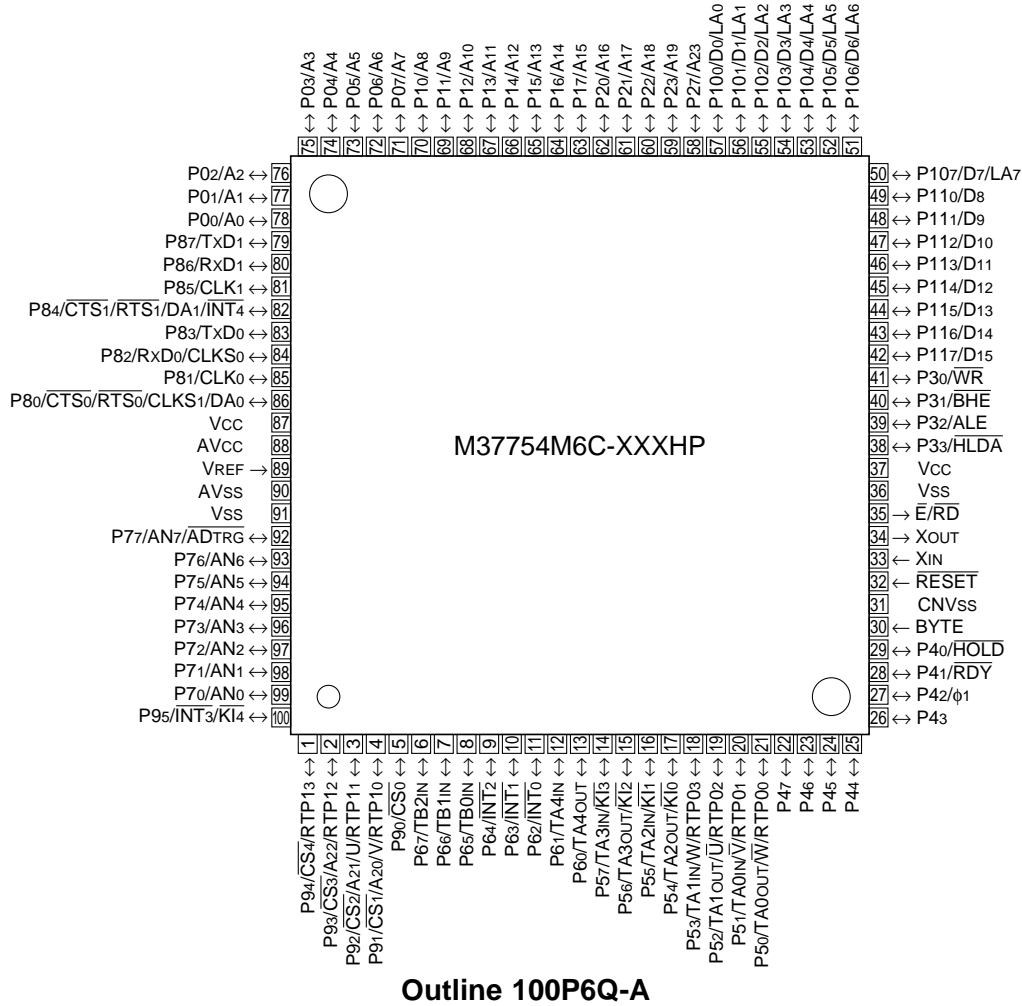


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M37754M6C-XXXGP
M37754M6C-XXXHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

M37754M6C-XXXHP PIN CONFIGURATION (TOP VIEW)



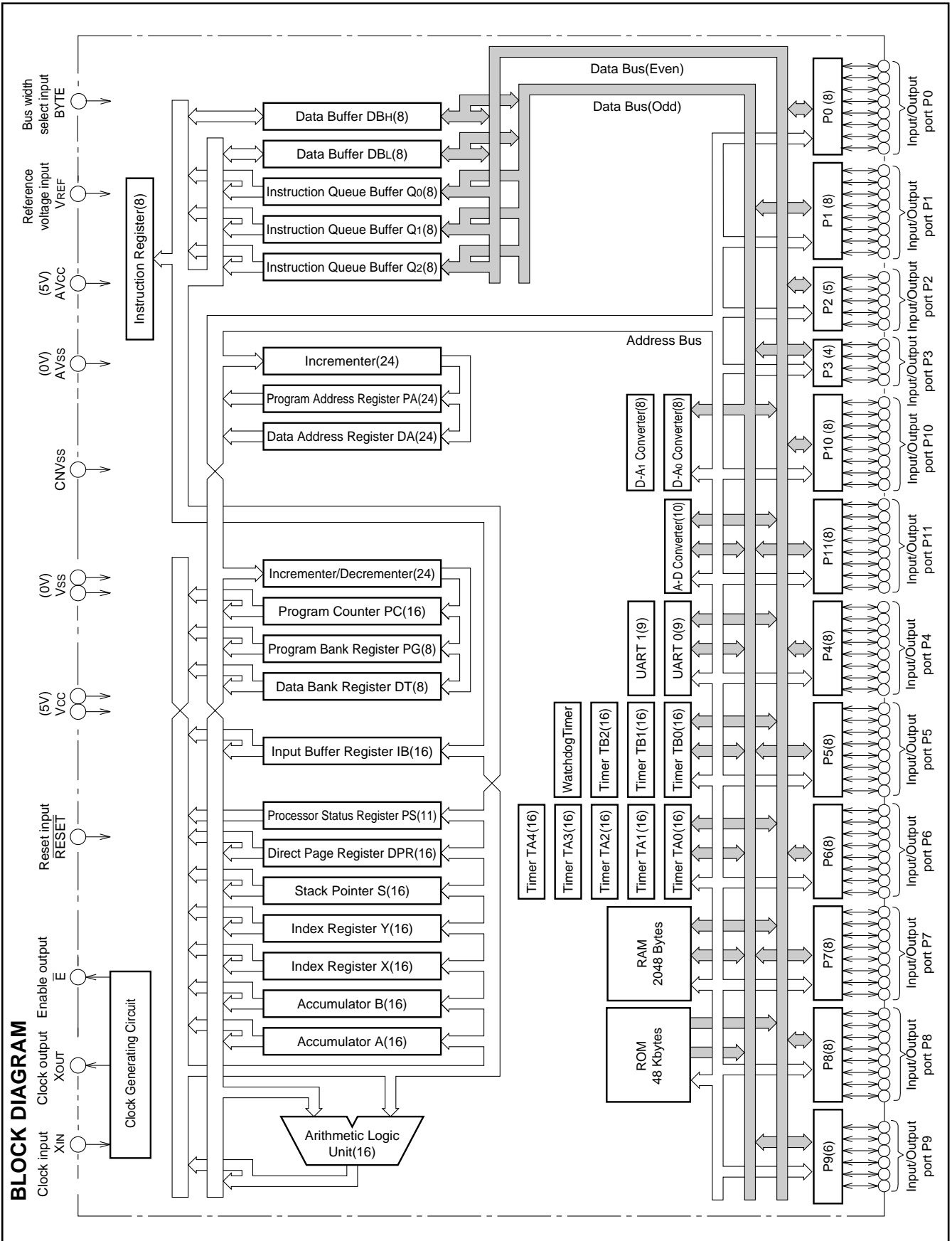
Differences between M37754M6C-XXXGP and M37754M6C-XXXHP

| Product | Package |
|-----------------|-----------------------------------|
| M37754M6C-XXXGP | 100-pin QFP (100P6S-A) |
| M37754M6C-XXXHP | 100-pin fine pitch QFP (100P6Q-A) |

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M37754M6C-XXXGP
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SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER



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FUNCTIONS OF M37754M6C-XXXGP

| Parameter | | Functions |
|--------------------------------------|--------------------------------|--|
| Number of basic machine instructions | | 109 |
| Instruction execution time | | 100 ns (the fastest instruction at external clock 40 MHz frequency) |
| Memory size | ROM | 48 Kbytes |
| | RAM | 2048 bytes |
| Input/Output ports | P0, P1, P4–P8, P10, P11 | 8-bit × 9 |
| | P2 | 5-bit × 1 |
| | P3 | 4-bit × 1 |
| | P9 | 6-bit × 1 |
| Multiple-function timers | TA0, TA1, TA2, TA3, TA4 | 16-bit × 5 |
| | TB0, TB1, TB2 | 16-bit × 3 |
| Serial I/O | | (UART or clock synchronous serial I/O) × 2 |
| A-D converter | | 10-bit × 1 (8 channels) |
| D-A converter | | 8-bit × 2 |
| Watchdog timer | | 12-bit × 1 |
| Dead-time timer | | 8-bit × 3 |
| Interrupts | | 5 external types, 16 internal types (Each interrupt can be set to priority levels 0–7.) |
| Clock generating circuit | | Built-in (externally connected to a ceramic resonator or quartz crystal resonator) |
| Supply voltage | | 5 V ± 10 % |
| Power dissipation | | 125 mW(at external clock 40 MHz frequency) |
| Input/Output characteristic | Input/Output withstand voltage | 5 V |
| | Output current | 5 mA |
| Memory expansion | | Maximum 16 Mbytes |
| Operating temperature range | | –20 to 85 °C |
| Device structure | | CMOS high-performance silicon gate process |
| Package | | 100-pin plastic molded QFP |

PIN DESCRIPTION (MICROCOMPUTER MODE)

| Pin | Name | Input/ Output | Functions |
|-----------------|-------------------------|------------------|--|
| Vcc, Vss | Power supply | | Supply 5 V±10 % to Vcc and 0 V to Vss. |
| CNVss | CNVss input | Input | This pin controls the processor mode. Connect to Vss for single-chip mode or memory expansion mode. Connect to Vcc for microprocessor mode. |
| RESET | Reset input | Input | This is reset input pin. The microcomputer is reset when supplying "L" level to this pin. |
| XIN | Clock input | Input | These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz-crystal resonator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open. |
| XOUT | Clock output | Output | |
| E | Enable output | Output | This pin outputs enable signal E, which indicates access state of data bus for single-chip mode. This pin outputs RD signal for memory expansion mode or microprocessor mode. |
| BYTE (Note) | Bus width select input | Input | This pin determines whether the external data bus is 8-bit width or 16-bit width for memory expansion mode or microprocessor mode. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs. |
| AVcc, AVss | Analog supply input | | Power supply for the A-D converter and the D-A converter. Connect AVcc to Vcc and AVss to Vss externally. |
| VREF | Reference voltage input | Input | This is reference voltage input pin for the A-D converter and the D-A converter. |
| P00-P07 | I/O port P0 | I/O | In single-chip mode, port P0 is an 8-bit I/O port. This port has an I/O direction register and each pin can be programmed for input or output. These ports are in the input mode when reset. Address (A0-A7) is output in memory expansion mode or microprocessor mode. |
| P10-P17 | I/O port P1 | I/O | In single-chip mode, these pins have the same functions as port P0. Address (A8-A15) is output in memory expansion mode or microprocessor mode. |
| P20-P23, P27 | I/O port P2 | I/O | In single-chip mode, these pins have the same functions as port P0. Address (A16-A19, A23) is output in memory expansion mode or microprocessor mode. |
| P30-P33 | I/O port P3 | I/O | In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, WR, BHE, ALE, and HLDA signals are output. |
| P40-P47 | I/O port P4 | I/O | In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, P40, P41, and P42 become HOLD and RDY input pins, and clock φ1 output pin respectively. Functions of other pins are the same as in single-chip mode. In memory expansion mode, P42 can be programmed as I/O port. |
| P50-P57 | I/O port P5 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2, timer A3, output pins for motor drive waveform, and input pins for key input interrupt. |
| P60-P67 | I/O port P6 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input INT0, INT1, and INT2, and input pins for timer B0, timer B1, and timer B2. |
| P70-P77 | I/O port P7 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as input pins for A-D converter. |
| P80-P87 | I/O port P8 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for UART0, UART1, output pins for D-A converter, and input pin for INT4. |
| P90-P95 | I/O port P9 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as input pin for INT3, output pins for motor drive waveform. In memory expansion mode and microprocessor mode, these pins can be programmed as address (A20-A22) or output pins for CS0-CS4. |

Note: It is impossible to change the input level of the BYTE pin in each bus cycle. In other words, bus width cannot be switched dynamically. Fix the input level of the BYTE pin to "H" or "L" according to the bus width used.

| Pin | Name | Input/Output | Functions |
|-------------|--------------|--------------|---|
| P100 – P107 | I/O port P10 | I/O | <p>In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, these pins become data I/O pins and operate as follows:</p> <p>(1) When using 16-bit width as external data bus width:</p> <ul style="list-style-type: none"> ● Accessing external memory <When reading> Pins' value is input into low-order internal data bus (DB0 to DB7). <When writing> Value of low-order internal data bus (DB0 to DB7) is output to these pins. ● Accessing internal memory <When reading> These pins become high impedance. <When writing> Value of internal data bus is output to these pins. <p>(2) When using 8-bit width as external data bus width:</p> <ul style="list-style-type: none"> ● Accessing external memory <When reading> Pins' value is input into internal data bus. The value is input into low-order internal data bus (DB0 to DB7) when accessing an even address; it is input into high-order internal data bus (DB8 to DB15) when accessing an odd address. <When writing> Value of internal data bus is output to these pins. The value of low-order internal data bus (DB0 to DB7) is output when accessing an even address; the value of high-order internal data bus (DB8 to DB15) is output when accessing an odd address. ● Accessing internal memory <When reading> These pins become high impedance. <When writing> Value of internal data bus is output to these pins. When the external bus width is 8 bits, the mode where low-order address (LA0 to LA7) is output when \overline{RD} or \overline{WR} output is "H" and data (D0 to D7) is input/output when \overline{RD} or \overline{WR} output is "L" can be selected in specified external memory area access cycle. |
| P110 – P117 | I/O port P11 | I/O | <p>In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, these pins operate as follows:</p> <p>(1) When using 16-bit width as external data bus width</p> <ul style="list-style-type: none"> ● Accessing external memory <When reading> The value is input into high-order internal data bus (DB8 to DB15) when accessing an odd address; these pins enter high impedance state when not accessing an odd address. <When writing> Value of high-order internal data bus (DB8 to DB15) is output to these pins. ● Accessing internal memory <When reading> These pins enter high impedance state. <When writing> Value of internal data bus is output to these pins. <p>(2) When using 8-bit width as external data bus width These pins become I/O port P110 – P117.</p> |

BASIC FUNCTION BLOCKS

The M37754M6C-XXXGP and M37754M6C-XXXHP has the same functions as the M37754M8C-XXXGP and M37754M8C-XXXHP except for the following :

- (1) The ROM size is different.
 - (2) The function of ROM area modification is not available.
- Therefore, refer to the section on the M37754M8C-XXXGP.

MEMORY

The memory map is shown in Figure 1. The address space is 16 Mbytes from addresses 016 to FFFFFFF16. The address space is divided into 64-Kbyte units called banks. The banks are numbered from 016 to FF16.

Internal ROM, internal RAM, and control registers for internal peripheral devices are assigned to bank 016.

The 48-Kbyte area from addresses 400016 to FFFF16 is the internal ROM.

Addresses FFD216 to FFFF16 are the RESET and interrupt vector addresses and contain the interrupt vectors. Refer to the section on interrupts for details.

The 2048-byte area from addresses 8016 to 87F16 contains the internal RAM. In addition to storing data, the RAM is used as stack during a subroutine call, or interrupts.

Assigned to addresses 016 to 7F16 are peripheral devices such as I/O ports, A-D converter, D-A converter, UART, timer, and interrupt control registers.

A 256-byte direct page area can be allocated anywhere in bank 016 using the direct page register DPR. In direct page addressing mode, the memory in the direct page area can be accessed with two words thus reducing program steps.

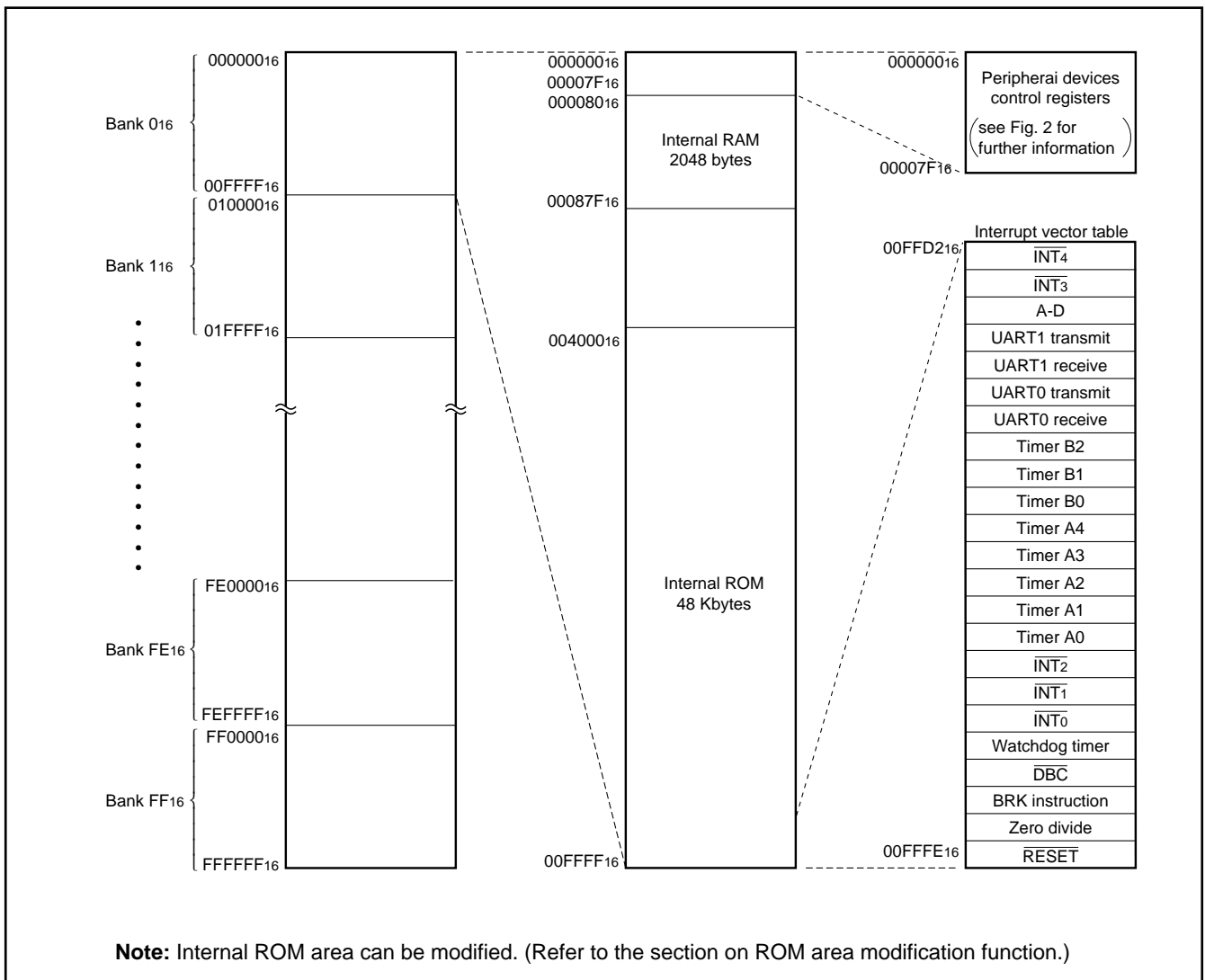


Fig. 1 Memory map

| Address (Hexadecimal notation) | | Address (Hexadecimal notation) | |
|--------------------------------|---|--------------------------------|---|
| 000000 | | 000040 | Count start register |
| 000001 | | 000041 | |
| 000002 | Port P0 register | 000042 | One-shot start register |
| 000003 | Port P1 register | 000043 | |
| 000004 | Port P0 direction register | 000044 | Up-down register |
| 000005 | Port P1 direction register | 000045 | Timer A write register |
| 000006 | Port P2 register | 000046 | Timer A0 register |
| 000007 | Port P3 register | 000047 | |
| 000008 | Port P2 direction register | 000048 | Timer A1 register |
| 000009 | Port P3 direction register | 000049 | |
| 00000A | Port P4 register | 00004A | Timer A2 register |
| 00000B | Port P5 register | 00004B | |
| 00000C | Port P4 direction register | 00004C | Timer A3 register |
| 00000D | Port P5 direction register | 00004D | |
| 00000E | Port P6 register | 00004E | Timer A4 register |
| 00000F | Port P7 register | 00004F | |
| 000010 | Port P6 direction register | 000050 | Timer B0 register |
| 000011 | Port P7 direction register | 000051 | |
| 000012 | Port P8 register | 000052 | Timer B1 register |
| 000013 | Port P9 register | 000053 | |
| 000014 | Port P8 direction register | 000054 | Timer B2 register |
| 000015 | Port P9 direction register | 000055 | |
| 000016 | Port P10 register | 000056 | Timer A0 mode register |
| 000017 | Port P11 register | 000057 | Timer A1 mode register |
| 000018 | Port P10 direction register | 000058 | Timer A2 mode register |
| 000019 | Port P11 direction register | 000059 | Timer A3 mode register |
| 00001A | Waveform output mode register | 00005A | Timer A4 mode register |
| 00001B | Dead-time timer | 00005B | Timer B0 mode register |
| 00001C | Pulse output data register 1 | 00005C | Timer B1 mode register |
| 00001D | Pulse output data register 0 | 00005D | Timer B2 mode register |
| 00001E | A-D control register 0 | 00005E | Processor mode register 0 |
| 00001F | A-D control register 1 | 00005F | Processor mode register 1 |
| 000020 | A-D register 0 | 000060 | Watchdog timer register |
| 000021 | | 000061 | Watchdog timer frequency select register |
| 000022 | A-D register 1 | 000062 | Chip select control register |
| 000023 | | 000063 | Chip select area register |
| 000024 | A-D register 2 | 000064 | Comparator function select register |
| 000025 | | 000065 | Reserved area (Note) |
| 000026 | A-D register 3 | 000066 | Comparator result register |
| 000027 | | 000067 | Reserved area (Note) |
| 000028 | A-D register 4 | 000068 | D-A register 0 |
| 000029 | | 000069 | |
| 00002A | A-D register 5 | 00006A | D-A register 1 |
| 00002B | | 00006B | |
| 00002C | A-D register 6 | 00006C | Particular function select register 0 |
| 00002D | | 00006D | Particular function select register 1 |
| 00002E | A-D register 7 | 00006E | INT4 interrupt control register |
| 00002F | | 00006F | INT3 interrupt control register |
| 000030 | UART0 transmit/receive mode register | 000070 | A-D interrupt control register |
| 000031 | UART0 baud rate register | 000071 | UART0 transmit interrupt control register |
| 000032 | UART0 transmit buffer register | 000072 | UART0 receive interrupt control register |
| 000033 | | 000073 | UART1 transmit interrupt control register |
| 000034 | UART0 transmit/receive control register 0 | 000074 | UART1 receive interrupt control register |
| 000035 | UART0 transmit/receive control register 1 | 000075 | Timer A0 interrupt control register |
| 000036 | UART0 receive buffer register | 000076 | Timer A1 interrupt control register |
| 000037 | | 000077 | Timer A2 interrupt control register |
| 000038 | UART1 transmit/receive mode register | 000078 | Timer A3 interrupt control register |
| 000039 | UART1 baud rate register | 000079 | Timer A4 interrupt control register |
| 00003A | UART1 transmit buffer register | 00007A | Timer B0 interrupt control register |
| 00003B | | 00007B | Timer B1 interrupt control register |
| 00003C | UART1 transmit/receive control register 0 | 00007C | Timer B2 interrupt control register |
| 00003D | UART1 transmit/receive control register 1 | 00007D | INT0 interrupt control register |
| 00003E | UART1 receive buffer register | 00007E | INT1 interrupt control register |
| 00003F | | 00007F | INT2 interrupt control register |

Note: Do not write to this address.

Fig. 2 Location of peripheral devices and interrupt control registers

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ELECTRICAL CHARACTERISTICS

The M37754M6C-XXXGP and M37754M6C-XXXHP have the same function as the M37754M8C-XXXGP and M37754M8C-XXXHP in the following :

- (1) ABSOLUTE MAXIMUM RATINGS
- (2) RECOMMENDED OPERATING CONDITIONS
- (3) ELECTRICAL CHARACTERISTICS
- (4) PERIPHERAL DEVICE INPUT/OUTPUT TIMING
- (5) TIMING REQUIREMENTS
- (6) SWITCHING CHARACTERISTICS

Therefore, refer to the corresponding section on the M37754M8C-XXXGP.

ADDRESSING MODES AND INSTRUCTION SET

The M37754M6C-XXXGP and M37754M6C-XXXHP have 29 powerful addressing modes; 1 addressing mode is added to the basis of the 7700 series. Refer to the "7751 Series Software Manual" for the details.

INSTRUCTION SET

The M37754M6C-XXXGP and M37754M6C-XXXHP have the extended instruction set; 6 instructions are added to the instruction set of 7700 series. The object code of this extended instruction set is upwards compatible to that of 7700 series instruction set.

Refer to the "7751 Series Software Manual" for the details.

SHORTENING NUMBER OF INSTRUCTION EXECUTION CYCLES

Shortening number of instruction execution cycles is realized in the M37754M6C-XXXGP and M37754M6C-XXXHP owing to modifications of the instruction execution algorithm and the CPU circuit, and others.

Refer to the "7751 Series Software Manual" about the number of instruction execution cycles.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders:

<M37754M6C-XXXGP>

- (1) M37754M6C-XXXGP mask ROM order confirmation form
- (2) 100P6S mark specification form
- (3) ROM data (EPROM 3 sets)

<M37754M6C-XXXHP>

- (1) M37754M6C-XXXHP mask ROM order confirmation form
- (2) 100P6Q mark specification form
- (3) ROM data (EPROM 3 sets)

**7700 FAMILY MASK ROM ORDER CONFIRMATION FORM
SINGLE-CHIP 16-BIT MICROCOMPUTER
M37754M6C-XXXGP
M37754M6C-XXXHP
MITSUBISHI ELECTRIC**

| | |
|-----------------|--|
| Mask ROM number | |
|-----------------|--|

| | | |
|---------|------------------------|----------------------|
| Receipt | Date: | |
| | Section head signature | Supervisor signature |
| | | |

Note : Please fill in all items marked ※

| | | | | | |
|------------|--------------|---------|---------------------|---------------------|------------|
| ※ Customer | Company name | TEL () | Issuance signatures | Responsible officer | Supervisor |
| | Date issued | Date: | | | |

※1. Confirmation

Specify the name of the product being ordered.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based on this data.

We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data.

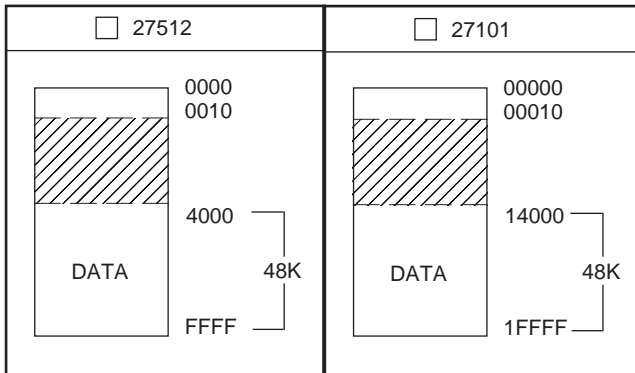
Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas

| | | | |
|--|--|--|--|
| | | | |
|--|--|--|--|

 (hexadecimal notation)

EPROM Type :



(1) Set "FF₁₆" in the shaded area.

(2) Address 0₁₆ to 10₁₆ are the area for storing the data on model designation and options. This area must be written with the data shown below.

Details for option data are given next in the section describing the STP instruction option.

Address and data are written in hexadecimal notation.

| | Address | | Address | | Address |
|--|---------|---|---------|---|-------------|
| | 4D | 0 | 43 | 8 | Option data |
| | 33 | 1 | 2D | 9 | |
| | 37 | 2 | FF | A | |
| | 37 | 3 | FF | B | |
| | 35 | 4 | FF | C | |
| | 34 | 5 | FF | D | |
| | 4D | 6 | FF | E | |
| | 36 | 7 | FF | F | |

※2. STP instruction option

One of the following sets of data should be written to the option data address (10₁₆) of the EPROM you have ordered.

Check @ in the appropriate box.

| | | |
|--|---|--------------------------|
| <input type="checkbox"/> STP instruction enable | <input type="checkbox"/> 01 ₁₆ | Address 10 ₁₆ |
| <input type="checkbox"/> STP instruction disable | <input type="checkbox"/> 00 ₁₆ | Address 10 ₁₆ |

※3. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 100P6S Mark Specification Form (for M37754M6C-XXXGP), 100P6Q Mark Specification Form (for M37754M6C-XXXHP) and attach to the Mask ROM Order Confirmation Form.

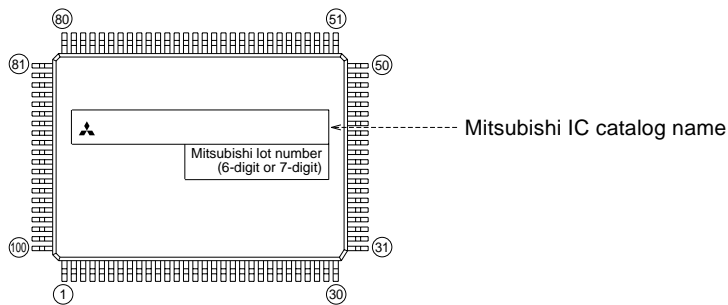
※4. Comments

100P6S (100-PIN QFP) MARK SPECIFICATION FORM

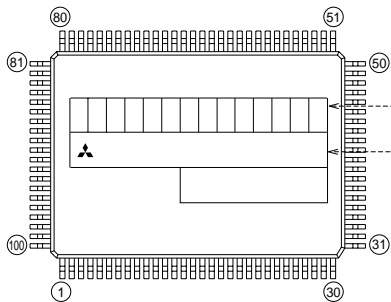
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi catalog name



Customer's Parts Number

Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note1 : The mark field should be written right aligned.

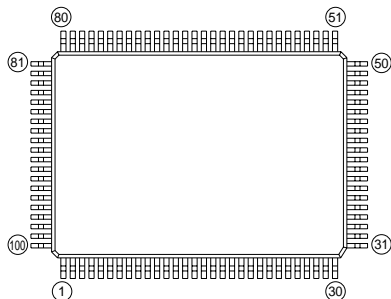
2 : The fonts and size of characters are standard Mitsubishi type.

3 : Customer's Parts Number can be up to 14 characters : Only 0 ~ 9, A ~ Z, +, -, /, (,), &, @, . (periods), , (commas) are usable.

4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

C. Special Mark Required



Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.

Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.

Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

Keep safety first in your circuit designs!

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

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REVISION DESCRIPTION LIST

M37754M6C-XXXGP/HP DATA SHEET

| Rev. No. | Revision Description | Rev. date |
|----------|--|-----------|
| 1.0 | First Edition | 971114 |
| 1.01 | The following are added: <ul style="list-style-type: none">•MASK ROM ORDER CONFIRMATION FORM•MARK SPECIFICATION FORM | 980528 |
| 2.00 | (1) For the “timer A write flag (address 45 ₁₆)”, it’s name is corrected: <ul style="list-style-type: none">• New register name: timer A write <u>register</u>• Related page: page 8 | 990428 |