



Integrated Device Technology, Inc.

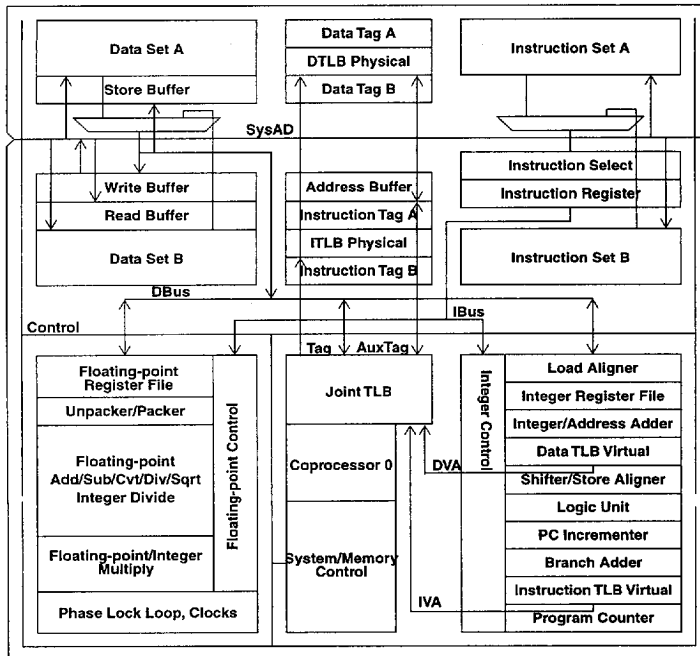
# ENHANCED ORION 64-BIT RISC MICROPROCESSOR

**ORION™**  
IDT79R4700™  
IDT79RV4700™  
Preliminary

## FEATURES

- True 64-bit microprocessor
  - 64-bit integer operations
  - 64-bit floating-point operations
  - 64-bit registers
  - 64-bit virtual address space
- High-performance microprocessor
  - 175 peak MIPS at 175MHz
  - 87 peak MFLOP/s at 175MHz
  - 132 SPECint92 at 175Mz
  - Two-way set associative caches
- Improved FPA multiply performance
  - 1 mul, 1 add every 4 clock cycles
- High level of integration
  - 64-bit integer CPU
  - 64-bit floating-point unit
  - 16KB instruction cache; 16KB data cache
  - Flexible MMU with large TLB
- Low-power operation
  - 3.3V power supply
  - 24mW/MHZ typical internal power dissipation (2.4W @ 100MHz, 3.3V)
  - Standby mode reduces internal power
- Standard operating system support includes:
  - Microsoft Windows™ NT
  - UNISOFT Unix™ System V.4
- Fully software and pin-compatible with R4600 ORION Processor Family
- Available in R4600 pin-compatible 179-pin PGA or 208-pin MQUAD
- 80-175MHz with mode bit dependent output clock frequencies
- 64GB physical address space
- Processor family for a wide variety of applications
  - Desktop workstations and PCs
  - Deskside or departmental servers
  - High-performance embedded applications (such as color printers, multi-media and internetworking.)

## BLOCK DIAGRAM



3038 drw 01

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## COMMERCIAL TEMPERATURE RANGE

JULY 1996

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**DESCRIPTION**

The IDT79R4700 Enhanced ORION 64-Bit RISC Microprocessor is a follow-on to the IDT79R4600, and is fully compatible with it. The R4700 has improved FPA multiply operations. The RV4700 is available only in 3.3V. The remaining features of the R4700 are the same.

The R4700 supports a wide variety of processor-based applications, from 32-bit Windows NT desktop or notebook systems through high-performance, 64-bit OLTP systems. Compatible with the R4600 family for both hardware and software, the R4700 will serve in many of the same applications, but, in addition supports faster floating point computation, thus improving its performance in graphics-oriented applications. It does not provide integrated secondary cache and multiprocessor support as found in the R4000SC and R4000MC, but an external secondary cache can be designed around it. The large on-chip two-way set associative caches make this unnecessary in many systems.

The R4700 brings R4400SC performance levels to the R4000PC package, while at the same time providing lower cost and lower power. It does this by providing larger on-chip caches that are two-way set associative, fewer pipeline stalls, and early restart for data cache misses. It also improves the performance of floating point multiply operations and allows 1 multiply and 1 add every 4 clock cycles. The result is >120 SPECint92 and >90 SPECfp92 (exact figures are system-dependent).

The R4700 is upwardly software compatible with the IDT79R3000™ microprocessor family, including the IDT RISC Controller™ 79R3051™/R3052™/R3041™/R3071™/R3081™ as well as the IDT79R4000 family of microprocessors. Microsoft Windows NT and UNISOFT Unix V.4 operating systems insure the availability of thousands of applications programs, geared to provide a complete solution to a large number of processing needs. An array of development tools facilitates the rapid development of

R4700-based systems, enabling a wide variety of customers to take advantage of the MIPS Open Architecture philosophy.

The 64-bit computing and addressing capability of the R4700 enables a wide variety of capabilities previously limited by a smaller address space. For example, the large address space allows operating systems with extensive file mapping; direct access to large files can occur without explicit I/O calls. Applications such as large CAD databases, multi-media, and high-quality image storage and retrieval all directly benefit from the enlarged address space.

This data sheet provides an overview of the features and architecture of the R4700 CPU. A more detailed description of the processor appears in the *IDT79R4600 and IDT79R4700 RISC Processor Hardware User's Manual*, available from IDT. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

**DATA SHEET REVISION HISTORY**

**Changes to version dated January 1996:**

Deleted data on 150MHz speed for 5V part only.

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**General Purpose Registers**

63	0
0	
r1	
r2	
•	
•	
•	
•	
r29	
r30	
r31	

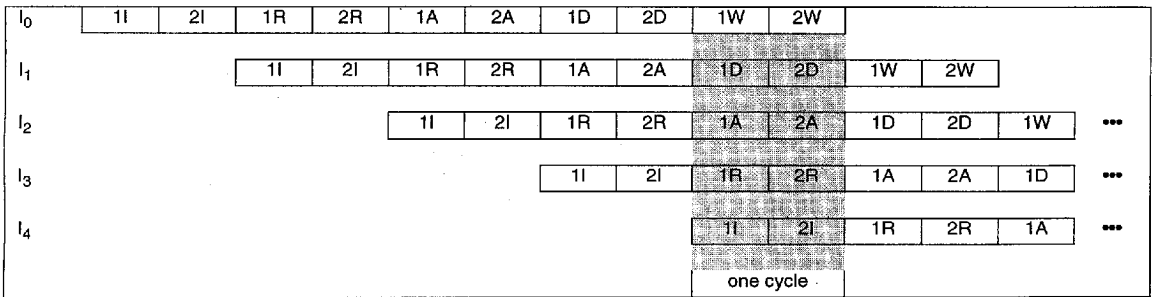
**Multiply/Divide Registers**

63	0
HI	
63	0
LO	

**Program Counter**

63	0
PC	

Figure 1. CPU Registers



**Key to Figure**

- 1I-1R Instruction cache access
- 2I Instruction virtual to physical address translation in ITLB
- 2A-2D Data cache access and load align
- 1D Data virtual to physical address translation in DTLB
- 1D-2D Virtual to physical address translation in JTLB
- 2R Register file read
- 2R Bypass calculation
- 2R Instruction decode
- 2R Branch address calculation
- 1A Issue or slip decision
- 1A-2A Integer add, logical, shift
- 1A Data virtual address calculation
- 2A Store align
- 1A Branch decision
- 2W Register file write

Figure 2. R4700 Pipeline

**HARDWARE OVERVIEW**

The R4700 family brings a high-level of integration designed for high-performance computing. The key elements of the R4700 are briefly described below. A more detailed description of each of these subsystems is available in the User's Manual.

**Pipeline**

The R4700 uses a 5-stage pipeline similar to the IDT79R3000. The simplicity of this pipeline allows the R4700 to be lower cost and lower power than super-scalar or super-pipelined processors. Unlike the R3000, the R4700 does virtual-to-physical translation in parallel with cache access. This allows the R4700 to operate at over three times the frequency of the R3000 and to support a larger TLB for address translation.

Compared to the 8-stage R4000 pipeline, the R4700 is more efficient, because it requires fewer stalls. Figure 2 shows the R4700 pipeline.

**Integer Execution Engine**

The R4700 implements the MIPS Instruction Set architecture, and thus is fully upward compatible with applications running on the earlier generation parts. The R4700 includes the same additions to the instruction set as found in the R4000 family of microprocessors, targeted at improving performance and capability while maintaining binary compatibility with earlier processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability among implementations of the MIPS instruction set architecture.

In addition to the instruction extensions detailed above, new instructions defined in the R4600 that take advantage of the 64-bit architecture of the processor are also incorporated into the R4700. The R4700 is fully software-compatible with the R4600. When operating as a 32-bit processor, the R4700 will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The register resources include: 32 general-purpose orthogonal integer registers, the HI/LO result registers for the integer multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

#### Register File

The R4700 has 32 general-purpose registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

#### ALU

The R4700 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all logical and shift operations. Each of these units is highly optimized and can perform an operation in a single pipeline cycle.

#### Integer Multiply/Divide

The R4700 uses the floating-point unit to perform integer multiply and divide. The results of the operation are placed in the *HI* and *LO* registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions. Table 1 shows the number of processor internal cycles required between an integer multiply or divide and a subsequent MFHI or MFLO operation, in order that no interlock or stall occurs. The R4700 performs an integer multiply faster than the R4600 by 2 clock cycles. However, it takes the same number of clock cycles for integer division.

Operation	32-bit	64-bit
MULT	6 - 9	7 - 10
DIV	42	74

Table 1. Integer Multiply/Divide Cycles

#### Floating-Point Co-Processor

The R4700 incorporates an entire floating-point co-processor on chip, including a floating-point register file and execution units. The floating-point co-processor forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit. The floating point coprocessor of the R4700 has improved the floating multiply operations compared to the R4600. This improves the peak MFLOPS to be equal to half of the pipeline clock rate.

#### Floating-Point Units

The R4700 floating-point execution units supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipe-

lined, allowing a new multiply to begin every 4 cycles.

As in the IDT79R3010A and IDT79R4000, the R4700 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments and highly desirable for debugging in any environment.

The floating-point unit operation's set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. These operations comply with the IEEE Standard 754. The floating point unit improves the multiply compared to the R4600 by performing a single precision multiply in 4 clock cycles and a double precision multiply in 5 clock cycles.

Table 2 gives the latencies of some of the floating-point instructions in internal processor cycles. Note that multiplies are pipelined, so that a new multiply can be initiated every 4 pipeline cycles

#### Floating-Point General Register File

The floating-point register file is made up of thirty-two 64-bit registers. With the LDC1 and SDC1 instructions the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store double-word instruction in every cycle.

The floating-point control register space contains two registers; one for determining configuration and revision information for the coprocessor and one for control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	4	5
DIV	32	61
SQRT	31	60
CMP	3	3
FIX	4	4
FLOAT	6	6
ABS	1	1
MOV	1	1
NEG	1	1
LWC1, LDC1	2	2
SWC1, SDC1	1	1

Table 2. Floating-Point Cycles

**System Control Co-processor (CP0)**

The system control co-processor in the MIPS architecture is responsible for the virtual memory sub-system, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent. The R4700 CP0 is identical to that of the R4600.

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction address translation buffer (the ITLB), a data address translation buffer (the DTLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

**System Control Co-Processor Registers**

The R4700 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined and changed, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the R4700 includes registers to implement a real-time cycle counting facility, to aid in cache diagnostic testing, and to assist in data error detection. Figure 3 shows the CP0 registers.

**Virtual-to-Physical Address Mapping**

The R4700 provides the user, supervisor, and kernel modes of virtual addressing, which is available to system software to provide a secure environment for user processes.

Bits in a status register determine which virtual addressing mode is used. While in user mode, the R4700 provides a single, uniform virtual address space of 256GB (2GB for 32-bit address mode).

When operating in the kernel mode, four distinct virtual address spaces—totalling 1024GB (4GB in 32-bit address mode)—are simultaneously available and are differentiated by the high-order bits of the virtual address.

The R4700 processor also supports a supervisor mode in which the virtual address space is 256.5GB (2.5GB in 32-bit address mode), divided into three regions based on the high-order bits of the virtual address. If the R4700 is configured for 64-bit virtual addressing, the virtual address space layout is an upward compatible extension of the 32-bit virtual address space layout. Figure 4 on page 6 shows the address space layout for the 32-bit virtual address operation.

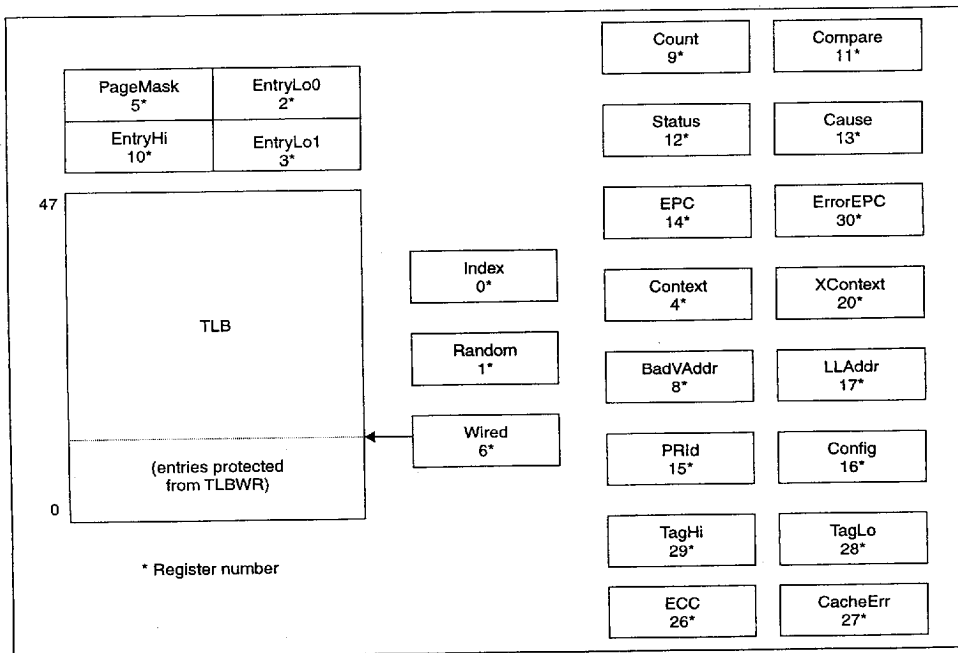


Figure 3. The R4700 CP0 Registers

**Joint TLB**

For fast virtual-to-physical address decoding, the R4700 uses a large, fully associative TLB which maps 96 Virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64GB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space, and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when a new entry is written. Thus, operating systems can provide special purpose maps; for example, a typical frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement algorithm when a TLB miss occurs. The R4700 provides a random replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB, and thus avoid being randomly replaced. This facilitates the design of real-time systems, by allowing deterministic access to critical software.

The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is: uncached, non-coherent write-back, non-coherent write-through write-allocate, non-coherent write-through no write-allocate. Non-coherent write-back is typically used for both code and data on the R4700; the write-through modes support more efficient frame buffer accesses than the R4000 family; cache coherency is not supported, however.

**Instruction TLB**

The R4700 also incorporates a two-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation, the least-recently used ITLB entry is filled from the JTLB. The operation of the ITLB is invisible to the user.

**Data TLB**

The R4700 also incorporates a four-entry data TLB. Each entry maps a 4KB page. The data TLB improves performance by allowing data address translation to occur in parallel with data address translation. When a miss occurs on an data address translation, the DTLB is filled from the JTLB. The DTLB refill is pseudo-LRU: the least recently used entry of the least recently used half is filled. The operation of the DTLB is invisible to the user.

Furthermore, the large two-way set-associative caches increase emulation performance of DOS and Windows 3.1 applications when running under Windows NT.

0xFFFFFFFF	Kernel virtual address space (kseg3) Mapped, 0.5GB
0xE0000000	
0xDFFFFFFF	Supervisor virtual address space (sseg) Mapped, 0.5GB
0xC0000000	
0xBFFFFFFF	Uncached kernel physical address space (kseg1) Unmapped, 0.5GB
0xA0000000	
0x9FFFFFFF	Cached kernel physical address space (kseg0) Unmapped, 0.5GB
0x80000000	
0x7FFFFFFF	User virtual address space (useg) Mapped, 2.0GB
0x00000000	

Figure 4. Kernel Mode Virtual Addressing (32-bit Mode)

**Cache Memory**

In order to keep the R4700's high-performance pipeline full and operating efficiently, the R4700 incorporates on-chip instruction and data caches that can be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel. The cache subsystem is the same as for the R4600.

**Instruction Cache**

The R4700 incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with word parity.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed in a single processor cycle. Instruction fetches require only 32 bits per cycle, for a peak instruction bandwidth of 700MB/sec at 175MHz. Sequential accesses take advantage of the 64-bit fetch to reduce power dissipation, and cache miss refill writes 64 bits-per-cycle to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize performance.

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### Data Cache

For fast, single cycle data access, the R4700 includes a 16KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

The normal write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can however select write-through on a per-page basis when it is appropriate, such as for frame buffers.

Associated with the data cache is the store buffer. When the R4700 executes a Store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the data cache in the next cycle that the data cache is not accessed (the next non-load cycle). The store buffer allows the R4700 to execute a store every processor cycle and to perform back-to-back stores without penalty.

### Write Buffer

Writes to external memory, whether cache miss writebacks, stores to uncached, or write-through addresses, use the on-chip write buffer. The write buffer holds up to four 64-bit address and 64-bit data pairs. The entire buffer is used for a data cache writeback and allows the processor to proceed in parallel with memory update. For uncached and write-through stores, the write buffer significantly increases performance over the R4000 family of processors.

### System Interface

The R4700 supports a 64-bit system interface that is compatible with the R4000PC system interface. This interface operates from two clocks provided by the R4700, TClock[1:0] and RClock[1:0], at some division of the internal clock.

The system interface consists of a 64-bit Address/Data bus with eight check bits and a 9-bit command bus protected with parity. In addition, there are eight handshake signals and 6 interrupt inputs. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 700MB/sec at 175MHz.

Figure 5 shows a typical system using the R4700. In this example two banks of DRAM are used to supply and accept data with a DDxxDD data pattern.

### System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4700 and the rest of the system. It is protected with an 8-bit parity check bus, SysADC.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The data rate and the bus frequency at which the R4700 transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no read or write buffering or a faster, high performance interface can be designed to communicate with the R4700. Again, the system designer has the flexibility to make these price/performance trade-offs.

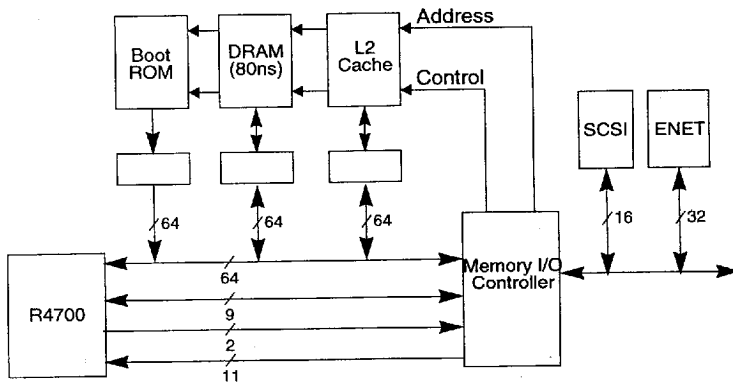


Figure 5. Desktop System Block Diagram

### System Command Bus

The R4700 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this data line is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4700. Processor requests are initiated by the R4700 and responded to by an external device. External requests are issued by an external device and require the R4700 to respond.

The R4700 supports one to eight byte and block transfers on the SysAD bus. In the case of a sub-doubleword transfer, the low-order three address bits give the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

### Handshake Signals

There are six handshake signals on the system interface. Two of these, RdRdy\* and WrRdy\* are used by an external device to indicate to the R4700 whether it can accept a new read or write transaction. The R4700 samples these signals before deasserting the address on read and write requests.

ExtRqst\* and Release\* are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts ExtRqst\*. The R4700 responds by asserting Release\* to release the system interface to slave state.

ValidOut\* and ValidIn\* are used by the R4700 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4700 asserts ValidOut\* when it is driving these buses with a valid command or data, and the external device drives ValidIn\* when it has control of the buses and is driving a valid command or data.

### Non-overlapping System Interface

The R4700 uses a non-overlapping system interface, compatible with the R4600. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4700 issues another request. The R4700 can issue read and write requests to an external device, and an external device can issue read and write requests to the R4700.

For processor read transaction the R4700 asserts ValidOut\* and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has RdRdy\* asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting Release\*. The external device can then begin sending the data.

Figure 6 shows a processor block read request and the external agent read response. The read latency is four cycles (ValidOut\* to ValidIn\*), and the response data pattern is DDxxDD. Figure 7 shows a processor block write.

### Write Reissue and Pipeline Write

The R4600 and the R4700 implement additional write protocols designed to improve performance. This implementation doubles the effective write bandwidth. The write re-issue has a high repeat rate of two cycles per write. A write issues if WrRdy\* is asserted two cycles earlier and is still asserted at the issue cycle. If it is not still asserted, the last write re-issues again. Pipelined writes have the same two cycle per write repeat rate but can issue one additional write after WrRdy\* de-asserts. They still follow the issue rule as R4x00 mode for other writes.

### External Requests

The R4700 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4700 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue requests to the processor, such as a request for the R4700 to write to the R4700 interrupt register. The R4700 supports Write, Null, and Read Response external requests.

### Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (MasterClock divided by 256). The low-frequency operation allows the initialization information to be kept in a low-cost serial EEPROM; alternatively the 20-or-so bits could be generated by the system interface ASIC or a simple PAL.

Immediately after the Vccok signal is asserted, the processor reads a bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

### JTAG Interface

For compatibility with the R4000PC, the R4700 supports the JTAG interface pins, with the serial input connected to serial output. Boundary scan is not supported.

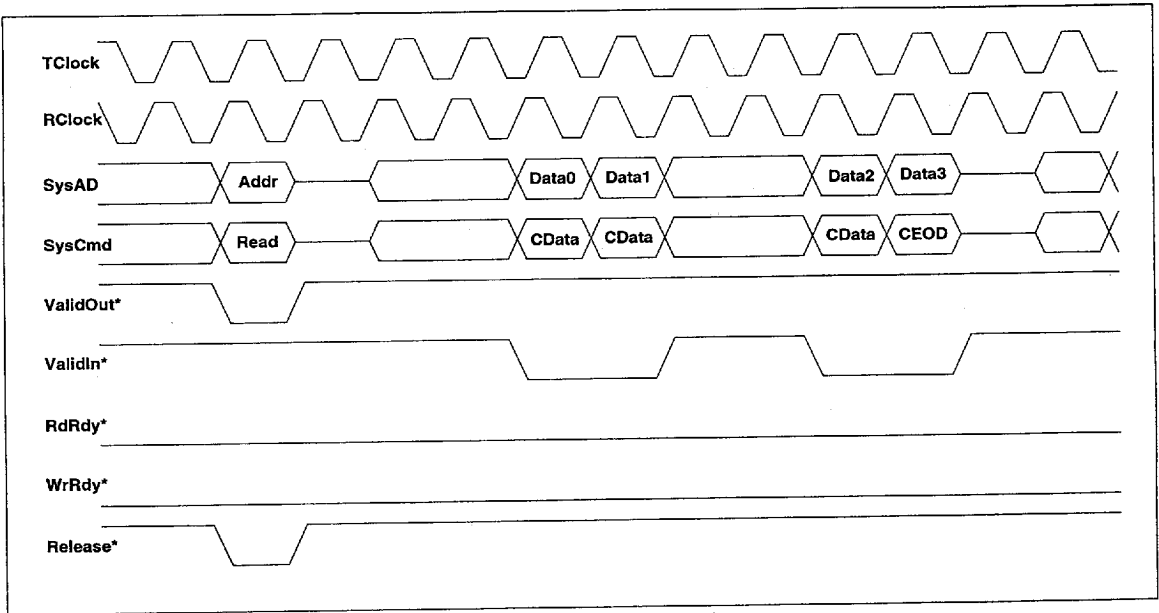


Figure 6. Processor Block Read

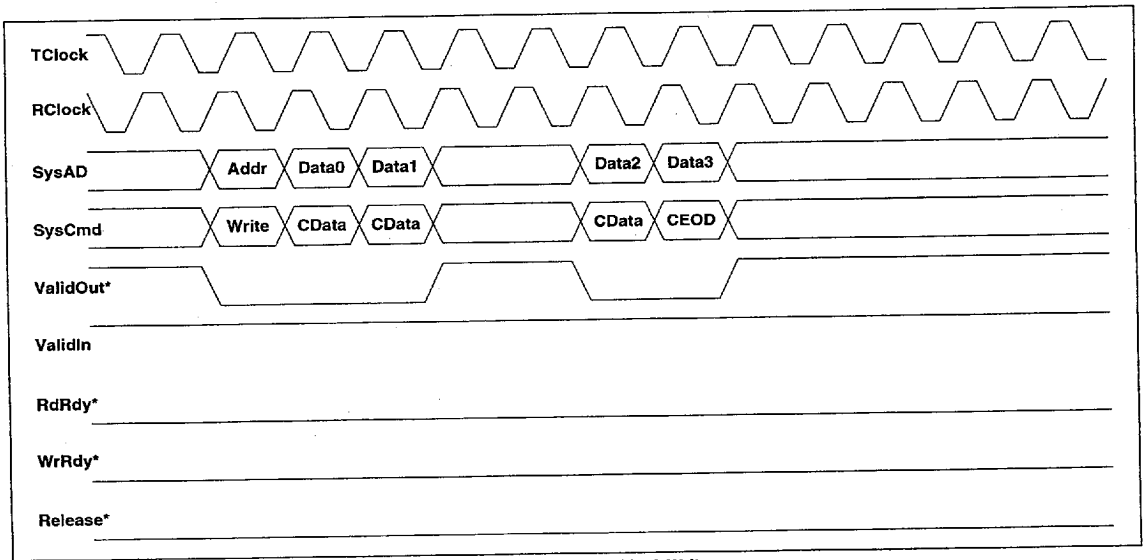


Figure 7. Processor Block Write

**Boot-Time Modes**

The boot-time serial mode stream is defined in Table 3. Bit 0 is the bit presented to the processor when V<sub>CCOK</sub> is asserted; bit 255 is the last.

**Power Management**

CP0 is also used to control the power management for the R4700. This is the standby mode and can be used to reduce the power consumption of the internal core of the CPU. Standby mode is entered by executing the WAIT instruction with the SysAD bus idle and is exited by an interrupt.

Mode bit	Description	Mode bit	Description
0	reserved (must be zero)	14..13	Output driver strength 10 → 100% strength (fastest), 11 → 83% strength, 00 → 67% strength, 01 → 50% strength (slowest)
4..1	Writeback data rate 0 → Δ, 1 → DDx, 2 → DDxx, 3 → Dx Dx, 4 → DDxxx, 5 → DDxxxx, 6 → DxxDxx, 7 → DDxxxxxx, 8 → DxxxDxxx, 9-15 reserved	bit 15	0 -> TClock[0] enabled 1 -> TClock[0] disabled
7..5	Clock divisor 0 → 2, 1 → 3, 2 → 4, 3 → 5, 4 → 6, 5 → 7, 6 → 8, 7 reserved	bit 16	0 -> TClock[1] enabled 1 -> TClock[1] disabled
8	0 → Little endian, 1 → Big endian	bit 17	0 -> RClock[0] enabled 1 -> RClock[0] disabled
10..9	00 → R4000 compatible, 01 → reserved, 10 → pipelined writes, 11 → write re-issue	bit 18	0 -> RClock[1] enabled 1 -> RClock[1] disabled
11	Disable the timer interrupt on Int[5]. 0 → Enabled 1 → Disabled	255..19	Reserved (must be zero)
12	reserved (must be zero)		

Table 3. Boot Time Mode Stream

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## PIN DESCRIPTION

Table 4 is a list of interface, interrupt, and miscellaneous pins available on the R4700. Signals marked with one asterisk are active when low. For compatibility with the R4600, the R4700 supports the JTAG interface pins, with the serial input connected to serial output. Boundary scan is not supported.

Pin Name	Type	Description
<b>System Interface</b>		
ExtRqst*	Input	External request Signals that the system interface needs to submit an external request.
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	Reserved system command/data identifier bus parity for the R4700 unused on input and zero on output.
<b>Clock/Control Interface</b>		
MasterClock	Input	Master clock Master clock input at one half the processor operating frequency.
MasterOut	Output	Master clock out Master clock output aligned with MasterClock.
RClock(1:0)	Output	Receive clocks Two identical receive clocks at the system interface frequency.
TClock(1:0)	Output	Transmit clocks Two identical transmit clocks at the system interface frequency.
IOOut	Output	Reserved for future output Always HIGH.
IOIn	Input	Reserved for future input Should be driven HIGH.
SyncOut	Output	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn	Input	Synchronization clock in Synchronization clock input. See SyncOut.
Fault*	Output	Fault Always HIGH.
VccP	Input	Quiet Vcc for PLL Quiet Vcc for the internal phase locked loop.

Table 4. Pin Descriptions (Page 1 of 2)

Pin Name	Type	Description
VssP	Input	Quiet Vss for PLL Quiet Vss for the internal phase locked loop.
<b>Interrupt Interface</b>		
Int*(5:0)	Input	Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.
<b>Initialization Interface</b>		
Vccok	Input	Vcc is OK When asserted, this signal indicates to the R4700 that the 3.3V (5.0V) power supply has been above 3.0V (4.5V) for more than 100 milliseconds and will remain stable. The assertion of Vccok initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of ColdReset. ColdReset must be de-asserted synchronously with MasterOut.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterOut.
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.

Table 4. Pin Descriptions (Page 2 of 2)

## STANDBY MODE OPERATIONS

The R4700 provides a means to reduce the amount of power consumed by the internal core when the CPU would otherwise not be performing any useful operations. This is known as "Standby Mode".

### Entering Standby Mode

Executing the WAIT instruction enables interrupts and enters Standby mode. When the WAIT instruction finishes the W pipe-stage, if the SysAd bus is currently idle, the internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, some of the input pin clocks (Int[5:0]\*, NMI\*, ExtReq\*, Reset\*, and Cold-Reset\*), and the output clocks—TClock[1:0], RClock[1:0] SyncOut, Modeclock and MasterOut—will continue to run. If the conditions are not correct when the WAIT instruction finishes the W pipe-stage (such as the SysAd bus is not idle), the WAIT is treated as a NOP.

Once the CPU is in Standby Mode, any interrupt—including the internally generated timer interrupt—will cause the CPU to exit Standby Mode.

## THERMAL CONSIDERATIONS

The R4700 utilizes special packaging techniques to improve the thermal properties of high-speed processors. The R4700 is packaged using cavity down packaging in a 179-pin PGA package with integral thermal slug, and a 208-lead MQUAD QFP package. These packages effectively dissipate the power of the CPU, increasing device reliability.

The R47000 utilizes the MQUAD package (the "MS" package), which is an all-aluminum package with the die attached to a normal copper lead frame mounted to the aluminum casing. Due to the heat-spreading effect of the aluminum, the package allows for an efficient thermal transfer between the die and the case. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation.

The R4700 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature,  $T_A$ , can be calculated using the thermal resistance from case to ambient ( $\theta_{CA}$ ) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \theta_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum ICC specification for the device.

Typical values for  $\theta_{CA}$  at various airflows are shown in Table 5.

Airflow (ft/min)	$\theta_{CA}$					
	0	200	400	600	800	1000
PGA	16	7	5	3	2.5	2
MQUAD	20	12	9	8	7	6

Table 5. Thermal Resistance ( $\theta_{CA}$ ) at Various Airflows

**Note:** The R4700 implements advanced power management to substantially reduce the average power dissipation of the device. This operation is described in the *IDT79R4600 & R4700 ORION Processor Hardware User's Manual*.

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	RV4700 3.3V±5%	R4700 5.0V±5%	Unit
		Commercial	Commercial	
V <sub>TERM</sub>	Terminal Voltage with respect to GND	-0.5 <sup>(2)</sup> to +4.6	-0.5 <sup>(2)</sup> to +7.0	V
T <sub>C</sub>	Operating Temperature (case)	0 to +85	0 to +85	°C
T <sub>BIAS</sub>	Case Temperature Under Bias	-55 to +125	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-55 to +125	°C
I <sub>IN</sub>	DC Input Current	20 <sup>(3)</sup>	20 <sup>(3)</sup>	mA
I <sub>OUT</sub>	DC Output Current	50	50 <sup>(4)</sup>	mA

## Notes:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>IN</sub> minimum = -2.0V for pulse width less than 15ns. V<sub>IN</sub> should not exceed V<sub>CC</sub> +0.5 Volts.
- When V<sub>IN</sub> < 0V or V<sub>IN</sub> > V<sub>CC</sub>
- Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

## RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	RV4700	R4700
			V <sub>CC</sub>	V <sub>CC</sub>
Commercial	0°C to +85°C (Case)	0V	3.3V±5%	5.0V±5%

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## DC ELECTRICAL CHARACTERISTICS—R4700

(V<sub>CC</sub> = 5.0±5%, T<sub>CASE</sub> = 0°C to +85°C)

Parameter	R4700 80 MHz		R4700 100MHz		R4700 133MHz		Conditions
	Min	Max	Min	Max	Min	Max	
V <sub>OL</sub>	—	0.1V	—	0.1V	—	0.1V	I <sub>OUT</sub> = 20uA
V <sub>OH</sub>	V <sub>CC</sub> - 0.1V	—	V <sub>CC</sub> - 0.1V	—	V <sub>CC</sub> - 0.1V	—	
V <sub>OL</sub>	—	0.4V	—	0.4V	—	0.4V	I <sub>OUT</sub> = 4mA
V <sub>OH</sub>	3.5V	—	3.5V	—	3.5V	—	
V <sub>IL</sub>	-0.5V	0.8V	-0.5V	0.8V	-0.5V	0.8V	—
V <sub>IH</sub>	2.0V	V <sub>CC</sub> + 0.5V	2.0V	V <sub>CC</sub> + 0.5V	2.0V	V <sub>CC</sub> + 0.5V	—
I <sub>IN</sub>	—	±10uA	—	±10uA	—	±10uA	0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
C <sub>IN</sub>	—	15pF	—	15pF	—	15pF	—
C <sub>OUT</sub>	—	15pF	—	15pF	—	15pF	—
I <sub>O</sub> LEAK	—	20uA	—	20uA	—	20uA	Input/Output Leakage

## POWER CONSUMPTION—R4700

Parameter	R4700 80 MHz		R4700 100MHz		R4700 133MHz		Conditions	
	Typical	Max	Typical <sup>(9)</sup>	Max	Typical <sup>(9)</sup>	Max		
System Condition:	80/20 MHz		100/25MHz		133/33MHz		—	
I <sub>CC</sub>	standby	—	150mA	—	175mA	—	225mA	C <sub>L</sub> = 0pF <sup>(8)</sup>
		—	215mA	—	250mA	—	325mA	C <sub>L</sub> = 50pF
	active	750mA	850 mA	875mA	1000mA	1175mA	1300mA	C <sub>L</sub> = 0pF No SysAd activity <sup>(8)</sup>
		850mA	1050mA	975mA	1200mA	1275mA	1500mA	C <sub>L</sub> = 50pF R4x00 compatible writes T <sub>C</sub> = 25°C
	850mA	1250mA	975mA	1400mA	1275mA	1675mA	C <sub>L</sub> = 50pF Pipelined writes or write re-issue T <sub>C</sub> = 25°C <sup>(8)</sup>	

**AC ELECTRICAL CHARACTERISTICS—R4700** $(V_{CC}=5.0V \pm 5\%; T_{CASE} = 0^{\circ}C \text{ to } +85^{\circ}C)$ **Clock Parameters—R4700**

Parameter	Symbol	Test Conditions	R4700 80MHz		R4700 100MHz		R4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
MasterClock HIGH	$t_{MCHIGH}$	Transition $\leq 5ns$	4	—	4	—	3	—	ns
MasterClock LOW	$t_{MCLow}$	Transition $\leq 5ns$	4	—	4	—	3	—	ns
MasterClock Frequency <sup>(5)</sup>	—	—	25	40	25	50	25	67	MHz
MasterClock Period	$t_{MCP}$	—	25	40	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{Jitterin}^{(8)}$	—	—	$\pm 250$	—	$\pm 250$	—	$\pm 250$	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}^{(8)}$	—	—	$\pm 500$	—	$\pm 500$	—	$\pm 500$	ps
MasterClock Rise Time	$t_{MCRise}^{(8)}$	—	—	5.5	—	5	—	4	ns
MasterClock Fall Time	$t_{MCFall}^{(8)}$	—	—	5.5	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	$256 \cdot t_{MCP}$	—	$256 \cdot t_{MCP}$	—	$256 \cdot t_{MCP}$	ns
JTAG Clock Period	$t_{JTAGCKP}$	—	—	$4 \cdot t_{MCP}$	—	$4 \cdot t_{MCP}$	—	$4 \cdot t_{MCP}$	ns

## NOTES:

5. Operation of the R4700 is only guaranteed with the Phase Lock Loop enabled.
6. Timings are measured from 1.5V of the clock to 1.5V of the signal.
7. Capacitive load for all output timings is 50pF.
8. Guaranteed by Design.
9. Typical integer instruction mix and cache miss rates.

SYSTEM INTERFACE PARAMETERS—R4700<sup>(6)</sup>

Parameter	Symbol	Test Conditions	R4700 80MHz		R4700 100MHz		R4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output <sup>(7)</sup>	$t_{DO}$	mode <sub>14..13</sub> = 10 (fastest)	1.0	9	1.0	9	1.0	9	ns
		mode <sub>14..13</sub> = 01 (slowest)	2.0	15	2.0	15	2.0	12	ns
Data Setup	$t_{DS}$	$t_{rise} = 5ns$	3.5	—	3.5	—	3.5	—	ns
Data Hold	$t_{DH}$	$t_{fall} = 5ns$	1.5	—	1.5	—	1.5	—	ns

## BOOT TIME INTERFACE PARAMETERS—R4700

Parameter	Symbol	Test Conditions	R4700 80MHz		R4700 100MHz		R4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	$t_{DS}$	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	$t_{DH}$	—	0	—	0	—	0	—	Master Clock Cycle

## CAPACITIVE LOAD DERATION—R4700

Parameter	Symbol	R4700 80MHz		R4700 100MHz		R4700 133MHz		Units
		Min	Max	Min	Max	Min	Max	
Load Derate	$C_{LD}$	—	2	—	2	—	2	ns/25pF

## DC ELECTRICAL CHARACTERISTICS—RV4700

(V<sub>CC</sub> = 3.3±5%, T<sub>CASE</sub> = 0°C to +85°C)

Parameter	RV4700 80 MHz		RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		RV4700 175MHz		Conditions
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OL</sub>	—	0.1V	—	0.1V	—	0.1V	—	0.1V	—	0.1V	I <sub>OUT</sub>   = 20uA
V <sub>OH</sub>	V <sub>CC</sub> - 0.1V	—	V <sub>CC</sub> - 0.1V	—	V <sub>CC</sub> - 0.1V	—	V <sub>CC</sub> - 0.1V	—	V <sub>CC</sub> - 0.1V	—	
V <sub>OL</sub>	—	0.4V	—	0.4V	—	0.4V	—	0.4V	—	0.4V	I <sub>OUT</sub>   = 4mA
V <sub>OH</sub>	2.4V	—	2.4V	—	2.4V	—	2.4V	—	2.4V	—	
V <sub>IL</sub>	-0.5V	0.2V <sub>CC</sub>	-0.5V	0.2V <sub>CC</sub>	-0.5V	0.2V <sub>CC</sub>	-0.5V	0.2V <sub>CC</sub>	-0.5V	0.2V <sub>CC</sub>	—
V <sub>IH</sub>	0.7V <sub>CC</sub>	V <sub>CC</sub> + 0.5V	0.7V <sub>CC</sub>	V <sub>CC</sub> + 0.5V	0.7V <sub>CC</sub>	V <sub>CC</sub> + 0.5V	0.7V <sub>CC</sub>	V <sub>CC</sub> + 0.5V	0.7V <sub>CC</sub>	V <sub>CC</sub> + 0.5V	—
V <sub>OHC</sub>	—	—	—	—	—	—	—	—	—	—	—
V <sub>ILC</sub>	—	—	—	—	—	—	—	—	—	—	—
V <sub>IHC</sub>	—	—	—	—	—	—	—	—	—	—	—
C <sub>IN</sub>	—	15pF	—	15pF	—	15pF	—	15pF	—	15pF	—
C <sub>OUT</sub>	—	15pF	—	15pF	—	15pF	—	15pF	—	15pF	—
I/O <sub>LEAK</sub>	—	20uA	—	20uA	—	20uA	—	20uA	—	20uA	Input/Output Leakage

## POWER CONSUMPTION—RV4700

Parameter	RV4700 80MHz		RV4700 100MHz		RV4700 133MHz		Conditions	
	Typical (9)	Max	Typical (9)	Max	Typical (9)	Max		
System Condition	80/20MHz		100/25MHz		133/33MHz		—	
I <sub>CC</sub>	standby	—	110mA	—	125mA	—	175mA	C <sub>L</sub> = 0pF <sup>(8)</sup>
		—	150mA	—	175mA	—	225mA	C <sub>L</sub> = 50pF
	active	500mA	750mA	575mA	875mA	775mA	1150mA	C <sub>L</sub> = 0pF No SysAd activity <sup>(8)</sup>
		575mA	975mA	650mA	1100mA	850mA	1375mA	C <sub>L</sub> = 50pF R4x00 compatible writes T <sub>C</sub> = 25°C
	575mA	1100mA	650mA	1275mA	850mA	1525mA	C <sub>L</sub> = 50pF Pipelined writes or write re-issue, T <sub>C</sub> = 25°C <sup>(8)</sup>	

Parameter	RV4700 150MHz		RV4700 175MHz		Conditions	
	Typical (9)	Max	Typical (9)	Max		
System Condition	150/38MHz		175/44MHz		—	
I <sub>CC</sub>	standby	—	200mA	—	200mA	C <sub>L</sub> = 0pF <sup>(8)</sup>
		—	250mA	—	250mA	C <sub>L</sub> = 50pF
	active	875mA	1300mA	1025mA	1500mA	C <sub>L</sub> = 0pF, No SysAd activity <sup>(8)</sup>
		950mA	1550mA	1200mA	1800mA	C <sub>L</sub> = 50pF R4x00 compatible writes T <sub>C</sub> = 25°C
	950mA	1725mA	1200mA	2000mA	C <sub>L</sub> = 50pF Pipelined writes or write re-issue, T <sub>C</sub> = 25°C <sup>(8)</sup>	

## AC ELECTRICAL CHARACTERISTICS — RV4700

 $(V_{CC}=3.3V \pm 5\%; T_{CASE} = 0^{\circ}C \text{ to } +85^{\circ}C)$ 

## Clock Parameters

Parameter	Symbol	Test Conditions	RV4700 80 MHz		RV4700 100MHz		RV4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
MasterClock HIGH	$t_{MCHIGH}$	Transition $\leq 5ns$	4	—	4	—	3	—	ns
MasterClock LOW	$t_{MCLOW}$	Transition $\leq 5ns$	4	—	4	—	3	—	ns
MasterClock Frequency <sup>(5)</sup>	—	—	25	40	25	50	25	67	MHz
MasterClock Period	$t_{MCP}$	—	25	40	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}^{(8)}$	—	—	$\pm 250$	—	$\pm 250$	—	$\pm 250$	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}^{(8)}$	—	—	$\pm 500$	—	$\pm 500$	—	$\pm 500$	ps
MasterClock Rise Time	$t_{MCRise}^{(8)}$	—	—	5.5	—	5	—	4	ns
MasterClock Fall Time	$t_{MCFall}^{(8)}$	—	—	5.5	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256*	—	256*	—	256*	ns
				$t_{MCP}$		$t_{MCP}$		$t_{MCP}$	

Parameter	Symbol	Test Conditions	RV4700 150MHz		RV4700 175MHz		Units
			Min	Max	Min	Max	
MasterClock HIGH	$t_{MCHIGH}$	Transition $\leq 5ns$	3	—	3	—	ns
MasterClock LOW	$t_{MCLOW}$	Transition $\leq 5ns$	3	—	3	—	ns
MasterClock Frequency <sup>(10)</sup>	—	—	25	75	25	87.5	MHz
MasterClock Period	$t_{MCP}$	—	13.3	40	11.4	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}^{(8)}$	—	—	$\pm 250$	—	$\pm 250$	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}^{(8)}$	—	—	$\pm 500$	—	$\pm 500$	ps
MasterClock Rise Time	$t_{MCRise}^{(8)}$	—	—	3.5	—	3.5	ns
MasterClock Fall Time	$t_{MCFall}^{(8)}$	—	—	3.5	—	3.5	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256*	—	256*	ns
				$t_{MCP}$		$t_{MCP}$	

10. Operation of the RV4700 is only guaranteed with the Phase Lock Loop enabled.

SYSTEM INTERFACE PARAMETERS—RV4700<sup>(6)</sup>

Parameter	Symbol	Test Conditions	RV4700 80MHz		RV4700 100MHz		RV4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output <sup>(7)</sup>	$t_{DM} = \text{Min}$	mode <sub>14..13</sub> = 10 (fastest)	1.0	9	1.0	9	1.0	9	ns
	$t_{DO} = \text{Max}$	mode <sub>14..13</sub> = 01 (slowest)	2.0	15	2.0	15	2.0	12	
Data Setup	$t_{DS}$	$t_{rise} = 3\text{ns}$	3.5	—	3.5	—	3.5	—	ns
Data Hold	$t_{DH}$	$t_{fall} = 3\text{ns}$	1.5	—	1.5	—	1.5	—	ns

Parameter	Symbol	Test Conditions	RV4700 150MHz		RV4700 175MHz	
			Min	Max	Min	Max
Data Output <sup>(7)</sup>	$t_{DM} = \text{Min}$	mode <sub>14..13</sub> = 10 (fastest)	1.0	8	1.0	8
	$t_{DO} = \text{Max}$	mode <sub>14..13</sub> = 01 (slowest)	2.0	12	2.0	12
Data Setup	$t_{DS}$	$t_{rise} = 3\text{ns}$	3.5	—	3.5	—
Data Hold	$t_{DH}$	$t_{fall} = 3\text{ns}$	1.5	—	1.5	—

## BOOT TIME INTERFACE PARAMETERS—RV4700

Parameter	Symbol	Test Conditions	RV4700 80 MHz		RV4700 100MHz		RV4700 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	$t_{DS}$	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	$t_{DH}$	—	0	—	0	—	0	—	Master Clock Cycle

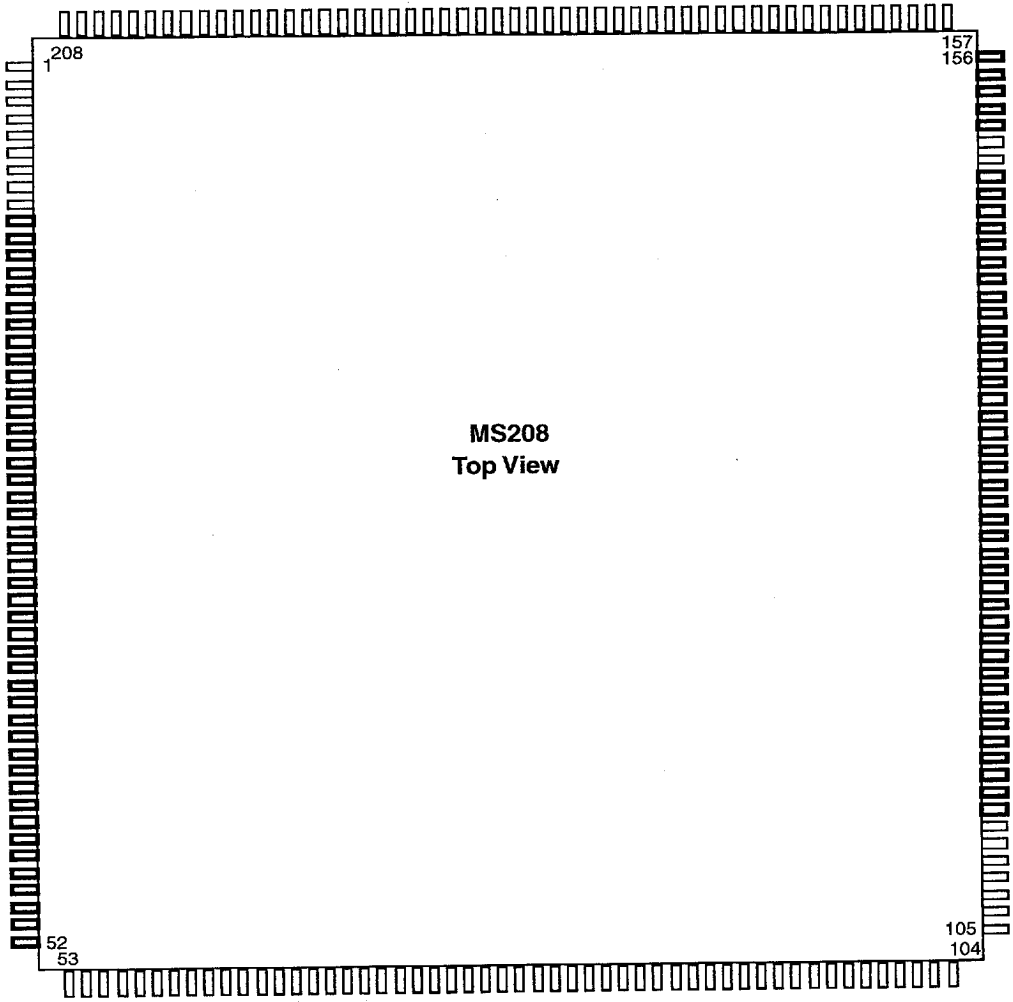
Parameter	Symbol	Test Conditions	RV4700 150MHz		RV4700 175MHz		Units
			Min	Max	Min	Max	
Mode Data Setup	$t_{DS}$	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	$t_{DH}$	—	0	—	0	—	Master Clock Cycle

## CAPACITIVE LOAD DERATION—RV4700

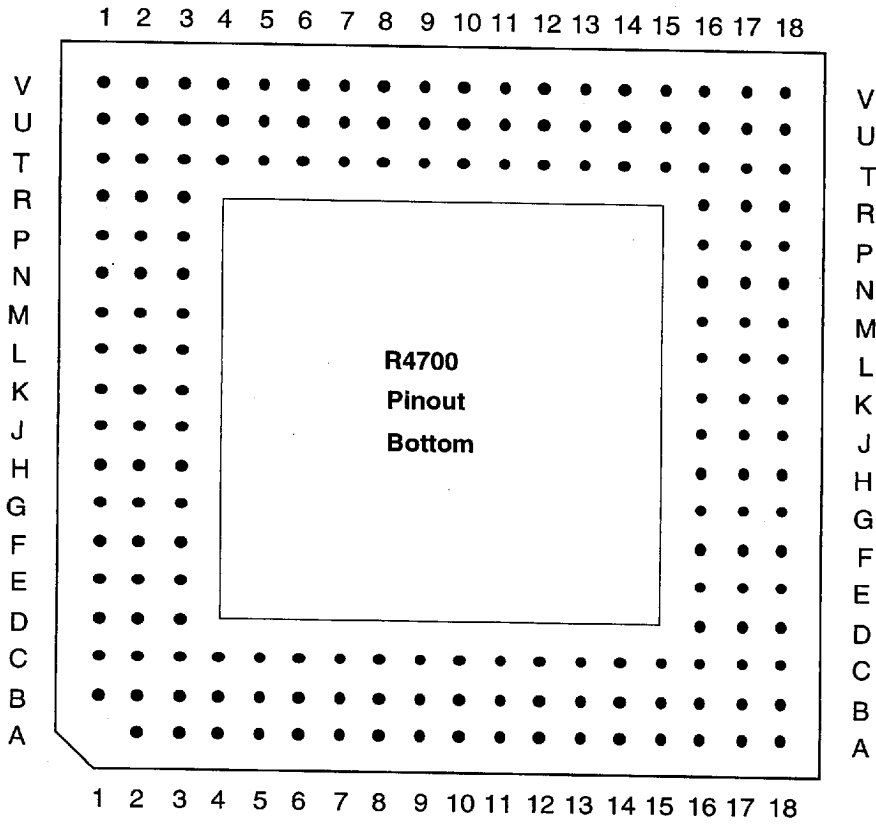
Parameter	Symbol	RV4700 80 MHz		RV4700 100MHz		RV4700 133MHz		Units
		Min	Max	Min	Max	Min	Max	
Load Derate	$C_{LD}$	—	2	—	2	—	2	ns/25pF

Parameter	Symbol	RV4700 150MHz		RV4700 175MHz		Units
		Min	Max	Min	Max	
Load Derate	$C_{LD}$	—	2	—	2	ns/25pF

PHYSICAL SPECIFICATIONS — 208-PIN MQUAD



PHYSICAL SPECIFICATIONS — PGA



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2884 drw 12

## R4700 MQUAD PACKAGE PIN-OUT†

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	N.C.	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	VSS	55	SysCmd2	107	N.C.	159	RClock0
4	VCC	56	SysAD36	108	N.C.	160	RClock1
5	SysAD45	57	SysAD4	109	VCC	161	SyncOut
6	SysAD13	58	SysCmd1	110	VSS	162	SysAD30
7	Fault*	59	VSS	111	SysAD21	163	VCC
8	SysAD44	60	VCC	112	SysAD53	164	VSS
9	VSS	61	SysAD35	113	RdRdy*	165	SysAD62
10	VCC	62	SysAD3	114	Modeln	166	MasterOut
11	SysAD12	63	SysCmd0	115	SysAD22	167	SysAD31
12	SysCmdP	64	SysAD34	116	SysAD54	168	SysAD63
13	SysAD43	65	VSS	117	VCC	169	VCC
14	SysAD11	66	VCC	118	VSS	170	VSS
15	VSS	67	N.C.	119	Release*	171	VCCOK
16	VCC	68	N.C.	120	SysAD23	172	SysADC3
17	SysCmd8	69	SysAD2	121	SysAD55	173	SysADC7
18	SysAD42	70	Int5*	122	NMI*	174	VCC
19	SysAD10	71	SysAD33	123	VCC	175	VSS
20	SysCmd7	72	SysAD1	124	VSS	176	N.C.
21	VSS	73	VSS	125	SysADC2	177	N.C.
22	VCC	74	VCC	126	SysADC6	178	N.C.
23	SysAD41	75	Int4*	127	VCC	179	N.C.
24	SysAD9	76	SysAD32	128	SysAD24	180	N.C.
25	SysCmd6	77	SysAD0	129	VCC	181	VCCP
26	SysAD40	78	Int3*	130	VSS	182	VSSP
27	N.C.	79	VSS	131	SysAD56	183	N.C.
28	N.C.	80	VCC	132	N.C.	184	N.C.
29	VSS	81	Int2*	133	SysAD25	185	MasterClock
30	VCC	82	SysAD16	134	SysAD57	186	VCC
31	SysAD8	83	SysAD48	135	VCC	187	VSS
32	SysCmd5	84	Int1*	136	VSS	188	SyncIn
33	SysADC4	85	VSS	137	IOOut	189	VCC
34	SysADC0	86	VCC	138	SysAD26	190	VSS
35	VSS	87	SysAD17	139	SysAD58	191	N.C.
36	VCC	88	SysAD49	140	IOIn	192	SysADC5
37	SysCmd4	89	Int0*	141	VCC	193	SysADC1
38	SysAD39	90	SysAD18	142	VSS	194	N.C.
39	SysAD7	91	VSS	143	SysAD27	195	VCC
40	SysCMD3	92	VCC	144	SysAD59	196	VSS
41	VSS	93	SysAD50	145	ColdReset*	197	SysAD47
42	VCC	94	ValidIn*	146	SysAD28	198	SysAD15
43	SysAD38	95	SysAD19	147	VCC	199	N.C.
44	SysAD6	96	SysAD51	148	VSS	200	SysAD46
45	ModeClock	97	VSS	149	SysAD60	201	VCC
46	WrRdy*	98	VCC	150	Reset*	202	VSS
47	SysAD37	99	ValidOut*	151	SysAD29	203	SysAD14
48	SysAD5	100	SysAD20	152	SysAD61	204	N.C.
49	VSS	101	SysAD52	153	VCC	205	TClock1
50	VCC	102	ExtRqst*	154	VSS	206	TClock0
51	N.C.	103	N.C.	155	N.C.	207	N.C.
52	N.C.	104	N.C.	156	N.C.	208	N.C.

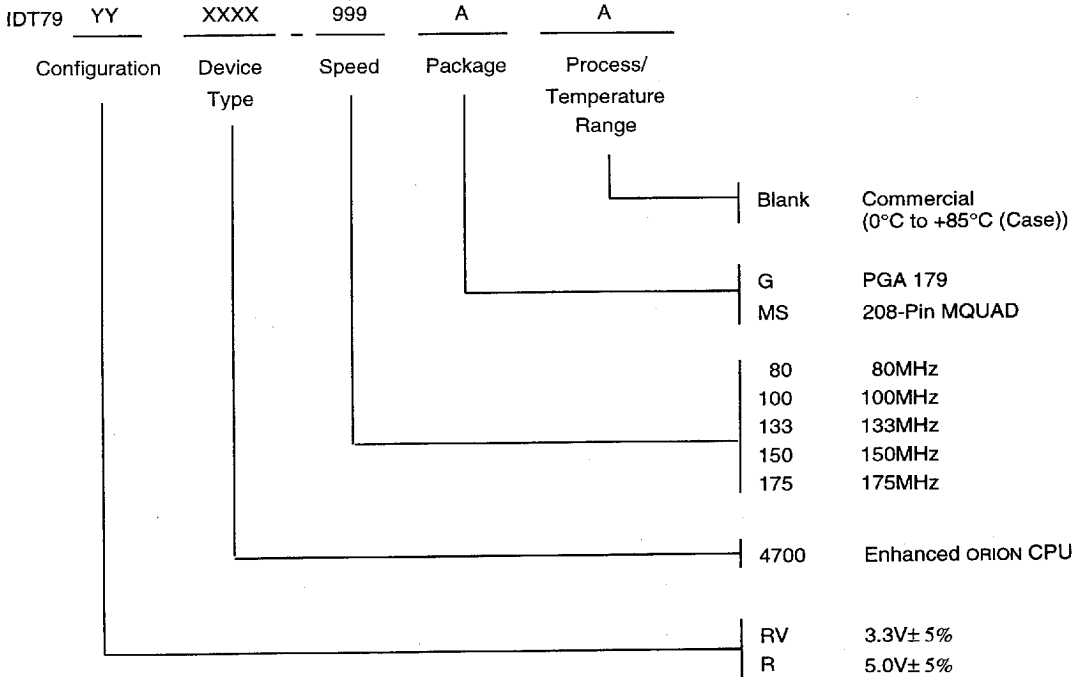
†N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

## R4700 PGA PACKAGE PIN-OUT†

Function	Pin	Function	Pin	Function	Pin
ColdReset*	T14	SysAD36	C3	VCC	C1
ExtRqst*	U2	SysAD37	B3	VCC	D18
Fault*	B16	SysAD38	C6	VCC	F1
Reserved 0 (NC)	U10	SysAD39	C7	VCC	G18
Reserved 1 (Vcc)	T9	SysAD40	C10	VCC	H1
IOIn	T13	SysAD41	C11	VCC	J18
IOOut	U12	SysAD42	B13	VCC	K1
Int0	N2	SysAD43	A15	VCC	L18
Int1	L3	SysAD44	C15	VCC	M1
Int2	K3	SysAD45	B17	VCC	N18
Int3	J3	SysAD46	E17	VCC	R1
Int4	H3	SysAD47	F17	VCC	T18
Int5	F2	SysAD48	L2	VCC	U1
MasterClock	J17	SysAD49	M3	VCC	V3
MasterOut	P17	SysAD50	N3	VCC	V6
ModeClock	B4	SysAD51	R2	VCC	V8
Modeln	U4	SysAD52	T3	VCC	V10
NMI	U7	SysAD53	U3	VCC	V12
RClock0	T17	SysAD54	T6	VCC	V14
RClock1	R16	SysAD55	T7	VCC	V17
RdRdy*	T5	SysAD56	T10	VSS	A3
Release	V5	SysAD57	T11	VSS	A6
Reset*	U16	SysAD58	U13	VSS	A8
SyncIn	J16	SysAD59	V15	VSS	A10
SyncOut	P16	SysAD60	T15	VSS	A12
SysAD0	J2	SysAD61	U17	VSS	A14
SysAD1	G2	SysAD62	N16	VSS	A17
SysAD2	E1	SysAD63	N17	VSS	A18
SysAD3	E3	SysADC0	C9	VSS	B1
SysAD4	C2	SysADC1	G17	VSS	C18
SysAD5	C4	SysADC2	T8	VSS	D1
SysAD6	B5	SysADC3	L16	VSS	F18
SysAD7	B6	SysADC4	B8	VSS	G1
SysAD8	B9	SysADC5	H16	VSS	H18
SysAD9	B11	SysADC6	U8	VSS	J1
SysAD10	C12	SysADC7	L17	VSS	K18
SysAD11	B14	SysCmd0	E2	VSS	L1
SysAD12	B15	SysCmd1	D3	VSS	M18
SysAD13	C16	SysCmd2	B2	VSS	N1
SysAD14	D17	SysCmd3	A5	VSS	P18
SysAD15	E18	SysCmd4	B7	VSS	R18
SysAD16	K2	SysCmd5	C9	VSS	T1
SysAD17	M2	SysCmd6	B10	VSS	U18
SysAD18	P1	SysCmd7	B12	VSS	V1
SysAD19	P3	SysCmd8	C13	VSS	V2
SysAD20	T2	SysCmdP	C14	VSS	V4
SysAD21	T4	TClock0	C17	VSS	V7
SysAD22	U5	TClock1	D16	VSS	V9
SysAD23	U6	VCCOk	M17	VSS	V11
SysAD24	U9	ValidIn*	P2	VSS	V13
SysAD25	U11	ValidOut*	R3	VSS	V16
SysAD26	T12	WrRdy*	C5	VSS	V18
SysAD27	U14	VCCP	K17	JTMS	E16
SysAD28	U15	VSSP	K16	JTDO	F16
SysAD29	T16	VCC	A2	JTDI	G16
SysAD30	R17	VCC	A4	JTCK	H17
SysAD31	M16	Reserved 1 (VCC)	A7		
SysAD32	H2	VCC	A9		
SysAD33	G3	VCC	A11		
SysAD34	F3	VCC	A13		
SysAD35	D2	VCC	A16		

†N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

**ORDERING INFORMATION**



**VALID COMBINATIONS**

IDT79R4700 - 80,100, 133	PGA, MQUAD Package
IDT79RV4700 - 80,100, 133, 150, 175	PGA, MQUAD Package