3.3 V 32M × 64/72-Bit SDRAM Modules
168-pin Unbuffered DIMM Modules

- 168 Pin unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications
- PC100 and PC133 versions
- One bank 32M × 64 and 32M × 72 organisation
- Optimized for byte-write non-parity or ECC applications
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- Programmed Latencies:

Product Speed		CL	t_{RCD}	t_{RP}
-7.5	PC133	3	3	3
-8	PC100	2	2	2
-8A	PC100	3	2	2

- Single + 3.3 V (± 0.3 V) power supply
- Programmable $\overline{CAS}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Uses Infineon 256 Mbit SDRAM components in 32M × 8 organization and TSOPII-54 packages
- Gold contact pads, card size: 133.35 mm × 31.75 mm × 4.00 mm
- SDRAM Performance:

		-7.5	-8	-8A	Unit
		PC133	PC100	PC100	
f_{CK}	Clock Frequency (max.)	133	100	100	MHz
t_{AC}	Clock Access Time	5.4	6	6	ns

The HYS 64V32300GU and HYS 72V32300GU are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organized as 32M × 64 and 32M × 72 in 1 memory bank high speed memory arrays designed with 256M Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use -7.5 speed sorted 32M × 8 SDRAM devices in TSOP54 packages to meet the PC133 requirement and -8,-8A & -8B components for the standard PC100 applications. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's PC100 module specification. The DIMMs have a serial presence detect, implemented with a serial E^2PROM using the 2-pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint, with 1.25“ (31.75 mm) height.

Ordering Information

Type	Code	Package	Descriptions	Module Height
HYS 64V32300GU-7.5-A HYS 64V32300GU-7.5-C	PC133-333-520	L-DIM-168-33	PC133 32M × 64 1 bank SDRAM module	1.25“
HYS 72V32300GU-7.5-A HYS 72V32300GU-7.5-C	PC133-333-520	L-DIM-168-33	PC133 32M × 72 1 bank ECC-SDRAM module	1.25“
HYS 64V32300GU-8-A HYS 64V32300GU-8-C	PC100-222-620	L-DIM-168-33	PC100 32M × 64 1 bank SDRAM module	1.25“
HYS 72V32300GU-8-A HYS 72V32300GU-8-C	PC100-222-620	L-DIM-168-33	PC100 32M × 72 1 bank ECC-SDRAM module	1.25“
HYS 64V32300GU-8A-A HYS 64V32300GU-8A-C	PC100-222-620	L-DIM-168-33	PC100 32M × 64 1 bank SDRAM module	1.25“
HYS 72V32300GU-8A-A HYS 72V32300GU-8A-C	PC100-222-620	L-DIM-168-33	PC100 32M × 72 1 bank ECC-SDRAM module	1.25“

Note: All part numbers end with a place code designating the die revision. Consult factory for current revision. Example: HYS 64V32300GU-8-A, indicating Rev. A dies are used for SDRAM components.

Pin Definitions and Functions

A0 - A12	Address Inputs	CLK0 - CLK3	Clock Input
BA0, BA1	Bank Selects	DQMB0 - DQMB7	Data Mask
DQ0 - DQ63	Data Input/Output	$\overline{CS0}$ - $\overline{CS3}$	Chip Select
CB0 - CB7	Check Bits (x72 organisation only)	V_{DD}	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read/Write Input	SDA	Serial Data Out for Presence Detect
CKE0, CKE1	Clock Enable	N.C./DU	No Connection

Address Format

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
32M × 64/72	HYS64/72V32300GU	13	10	2	8k	64 ms	7.8 µs

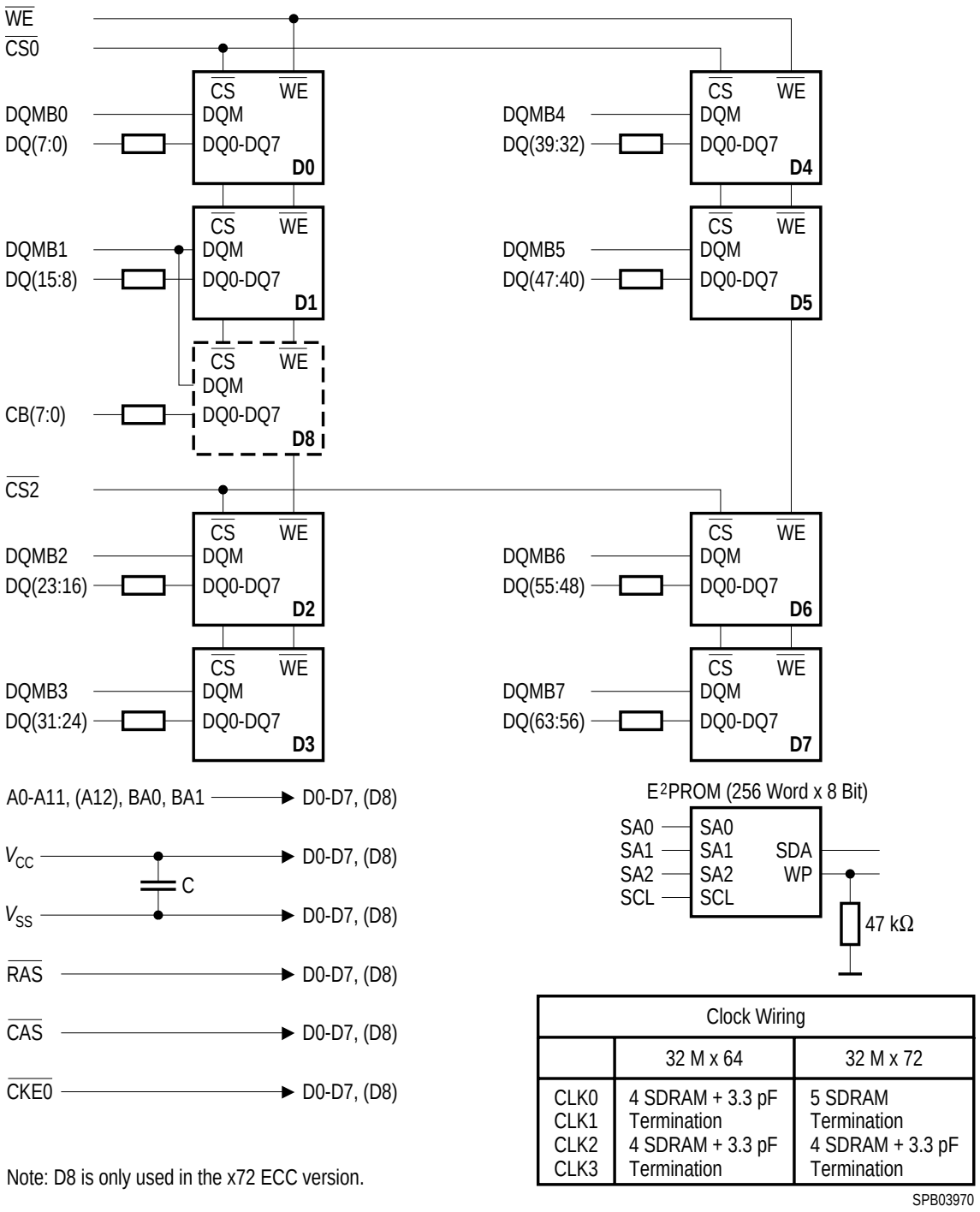
Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	$\overline{CS2}$	87	DQ33	129	$\overline{CS3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	DU	90	V_{DD}	132	N.C.
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	N.C.	92	DQ37	134	N.C.
9	DQ6	51	N.C.	93	DQ38	135	N.C.
10	DQ7	52	N.C. (CB2)	94	DQ39	136	CB6
11	DQ8	53	N.C. (CB3)	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52

Pin Configuration (cont'd)

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
19	DQ14	61	N.C.	103	DQ46	145	N.C.
20	DQ15	62	DU	104	DQ47	146	DU
21	N.C. (CB0)	63	CKE1	105	N.C. (CB4)	147	N.C.
22	N.C. (CB1)	64	V_{SS}	106	N.C. (CB5)	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	N.C.	66	DQ22	108	N.C.	150	DQ54
25	N.C.	67	DQ23	109	N.C.	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{CS0}$	72	DQ27	114	$\overline{CS1}$	156	DQ59
31	DU	73	V_{DD}	115	$\overline{RAS}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10	80	N.C.	122	BA0	164	N.C.
39	BA1	81	WP	123	A11	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V_{DD}	126	A12	168	V_{DD}

Note: Pin names in parantheses are for the x72 ECC versions; example: Pin 106 = (CB5)



Clock Wiring		
	32 M x 64	32 M x 72
CLK0 CLK1 CLK2 CLK3	4 SDRAM + 3.3 pF Termination 4 SDRAM + 3.3 pF Termination	5 SDRAM Termination 4 SDRAM + 3.3 pF Termination

Block Diagram: 32M × 64/72 One Bank SDRAM DIMM Modules

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5	0.8	V
Output High Voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V
Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 40	40	µA
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 40	40	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		max. **32M × 64**	max. **32M × 72**	
Input Capacitance (A0 to A11, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I1}	65	72	pF
Input Capacitance ($\overline{CS0}$ - $\overline{CS3}$)	C_{I2}	32	40	pF
Input Capacitance (CLK0 - CLK3)	C_{ICL}	38	40	pF
Input Capacitance (CKE0, CKE1)	C_{I3}	65	72	pF
Input Capacitance (DQMB0 - DQMB7)	C_{I4}	13	16	pF
Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	10	10	pF
Input Capacitance (SCL, SA0-2)	C_{SC}	8	8	pF
Input/Output Capacitance	C_{SD}	8	8	pF

Operating Currents per SDRAM Component [1)]
T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.3 V
(Recommended Operating Conditions unless otherwise noted)

Parameter	Test Condition	Symbol	-7.5	-8/-8A	Unit	Note
			max.			
Operating current $t_{RC} = t_{RCMIN.}$, $t_{CK} = t_{CKMIN.}$ Outputs open, Burst Length = 4, CL = 3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	–	I_{CC1}	270	210	mA	2)
Precharge stand-by current in Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, CKE ≤ $V_{IL(MAX.)}$	t_{CK} = min.	I_{CC2P}	2	2	mA	2)
Precharge Stand-by Current in Non-Power Down Mode $\overline{CS} = V_{IH\ (MIN.)}$, CKE ≥ $V_{IH(MIN.)}$	t_{CK} = min.	I_{CC2N}	25	19	mA	2)
No operating current t_{CK} = min., $\overline{CS} = V_{IH(MIN.)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	50	45	mA	2)
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}	10	10	mA	2)
Burst operating current t_{CK} = min., Read command cycling	–	I_{CC4}	80	70	mA	2), 3)
Auto refresh current t_{CK} = min., Auto Refresh command cycling	–	I_{CC5}	140	130	mA	2)
Self refresh current Self Refresh Mode, CKE = 0.2 V		I_{CC6}	2.5	2.5	mA	2)

Notes

1. All values are shown per one SDRAM component.
2. These parameters depend on the cycle rate. These values are measured at 133 MHz operation frequency for -7.5 and at 100 MHz for -8 and-8A modules.
   Input signals are changed once during t_{CK}, excepts for I_{CC6} and for stand-by currents when t_{CK} = infinity.
3. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 are assumed and the V_{DDQ} current is excluded.

AC Characteristics [1), 2)]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.		
Clock and Access Time							
Clock Cycle Time	t_{CK}						–
$\overline{CAS}$ Latency = 3		7.5	–	10	–	ns	
$\overline{CAS}$ Latency = 2		12	–	10	–	ns	
System Frequency	f_{CK}						–
$\overline{CAS}$ Latency = 3		–	133	–	100	MHz	
$\overline{CAS}$ Latency = 2							
for HYB64/72V32300GU-7.5-A		–	83	–	100	MHz	*)
for HYB64/72V32300GU-7.5-C		–	100	–	100	MHz	*)
Clock Access Time	t_{AC}						2), 3)
$\overline{CAS}$ Latency = 3		–	5.4	–	6	ns	
$\overline{CAS}$ Latency = 2		–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	3	–	ns	4)
Clock Low Pulse Width	t_{CL}	2.5	–	3	–	ns	4)
Setup and Hold Parameters							
Input Setup Time	t_{IS}	1.5	–	2	–	ns	5)
Input Hold Time	t_{IH}	0.8	–	1	–	ns	5)
Power Down Mode Entry Time	t_{SB}	–	1	–	1	CLK	6)
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	CLK	7)
Mode Register Setup Time	t_{RSC}	2	–	2	–	CLK	
Transition Time (rise and fall)	t_T	1	–	1	–	ns	–
Common Parameters							
$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}	20	–	20	–	ns	–
Precharge Time	t_{RP}	20	–	20	–	ns	–
Active Command Period	t_{RAS}	45	100k	50	100k	ns	–
Cycle Time	t_{RC}	67.5	–	70	–	ns	–
Bank to Bank Delay Time	t_{RRD}	15	–	16	–	ns	–
$\overline{CAS}$ to $\overline{CAS}$ Delay Time (same bank)	t_{CCD}	1	–	1	–	CLK	–

AC Characteristics (cont'd) [1), 2)]
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.		
Refresh Cycle							
Refresh Period (8192 cycles)	t_{REF}	–	64	–	64	ms	–
Self Refresh Exit Time	t_{SREX}	1	–	1	–	CLK	8)
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	2)
Data Out to Low Impedance	t_{LZ}	0	–	0	–	ns	–
Data Out to High Impedance	t_{HZ}	3	7	3	8	ns	9)
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	CLK	–
Write Cycle							
Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	–

AC Characteristics [1), 2)]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

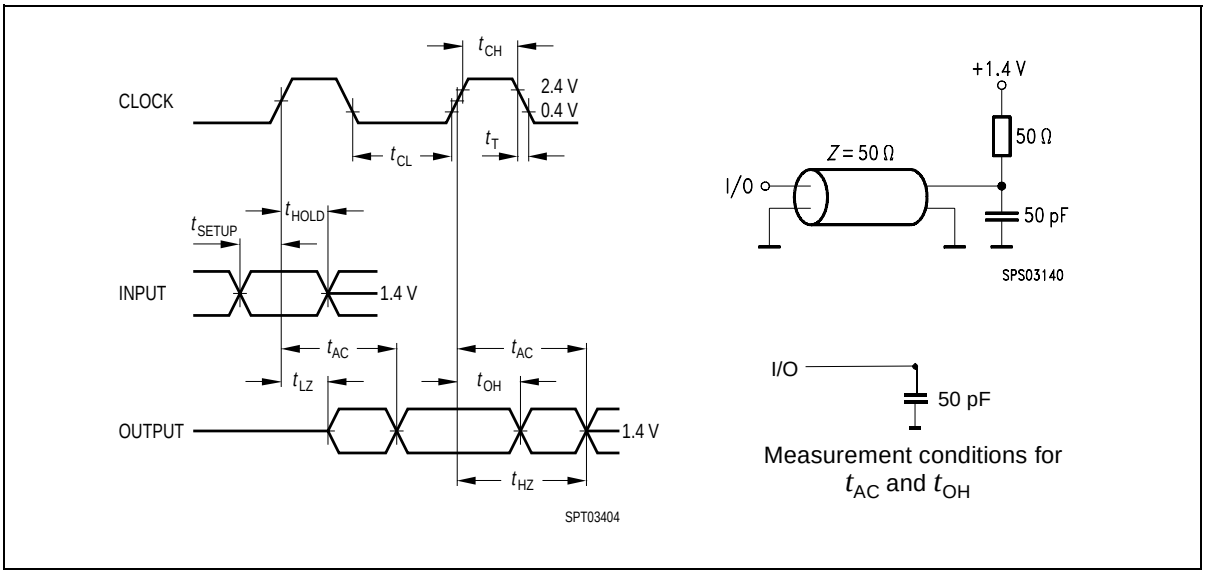
Parameter	Symbol	Limit Values		Unit	Note
		-8A PC100-322			
		min.	max.		
Clock and Clock Enable					
Clock Cycle Time	t_{CK}				–
$\overline{CAS}$ Latency = 3		10	–	ns	
$\overline{CAS}$ Latency = 2		12	–	ns	
System Frequency	f_{CK}				–
$\overline{CAS}$ Latency = 3		–	100	MHz	
$\overline{CAS}$ Latency = 2		–	83	MHz	
Access Time from Clock	t_{AC}				2), 3)
$\overline{CAS}$ Latency = 3		–	6	ns	
$\overline{CAS}$ Latency = 2		–	6	ns	
Clock High Pulse Width	t_{CH}	3	–	ns	4)
Clock Low Pulse Width	t_{CL}	3	–	ns	4)
Setup and Hold Times					
Input Setup Time	t_{IS}	2	–	ns	5)
Input Hold Time	t_{IH}	1	–	ns	5)
Power Down Mode Entry Time	t_{SB}	–	1	CLK	6)
Power Down Mode Exit Setup Time	t_{PDE}	1	–	CLK	7)
Mode Register Setup Time	t_{RSC}	2	–	CLK	–
Transition Time	t_T	0.5	10	ns	–
Common Parameters					
Row to Column Delay Time	t_{RCD}	20	–	ns	5)
Row Precharge Time	t_{RP}	20	–	ns	5)
Row Active Time	t_{RAS}	50	100k	ns	5)
Row Cycle Time	t_{RC}	70	–	ns	5)
Activate (a) to Activate (b) Command Period	t_{RRD}	16	–	ns	5)
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period	t_{CCD}	1	–	CLK	–

AC Characteristics (cont'd) [1), 2)]
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values		Unit	Note
		-8A PC100-322			
		min.	max.		
Refresh Cycle					
Refresh Period (8192 cycles)	t_{REF}	–	64	ms	–
Self Refresh Exit Time	t_{SREX}	10	–	ns	8)
Read Cycle					
Data Out Hold Time	t_{OH}	3	–	ns	2)
Data Out to Low Impedance Time	t_{LZ}	0	–	ns	–
Data Out to High Impedance Time	t_{HZ}	3	8	ns	9)
DQM Data Out Disable Latency	t_{DQZ}	–	2	CLK	–
Write Cycle					
Data Input to Precharge (write recovery)	t_{WR}	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	CLK	–

Notes

1. All AC characteristics are shown for device level.
   An initial pause of 100 µs is required after power-up. Then a Precharge All Banks command must be given followed by eight Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown in Figure below. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V/ ns edge rate between 0.8 V and 2.0 V.
3. If clock rising time is longer than 1 ns, a time (t_T/2 – 0.5) ns must be added to this parameter.
4. Rated at 1.4 V.
5. If t_T is longer than 1 ns, a time (t_T – 1) ns must be added to this parameter.
6. Whenever the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up” the device.
7. Timing is a asynchronous. If setup time is not met by rising edge of the clock then the CKE signal is assumed latched on the next cycle.
8. Self Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied after the Self Refresh Exit command is registered.
9. This is referenced to the time at which the output achieved the open circuit condition, not to output voltage levels.



Note: *) 256MByte PC133 modules with place code “-C” indicating Rev. C dies are used as memory components are fully PC100 2-2-2 backwards compatible, where PC133 modules with place code “-A” operates as PC100 3-2-2 on a 100 Mhz memory bus.

A serial presence detect storage device - E^2PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus).

SPD-Table for PC133 Modules

Byte#	Description	SPD Entry Value	Hex	
			32M × 64 -7.5	32M × 72 -7.5
0	Number of SPD Bytes	128	80	80
1	Total Bytes in Serial PD	256	08	08
2	Memory Type	SDRAM	04	04
3	Number of Row Addresses (without BS bits)	13	0D	0D
4	Number of Column Addresses	10	0A	0A
5	Number of DIMM Banks	1	01	01
6	Module Data Width	64/72	40	48
7	Module Data Width (cont'd)	0	00	00
8	Module Interface Levels	LVTTL	01	01
9	SDRAM Cycle Time at CL = 3	7.5 ns	75	75
10	SDRAM Access Time from Clock at CL = 3	5.4 ns	54	54
11	DIMM Config	none/ECC	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82	82
13	SDRAM Width, Primary	x8	08	08
14	Error Checking SDRAM Data Width	n/a/x8	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01	01
16	Burst Length Supported	1, 2, 4 & 8	0F	0F
17	Number of SDRAM Banks	4	04	04
18	Supported $\overline{CAS}$ Latencies	$\overline{CAS}$ latency = 2 & 3	06	06
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01	01
20	$\overline{WE}$ Latencies	Write latency = 0	01	01
21	SDRAM DIMM Module Attributes	non buffered/non reg.	00	00
22	SDRAM Device Attributes: General	V_{DD} tol +/– 10%	0E	0E
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2 for HYS64/72V32300GU-7.5-A	12.0 ns	C0	C0
	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 2 for HYS64/72V32300GU-7.5-C	10.0 ns	A0	A0
24	Max. Data Access Time from Clock for CL = 2	6.0 ns	60	60
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF
26	Maximum Data Access Time from Clock at CL = 1	not supported	FF	FF
27	Minimum Row Precharge Time	20 ns	14	14
28	Minimum Row Active to Row Active Delay t_{RRD}	15 ns	0F	0F
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay t_{RCD}	20 ns	14	14
30	Minimum $\overline{RAS}$ Pulse Width t_{RAS}	45 ns	2D	2D
31	Module Bank Density (per bank)	256 MByte	40	40
32	SDRAM Input Setup Time	1.5 ns	15	15

SPD-Table for PC133 Modules (cont'd)

Byte#	Description	SPD Entry Value	Hex	
			32M × 64 -7.5	**32M × 72 -7.5**
33	SDRAM Input Hold Time	0.8 ns	08	08
34	SDRAM Data Input Hold Time	1.5 ns	15	15
35	SDRAM Data Input Setup Time	0.8 ns	08	08
62-61	Superset Information (may be used in future)	–	FF	FF
62	SPD Revision	Revision 1.2	12	12
63	Checksum for Bytes 0 - 62 for HYS64/72V32300GU-7.5-A	–	56	68
	Checksum for Bytes 0 - 62 for HYS64/72V32300GU-7.5-C	–	36	48
64-125	Manufacturers Information (optional) (FF_H if not used)	–	XX	XX
126	Frequency Specification		64	64
127	100 MHz Support Details for HYS64/72V32300GU-7.5-A for HYS64/72V32300GU-7.5-C	–	 AD AF	 AD AF
128+	Unused Storage Locations	–	FF	FF

SPD-Table for PC100 Modules

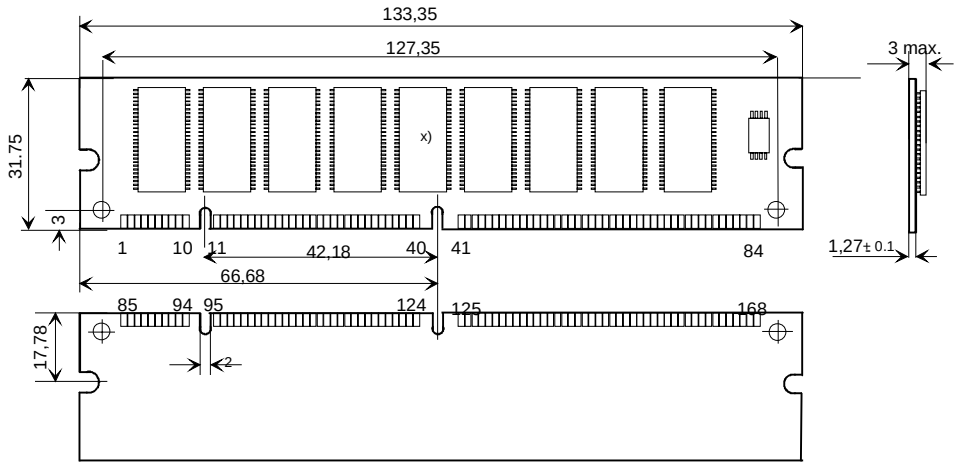
Byte#	Description	SPD Entry Value	Hex			
			32M × 64 one bank -8	32M × 64 one bank -8A	32M × 72 one bank -8	32M × 72 one bank -8A
0	Number of SPD Bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	13	0D	0D	0D	0D
4	Number of Column Addresses	10	0A	0A	0A	0A
5	Number of DIMM Banks	1	01	01	01	01
6	Module Data Width	64/72	40	40	48	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL = 3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access Time from Clock at CL = 3	6.0 ns	60	6.0	60	60
11	DIMM Config	none/ECC	00	00	02	02
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82	82	82	82
13	SDRAM Width, Primary	x8	08	08	08	08
14	Error Checking SDRAM Data Width	n/a/x8	00	00	08	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01	01	01	01
16	Burst Length Supported	1, 2, 4 & 8	0F	0F	0F	0F
17	Number of SDRAM Banks	4	04	04	04	04
18	Supported $\overline{\text{CAS}}$ Latencies	$\overline{\text{CAS}}$ latency = 2 &3	06	06	06	06
19	$\overline{\text{CS}}$ Latencies	$\overline{\text{CS}}$ latency = 0	01	01	01	01
20	$\overline{\text{WE}}$ Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM Module Attributes	non buffered/ non reg.	00	00	00	00
22	SDRAM Device Attributes: General	V_{DD} tol +/– 10%	0E	0E	0E	0E
23	Min. Clock Cycle Time at $\overline{\text{CAS}}$ Latency = 2	10.0/15.0 ns	A0	F0	A0	F0

SPD-Table for PC100 Modules

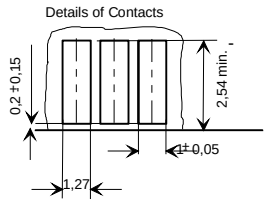
Byte#	Description	SPD Entry Value	Hex			
			32M × 64 one bank -8	32M × 64 one bank -8A	32M × 72 one bank -8	32M × 72 one bank -8A
24	Max. Data Access Time from Clock for CL = 2	6.0/7.0 ns	60	60	60	60
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Maximum Data Access Time from Clock at CL = 1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20/30 ns	14	14	14	14
28	Minimum Row Active to Row Active Delay t_{RRD}	16/20 ns	10	14	10	14
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay t_{RCD}	20 ns	14	14	14	14
30	Minimum $\overline{RAS}$ Pulse Width t_{RAS}	50/60 ns	32	32	32	32
31	Module Bank Density (per bank)	256 MByte	40	40	40	40
32	SDRAM Input Setup Time	2 ns	20	20	20	20
33	SDRAM Input Hold Time	1 ns	10	10	10	10
34	SDRAM Data Input Setup Time	2 ns	20	20	20	20
35	SDRAM Data Input Hold Time	1 ns	10	10	10	10
62-61	Superset Information (may be used in future)	–	FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for Bytes 0 - 62	–	99	ED	AB	FF
64-125	Manufacturers Information	–	XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	100 MHz Support Details	–	AF	AD	AF	AD
128+	Unused Storage Locations	–	FF	FF	FF	FF

Package Outlines

L-DIM-168-33
SDRAM DIMM Module Package
HYS 64/72V32300GU



x) on ECC modules only



DM168-33.WMF