8K x 8 RADIATION-HARDENED ROM HC6664

FEATURES

RADIATION

- Fabricated with RICMOS™ Epitaxial 1.2 µm Process
- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ N/cm²
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad(Si)/s
- ROM cells are SEU immune
- Dose Rate Survivability through $1x10^{12}$ rad(Si)/s
- Latchup Free

OTHER

- Listed on SMD #5962-93171. Available as MIL-I-38535 QML Class Q and V
- Access Time of 25 ns (typical) < 55 ns worst case (-55 to 125° C)
- Low Power Operation (worst case) < 33 mW/MHz Active < 2.5 mW Standby
- Asynchronous Operation
- TTL or CMOS Input Options with Tri-State Outputs
- Single 5 V ± 10% Power Supply
- 36-Pin Flat Pack (0.630 x 0.630 in²)
- 28-Pin DIP (Std 0.600 x 1.400 in²)
- JEDEC Compatible Pin Ordering

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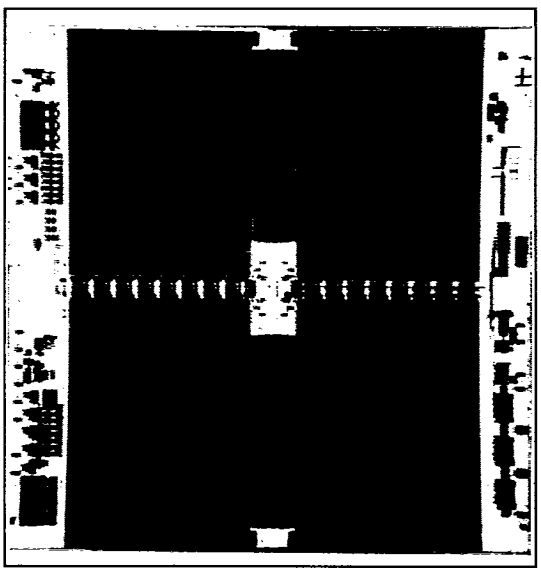
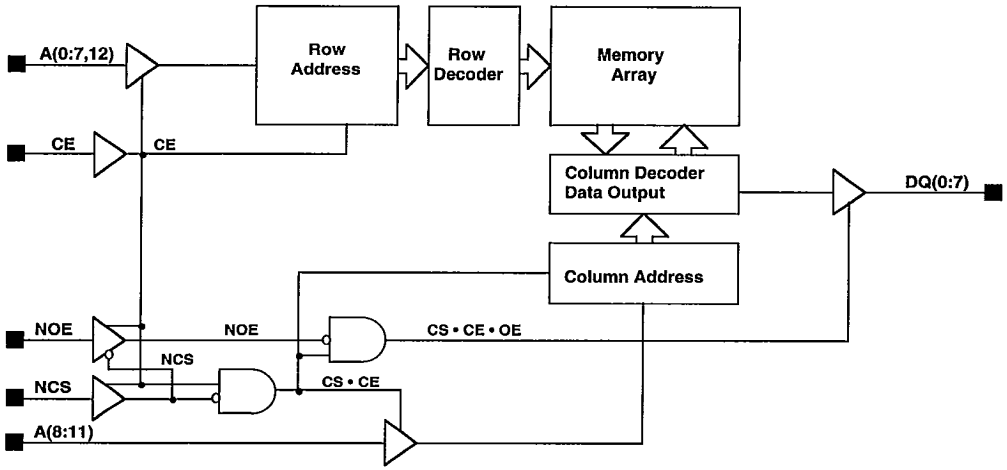
GENERAL DESCRIPTION

The 8K x 8 Radiation-Hardened ROM is a high performance 8192 x 8-bit read only memory with industry-standard functionality. It is fabricated with Honeywell's radiation-hardened CMOS technology, and is designed for use in state-of-the-art digital systems operating in space-level radiation environments. The ROM operates over the full military temperature range and requires only a single 5 V ± 10% power supply. All inputs and outputs are TTL or CMOS compatible.

Honeywell's enhanced RICMOS™ (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The RICMOS™ process is a 5 volt, n-well CMOS technology with a 250 Å gate oxide and a minimum feature size of 1.2 µm. Additional features include two layers of interconnect metallization, a lightly doped drain (LDD) structure for improved short channel reliability, and an epitaxial starting material for latchup-free operation.



FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-12 Address input pins which select a particular eight–bit word within the memory array.

DQ: 0-7 Data pins which serve as data output for a read operation

NCS Negative chip select at a low level activates a read operation. When at a high level, it defaults the ROM to a standby condition and holds the data output drivers in a high impedance state. The input circuit for input pins NOE and A: 8-11 is disabled and the signal propagation path on the remaining enabled inputs is truncated to reduce power. Dynamic IDD chip current due to partial propagation of the signal into the circuitry will occur if the enabled input pins are not quiescent. The enabled input circuits will contribute DC IDD chip current if their input pins are not at VDD or VSS levels. If this signal is not used it must be connected to VSS.

NOE Negative output enable at a high level holds the data output drivers in a high impedance state. When at a low level, data output driver state is defined by NCS and CE. If this signal is not used it must be connected to VSS.

CE Chip enable at a high level allows normal operation. When at a low level, it forces the ROM to a precharge condition, disables the input circuits on all other input pins and holds the data output drivers in a high impedance state. The dynamic and DC IDD chip current contribution from all other input circuits caused by input pins transitioning and/or not at VDD or VSS levels is eliminated. If this signal is not used it must be connected to VDD.

TRUTH TABLE

NCS	CE	NOE	MODE	DQ
L	H	L	Read	Data Out
H	H	XX	Deselected	High Z
XX	L	XX	Disabled	High Z

Notes
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X, CE=X.

RADIATION-HARDENED CHARACTERISTICS

Total Ionizing Radiation Dose

The ROM will meet all stated functional and electrical specifications after a total ionizing radiation dose of $1x10^6$ rad(SiO_2) applied at TA = 25°C. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and TA =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and ROM product using 10 keV X-ray radiation. RICMOS™ ROM performance and transistor threshold shift correlation have been made between 10 keV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at TA = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is equivalent to standard military radiation test environments.

Transient Pulse Ionizing Radiation

Data in the ROM can be accessed during and after exposure to a transient ionizing radiation pulse of ≤ 1 µs duration up to $1x10^9$ rad(Si)/s, when applied within specified operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ≤10%), it is suggested that a minimum of 0.8 µF per part of stiffening capacitance be placed between the package (chip) VDD and VSS, with a maximum inductance between the package (chip) and stiffening capacitance of 0.7 nH per part. If there are no operate-through requirements, the capacitance specification can be reduced to a minimum of 0.1 µF per part.

The ROM will meet any functional or electrical specification after exposure to a radiation pulse of ≤ 50 ns duration up to $1x10^{12}$ rad(Si)/s, when applied within specified operating conditions. Note that the current conducted during the pulse by the ROM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The ROM will meet all stated functional and electrical specifications after a total neutron fluence of up to $1x10^{14}$ N/cm² applied within specified operating or storage conditions.

Soft Error Rate

The ROM cells are immune to soft errors.

Latchup

The ROM will not latch up due to any of the above radiation exposure conditions, when applied within specified operating conditions. Fabrication with the RICMOS™ p-epi on p+ substrate process and use of proven design techniques such as double guard banding ensure latchup immunity.

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RADIATION-HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	≥$1x10^6$	rad(SiO_2)	TA=25°C
Transient Dose Rate Upset	≥$1x10^9$	rad(Si)/s	Pulse width≤1 µs
Transient Dose Rate Survivability	≥$1x10^{12}$	rad(Si)/s	Pulse width≤50 ns, X-ray, VDD=6.5 V, TA=25°C
Neutron Fluence	≥$1x10^{14}$	N/cm²	1 MeV equivalent, Unbiased, TA=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.

(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to +125°C.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating Min	Rating Max	Units
VDD	Positive Supply Voltage (referenced to VSS)		-0.5	7.0	V
VPIN	Voltage on Any Pin (referenced to VSS)		-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)		-65	150	°C
TSOLDER	Soldering Temperature • Time			270•5	°C•s
PD	Total Package Power Dissipation (2)			2.5	W
IOUT	DC or Average Output Current			25	mA
VPROT	Electrostatic Discharge Protection Voltage (3)			4000	V
ΘJC	Thermal Resistance (Junction-to-Case)	36 FP		2	°C/W
		28 DIP		10	
TJ	Junction Temperature			175	°C

(1) Stresses in excess of those listed above may result in permanent damage to the HC6364. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) RAM power dissipation due to IDDS and IDDOP, plus RAM output driver power dissipation due to external loading must not exceed this value.
(3) Class 3 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description Min	Description Typ	Description Max	Units
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical	Worst Case Min	Worst Case Max	Units	Test Conditions
CI	Input Capacitance	7		9	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance	12		14	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only.

DC ELECTRICAL CHARACTERISTICS

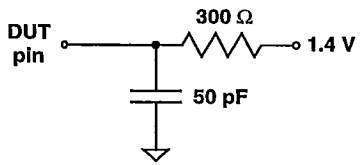
Symbol	Parameter	Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions (3)
IDDSB1	Static Supply Current	10		450	µA	IO = 0 Inputs Stable
IDDSB2	Static Supply Current with Chip Disabled	10		450	µA	VSS≤VI≤VDD IO = 0 ; CE = VIL (4)
IDDSEIH	Static Supply Current per Enabled Input*	6		30	µA	VIH = VDD-0.5V, CE = VIH (4)
IDDSEIL	Static Supply Current per Enabled Input*	6		30	µA	VIL = 0.5V, CE = VIH (4)
IDDOPR	Dynamic Supply Current, Selected (Read)	5		6	mA	f=1 MHz IO=0 CE=VIH NCS=VIL (5)
IDDOP1	Dynamic Supply Current, Deselected	0.8		1.0	mA	f=1 MHz IO=0 NCS=CE=VIH (5)
IDDOP2	Dynamic Supply Current, Disabled	1		20	µA	f=1 MHz IO=0 CE=VIL (5)
II	Input Leakage Current	0.05	-5	5	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current	0.1	-10	10	µA	VSS≤VIO≤VDD Output=high Z
VIL	Low-Level Input Voltage (TTL) (CMOS)	1.3		0.8 0.3*VDD	V	VDD=4.5V
VIH	High-Level Input Voltage (TTL) (CMOS)	1.7	2.2 0.7*VDD		V	VDD=5.5V
VOL	Low-Level Output Voltage	0.2		0.4 0.1	V	IOL = 10 mA VDD=4.5V IOL = 20 µA (4)
VOH	High-Level Output Voltage	4.4	4.2 VDD-0.1		V	IOH = -5 mA VDD=4.5V IOH = -20 µA (4)

(1) Typical operating conditions: VDD = 5.0 V,TA = 25°C, pre-radiation
(2) Worst case operating conditions: VDD = 4.5 V to 5.5 V, TA = -55°C to +125°C, total dose through $1x10^5$ rad(SiO_2)
(3) Input High = VIH ≥ VDD - 0.3 Volt, Input Low = VIL ≤ 0.3 Volt
(4) Guaranteed but not tested
(5) All inputs switching, DC average current

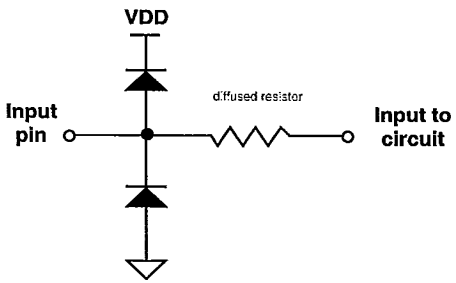
* ENABLED INPUT PINS TRUTH TABLE

CE	NCS	# of enabled input pins
H	L	19
H	H	13
L	X	1

X: VI = VIH OR VIL



EQUIVALENT LOAD CIRCUIT

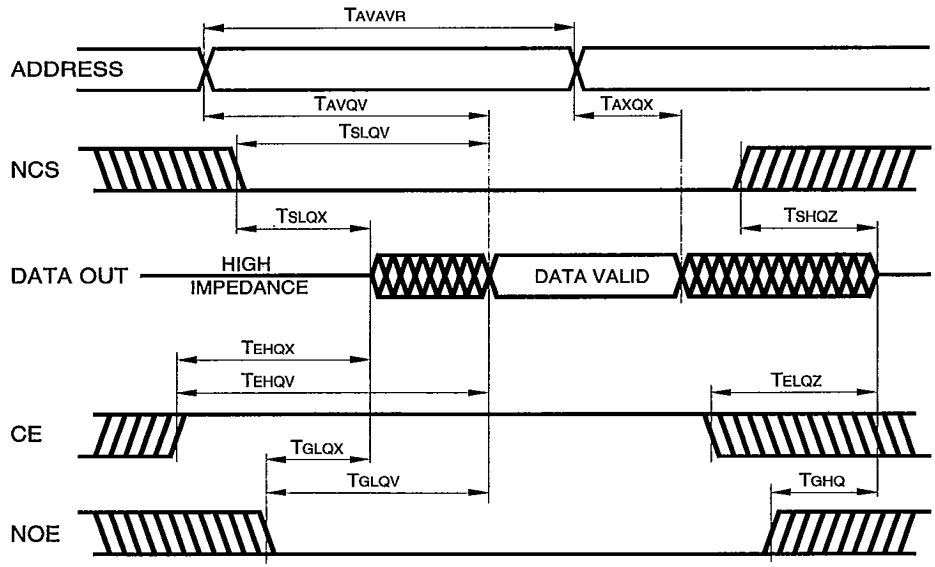


EQUIVALENT ESD PROTECTION CIRCUIT

READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) 0 to 80 °C Min	Worst Case (3) 0 to 80 °C Max	Worst Case (3) -55 to 125 °C Min	Worst Case (3) -55 to 125 °C Max	Units
TAVAVR	Address Read Cycle Time	27	45		55		ns
TAVQV	Address Access Time	25		45		55	ns
TAXQX	Address Change to Output Invalid Time	15	5		5		ns
TSLQV	Chip Select Access Time	21		45		55	ns
TSLQX	Chip Select Output Enable Time	6	0		0		ns
TSHQZ	Chip Select Output Disable Time	10		20		20	ns
TEHQV	Chip Enable Access Time	30		45		55	ns
TEHQX	Chip Enable Output Enable Time	11	0		0		ns
TELQZ	Chip Enable Output Disable Time	11		25		25	ns
TGLQV	Output Enable Access Time	11		15		15	ns
TGLQX	Output Enable Output Enable Time	7	0		0		ns
TGHQZ	Output Enable Output Disable Time	10		15		15	ns

(1) Test conditions: input switching levels VIL/VIH=0.0 V/3.0 V for TTL input buffers, and VIL/VIH=0.5 V/VDD-0.5 V for CMOS input buffers, input rise and fall times <5 ns, capacitive output loading=50 pF. Timing reference levels are shown in the Tester AC Timing Characteristics table.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, total dose through $1x10^5$ rad(SiO_2)
The -55 to 125 °C values are tested and the 0 to 80 °C values are extrapolated.



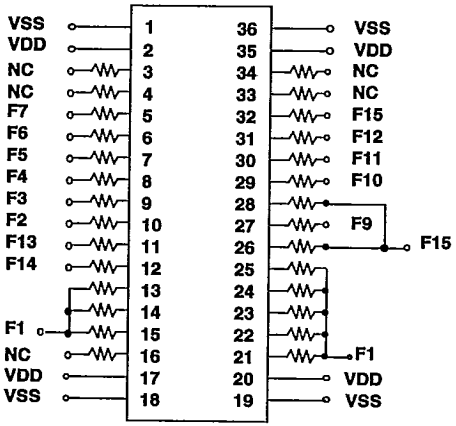
READ CYCLE

The ROM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and/or with CE held continuously high.

For an address activated read cycle, NCS must be valid prior to, coincident with, or within (TAVQV minus TSLQV) time following the activating address edge transition(s). CE must be valid a minimum of (TEHQV minus TAVQV) time prior to the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAVR. When the ROM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the ROM until TAVQX time following the next sequential address transition.

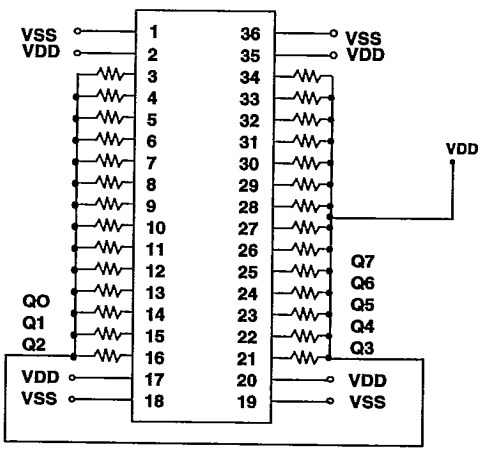
To control a read cycle with NCS, all addresses must be valid at least (TAVQV minus TSLQV) time prior to the enabling NCS edge transition. CE must be valid a minimum of (TEHQV minus TSLQV) time prior to the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when NCS is low will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.



DYNAMIC BURN-IN DIAGRAM

VDD = 5.5 ± 0.5V, R ≤ 10 KΩ, VIH = VDD, VIL = VSS
Ambient Temperature ≥ 125 °C, F0 ≥ 100 KHz Sq Wave
Frequency of F1 = F0/2, F2 = F0/4, F3 = F0/8, etc.

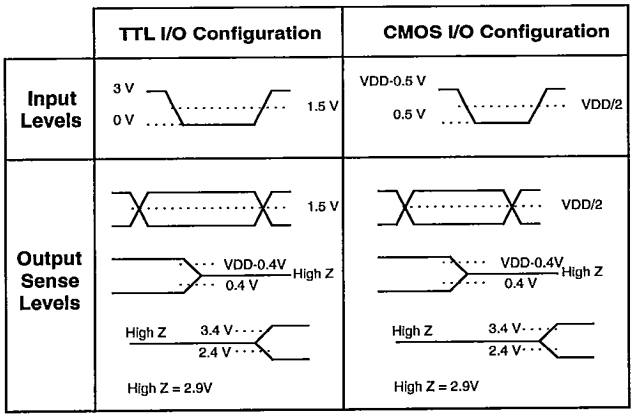


STATIC BURN-IN DIAGRAM

VDD = 5.5 ± 0.5V, R ≤ 10 KΩ
Ambient Temperature ≥ 125 °C

Note:
28-Pin DIP diagrams not shown but have similar connections.

TESTER AC TIMING CHARACTERISTICS



ROM MASK DEFINITION

To generate a mask for a ROM code, an ASCII file may be submitted. The format for the code should take the form of:

- Two fields, address followed by data in hexadecimal code.
- Addresses do not need to be in order.
- Address and data fields must be separated by at least one space or "/".
- A ";" may terminate the line, but is not required.
- No "End of File" characters are required.
- Comments are preceded by "#" .
- Comments may be on the same line AFTER address and data fields.
- Unused locations do not need to be addressed, but MUST be specified as all zeroes or all ones. This can be done as a comment.

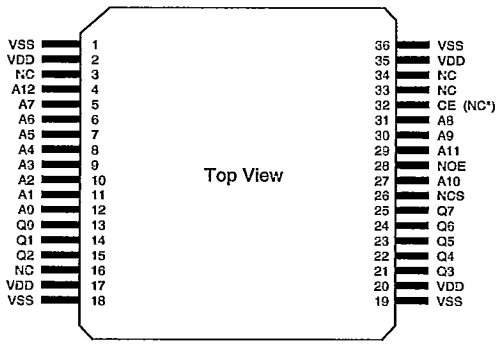
Example:

```
############################
#
# 8K X 8 ROM
#
# PATTERN #xxxx-001
#
# Dated: 12/31/89
#
############################
0 0
1 1
2 1
3 3
4 5
5 / 9
6 d
7 / 7
8 8
9 9
a a
d d
c c
11 11
############################
#
# Unused locations are zero.
#
############################
```

PACKAGING

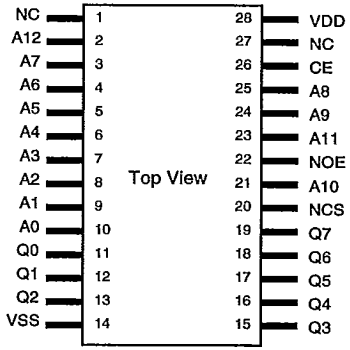
The 8K x 8 ROM is offered in a custom 36-lead flat pack or 28-lead DIP. Both packages are constructed of multilayer ceramic (Al_2O_3) and contains internal power and ground planes. Optional capacitors can be mounted to the packages to maximize supply noise decoupling and increase board packing density. The capacitors attach directly to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment. All NC pins must be connected to either VDD, VSS or an active driver to prevent charge build up in the radiation environment.

36-LEAD FLAT PACK PINOUT



* Optional package pin configuration (NC = no connect)

28-LEAD DIP PINOUT



(NC = no connect)

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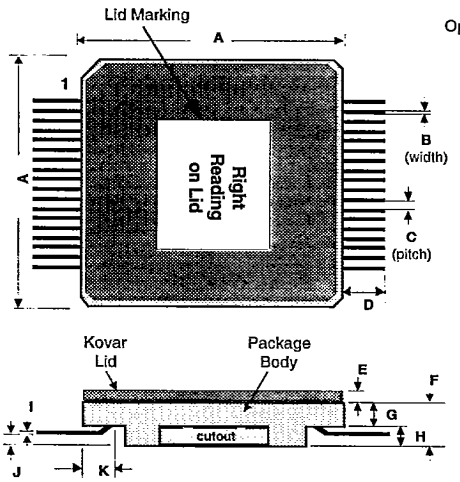
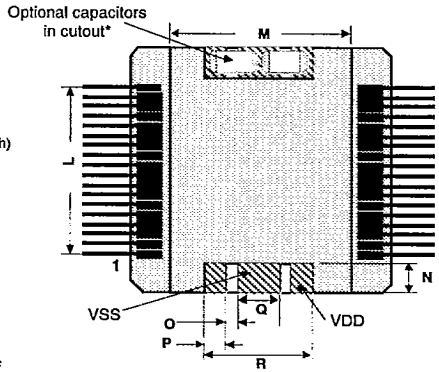
36-LEAD FLAT PACK





All dimensions in inches

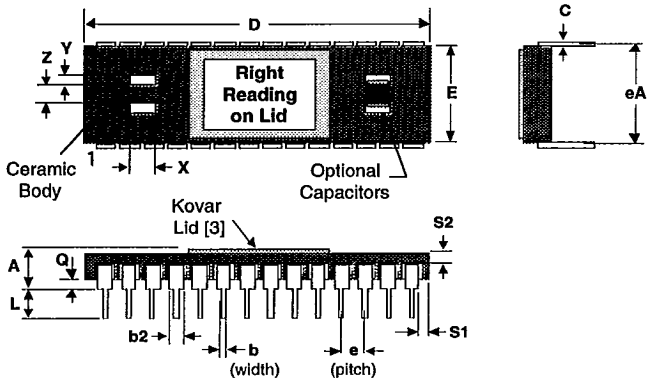
A	0.630 ± 0.007	J	0.026 min
B	0.008 ± 0.002	K	0.050 ref
C	0.025 ± 0.002	L	0.425 ± 0.005
D	0.270 min [1]	M	0.480 ± 0.006
E	0.012 ± 0.001	N	0.080 ref
F	0.115 ± 0.010	O	0.030 ref
G	0.065 ± 0.007	P	0.050 ref
H	0.050 ± 0.004	Q	0.100 ref
I	0.0060 ± 0.0015	R	0.260 ref

[1] Parts delivered with leads unformed

36 Lead Flat Pack
Package body: Honeywell #22005907
Kovar lid (solder seal): Honeywell #22006823-043
Package carrier: Honeywell #22007244
Package socket: Honeywell #22016515

*** Contact factory for optional on-package capacitors**

28-LEAD DIP



All dimensions in inches [1]

A	0.175 (max)	L	0.125 to 0.200
b	0.020 ± 0.006	Q	0.015 to 0.060
b2	0.055 ± 0.010	S1	0.005 (min)
c	0.009 to 0.012	S2	0.005 (min)
D	1.400 ± 0.020	X	0.100 ref
E	0.595 ± 0.015	Y	0.050 ref
e	0.100 BSC [2]	Z	0.075 ref
eA	0.600 BSC [2]		

[1] Dimensions meet MIL-STD-1835, Config. C, D-10
[2] BSC - Basic lead Spacing between Centers
[3] Lid tied to VSS

ORDERING INFORMATION

H — **SOURCE**
H=HONEYWELL

C — **PROCESS**
C=CMOS

6664/1 — **PART NUMBER AND PIN CONFIGURATION (3)**

X — **PACKAGE DESIGNATION**
X=36-Lead Flat Pack without capacitors
Y=36-Lead Flat Pack with capacitors
R=28-Lead DIP without capacitors
S=28-Lead DIP with capacitors
- =Bare Die (No Package)

S — **SCREEN LEVEL**
C=Brass Board
S=Modified Class S (1)
Q=QML Class Q
V=QML Class V

H — **RADIATION HARDNESS**
H=1x10^6 rad(SiO_2)

Z — **SOFT ERROR RATE (2)**
Z <1x10^{-10} upsets/bit-day
- = Brass Board

T — **INPUT BUFFER TYPE**
C=CMOS Levels
T=TTL Levels

(1) Refer to Standard Assembly and Screening Procedures section for Honeywell's screening procedures.
(2) Soft error rate (SER) specifications indicate worst case, high temperature (125°C).
(3) Optional pin configurations: (NC = no connect)

	36-LEAD FP		28-LEAD DIP	
	PIN 32	PIN 34	PIN 26	PIN 20
HC6364/1	CE	NC	CE	NCS
HC6364/2	NC	NC	-	-

Honeywell