GP517/1RZ

Advance Information

T-52-33-13

High-Reliability, Radiation-Hardened CMOS/SOS Interrupt Controller

Aerospace Class S Screening

Features:
- *Provides interrupt controller functions*
- *Meets the interrupt structure of Mil-Std-1750A*
- *Includes two timers and a Trigger Go counter*
- *Concatenable in multiples of eight bits*
- *Full military-temperature-range operation*
- *40-mil-center hermetic leadless package for high packing density*

The RCA-GP517/1RZ, a CMOS/SOS, radiation-hardened, LSI, microprogrammable interrupt controller, is part of the EPIC (emulation programmable IC) family. The EPIC family contains a number of microprogrammable and bit-slice ICs for space computers and other high-performance emulating computer applications. The GP517 works well with EPIC family microprogram sequencers like the GP501 and GP502 (2910 type).

The GP517 incorporates the functions required of interrupt controllers, but, in addition, has features tailored to meet the interrupt structure of MIL-STD-1750A. The MIL-STD-1750A defines a 16-bit microprocessor instruction set that is finding increased use in military and space applications.

The GP517/1RZ interrupt controller is available in a 48-contact leadless-chip-carrier package (J suffix) and in a 64-lead ceramic flatpack (K suffix).

Radiation Features:
- *Radiation hardened to 100 krads (Si)*
- *Latch-up free under transient radiation*
- *Resistance to upset under transient radiation rate of up to 1 x 10^{10} rads (Si)/sec*

OPERATING CONDITIONS at T_A = -55° C to +125° C. For maximum reliability, operating conditions should be selected so that operation is always with the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	4.5	10.5	V

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +11 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C ..... 500 mW
For T_A = +100 to +125° C ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125° C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING FOR K PACKAGE TYPES):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

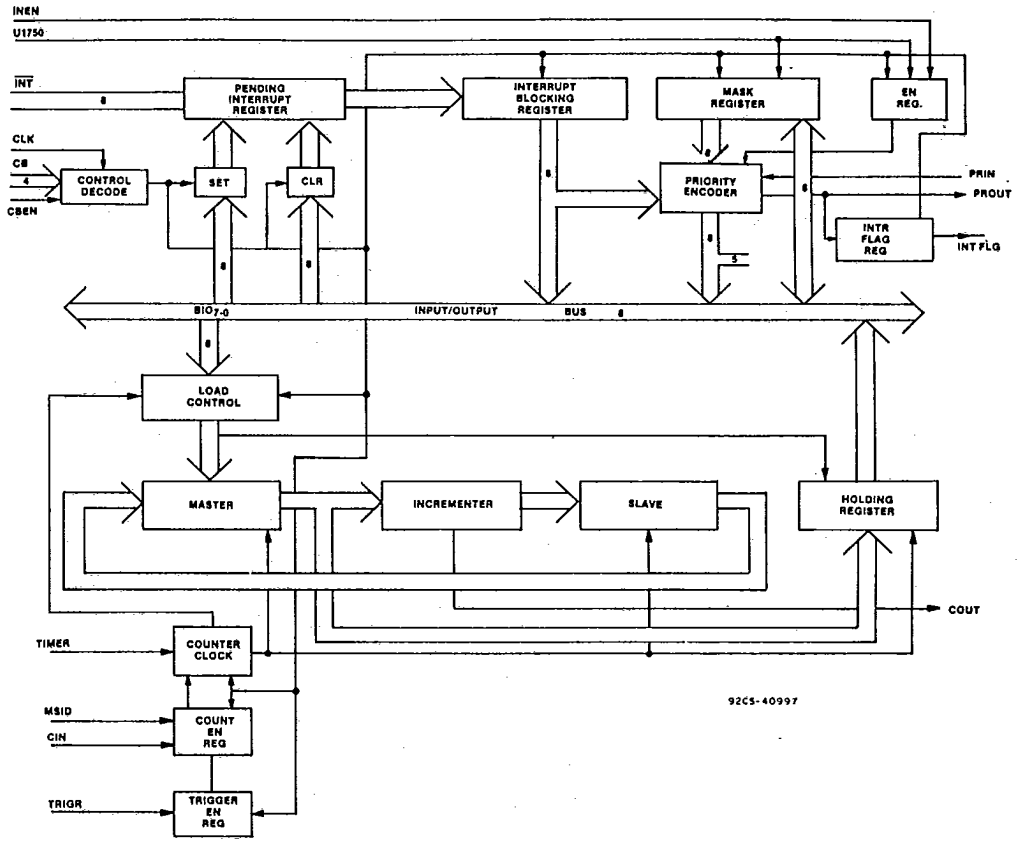

Fig. 1(a) - Functional diagram of the GP517 as an 8-bit slice.

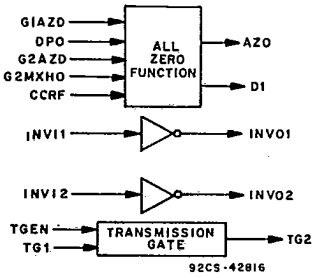

Fig. 1(b) - Random on-chip logic of GP517.

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

CHARACTERISTIC		CONDITIONS	LIMITS						UNITS
			-55°C, +25°C		+125°C		Post† Radiation +25°C		
			Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{DD}	V_{IN}=0 V or V_{DD}	—	0.5	—	1.5	—	1.5	mA
Operating Device Current	I_{OPR} Note 3	Open Circuit Outputs Cycle Time=200 ns	—	5	—	7.5	—	7.5	mA
		Open Circuit Outputs Cycle Time=1000 ns	—	2.5	—	3.5	—	3.5	mA
Input Leakage Current, Low	I_{IL}	V_{IN}=0, Note 1	—	20	—	30	—	30	µA
Input Leakage Current, High	I_{IH}	V_{IN}=V_{DD}, Note 1	—	20	—	30	—	30	µA
3-State Output Leakage Current	I_{OZL}	Applied Voltage=0 V, Note 1	—	20	—	30	—	30	µA
3-State Output Leakage Current	I_{OZH}	Applied Voltage=V_{DD}, Note 1	—	20	—	30	—	30	µA
Output (Sink) Current	I_{OL}	V_{OUT}=0.4 V	0.3	—	0.2	—	0.2	—	mA
Output (Source) Current	I_{OH}	V_{OUT}=V_{DD}-0.4 V	0.3	—	0.2	—	0.2	—	mA
Output (Sink) Current-Bus	I_{OL} Bus	V_{OUT}=0.4 V	2.5	—	1.8	—	1.8	—	mA
Output (Source) Current-Bus	I_{OH} Bus	V_{OUT}=V_{DD} -0.4 V	2.5	—	1.8	—	1.8	—	mA
Output Voltage Low Level	V_{OL}	Note 2	—	0.5	—	0.5	—	0.5	V
Output Voltage High Level	V_{OH}	Note 2	4.5	—	4.5	—	4.5	—	V
Input Low Voltage	V_{IL}	V_{OUT}=0.5 V or 4.5 V	—	0.75	—	0.75	—	0.75	V
Input High Voltage	V_{IH}	V_{OUT}=0.5 V or 4.5 V	4.25	—	4.25	—	4.25	—	V

†The limits shown are for tests performed within one hour of radiating to 100 krads (Si).

NOTES:
1. All other inputs (non-measured) are held at opposite logic level.
2. Input levels shall be V_{DD} and V_{SS}. Outputs open.
3. Measured while running the vector set.

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STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 10 V ± 5%

CHARACTERISTIC		CONDITIONS	LIMITS						UNITS
			-55°C, +25°C		+125°C		Post† Radiation +25°C		
			Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current	I_{DD}	V_{IN}=0 V or V_{DD}	—	1	—	3	—	3	mA
Operating Device Current	I_{OPR} Note 3	Open Circuit Outputs Cycle Time=200 ns	—	10	—	15	—	15	mA
		Open Circuit Outputs Cycle Time=1000 ns	—	5	—	7.5	—	7.5	mA
Input Leakage Current, Low	I_{IL}	V_{IN}=0, Note 1	—	30	—	40	—	40	μA
Input Leakage Current, High	I_{IH}	V_{IN}=V_{DD}, Note 1	—	30	—	40	—	40	μA
3-State Output Leakage Current	I_{OZL}	Applied Voltage=0 V, Note 1	—	30	—	40	—	40	μA
3-State Output Leakage Current	I_{OZH}	Applied Voltage=V_{DD}, Note 1	—	30	—	40	—	40	μA
Output (Sink) Current	I_{OL}	V_{OUT}=0.5 V	0.6	—	0.4	—	0.4	—	mA
Output (Source) Current	I_{OH}	V_{OUT}=V_{DD}-0.5 V	0.6	—	0.4	—	0.4	—	mA
Output (Sink) Current-Bus	I_{OL} Bus	V_{OUT}=0.5 V	6	—	4.3	—	4.3	—	mA
Output (Source) Current-Bus	I_{OH} Bus	V_{OUT}=V_{DD} -0.5 V	6	—	4.3	—	4.3	—	mA
Output Voltage Low Level	V_{OL}	Note 2	—	0.5	—	0.5	—	0.5	V
Output Voltage High Level	V_{OH}	Note 2	9.5	—	9.5	—	9.5	—	V
Input Low Voltage	V_{IL}	V_{OUT}=1 V or 9 V	—	1.5	—	1.5	—	1.5	V
Input High Voltage	V_{IH}	V_{OUT}=1 V or 9 V	8.5	—	8.5	—	8.5	—	V

†The limits shown are for tests performed within one hour of radiating to 100 krads (Si).

NOTES:
1. All other inputs (non-measured) are held at opposite logic level.
2. Input levels shall be V_{DD} and V_{SS}. Outputs open.
3. Measured while running the vector set.

DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ± 5%

CHARACTERISTIC	PROP. DELAY t_{PD}	MAXIMUM LIMITS			UNITS	FIG.
		-55°C, +25°C	+125°C	Post† Radiation +25°C		
INT0→PROUT	HL	110	150	150		6
$CB_{0,2,3}$→PROUT	LH	125	168	168		7
CLOCK→PROUT	HL	125	168	168		8
CLOCK→PROUT	LH	125	168	168		8
PRIN→PROUT	HL	65	87	87		9
CLOCK→COUT	LH	160	216	216		10
TIMER→COUT	HL	100	135	135		11
CBEN→BIO_3	ZH	100	135	135		12
CLOCK→INTFLG	LH	60	80	80		13
CLOCK→INTFLG	HL	65	87	87		14
PRIN→PROUT	LH	100	135	135	ns	9
G1AZD→D1	HL	35	47	47		15
G2AZD→AZO	HL	35	47	47		16
G2MXH0→D1	LH	65	87	87		17
CBEN→BIO_{2-0}	ZL	105	141	141		12
$CB_{0,3}$→PROUT	HL	105	141	141		18
$CB_{0,1,2}$→BIO_{7-0}	ZH	80	108	108		19
INVI1→INVIO1	LH	45	60	60		20
INVI2→INVIO2	LH	45	60	60		21
INVI1→INVIO1	HL	45	60	60		20
INVI2→INVIO2	HL	45	60	60		21

†Radiation measurements are made on two samples/wafer. The limits shown are for tests performed within one hour of radiating to 100 krads (Si).

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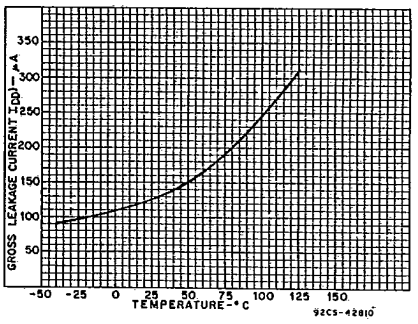

Fig. 2 - Typical gross leakage as a function of temperature.

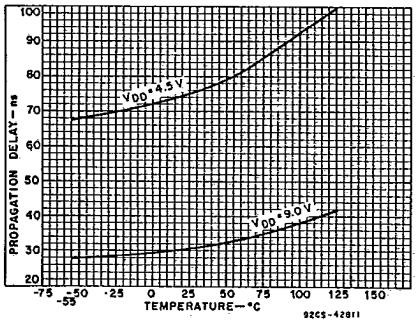

Fig. 3 - Typical propagation delay as a function of temperature.

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DYNAMIC ELECTRICAL CHARACTERISTICS, V_{DD} = 10 V ± 5%

CHARACTERISTIC	PROP. DELAY t_{PD}	MAXIMUM LIMITS			UNITS	FIG.
		-55°C, +25°C	+125°C	Post† Radiation +25°C		
$\overline{INT0}$→PROUT	HL	55	75	75		6
$CB_{0,2,3}$→PROUT	LH	65	87	87		7
CLOCK→PROUT	HL	65	87	87		8
CLOCK→PROUT	LH	65	87	87		8
PRIN→PROUT	HL	35	47	47		9
CLOCK→COUT	LH	85	114	114		10
TIMER→COUT	HL	55	75	75		11
CBEN→BIO_3	ZH	55	75	75		12
CLOCK→INTFLG	LH	35	47	47		13
CLOCK→INTFLG	HL	35	47	47		14
PRIN→PROUT	LH	50	75	75	ns	9
G1AZD→D1	HL	20	27	27		15
G2AZD→AZO	HL	20	27	27		16
G2MXH0→D1	LH	35	47	47		17
CBEN→BIO_{2-0}	ZL	55	75	75		12
$CB_{0,3}$→PROUT	HL	55	75	75		18
$CB_{0,1,2}$→BIO_{7-0}	ZH	40	54	54		19
INVI1→INVIO1	LH	25	33	33		20
INVI2→INVIO2	LH	25	33	33		21
INVI1→INVIO1	HL	25	33	33		20
INVI2→INVIO2	HL	25	33	33		21

†Radiation measurements are made on two samples/wafer. The limits shown are for tests performed within one hour of radiating to 100 krads (Si).

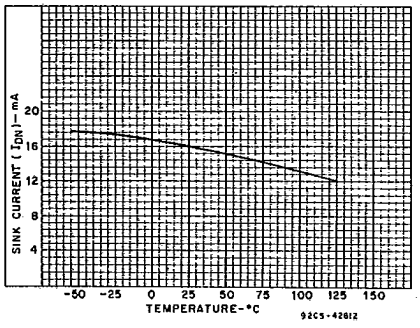


Fig. 4 - Typical sink current as a function of temperature.

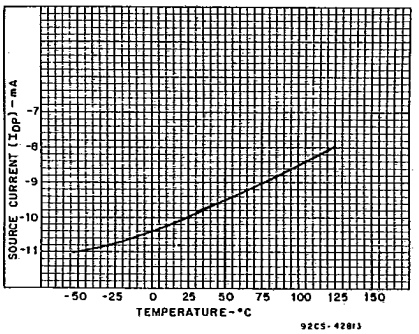
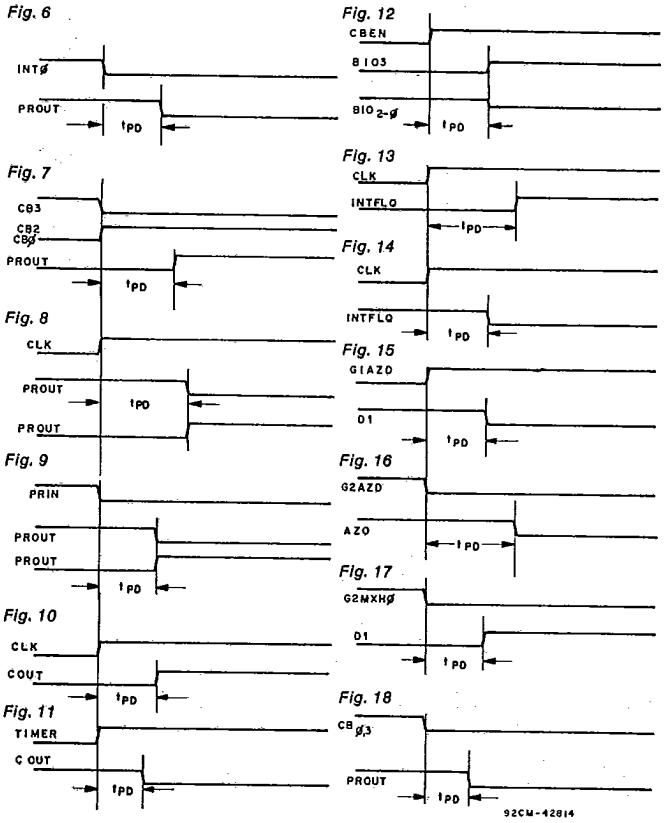
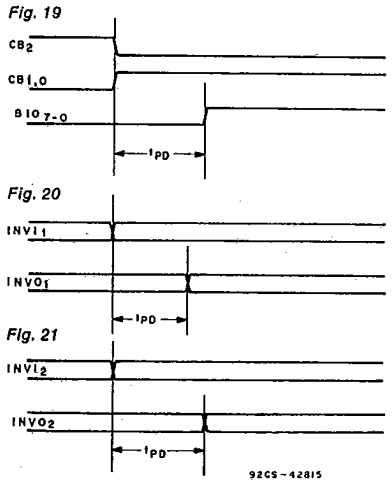


Fig. 5 - Typical source current as a function of temperature.

Timing Diagrams for Measuring Propagation Delays
Figure numbers are referred to in the Dynamic Electrical Characteristics charts.





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ARCHITECTURE AND MICROPROGRAMMING

The GP517 has three functions: interrupt handling, timer handling, and random logic operation. A functional block diagram of the interrupt controller, designed as an 8-bit slice, is shown in Fig. 1(a). The random logic is shown in Fig. 1(b).

The GP517 meets all the requirements of the 1750A interrupt structure. The IC has on-chip timer handling. For 16 interrupt lines, two units can be concatenated. If the device address pin (MSID) is wired high, the IC represents the most significant slice; if grounded, the IC is the least significant slice.

The interrupt handler responds to negative-going interrupt pulses. Of the 8 inputs on each slice, input 0 has the highest priority and input 7 the lowest. Each register on the chip is loaded from or read to the bidirectional bus BIO_{7-0}. BIO_0 is connected to the highest priority interrupt, BIO_7 to the lowest.

Arriving interrupts are stored in the PI register, then loaded into the interrupt blocking register, the output of which is used by the priority encoder, provided the mask bits are set (high) and the output of the enable register is high. Note that the blocking register cannot be loaded when the PI register is being read or when it is being used to encode a vector output to the bus. If the signal U1750 is high, interrupts 0, 1, and 5 do not use the enable register, and 0 and 5 do not use their mask bits. Hence, the interrupt definitions for 0, 1, and 5 in Table I are satisfied.

The priority output (PROUT) is low if an interrupt has been stored in the interrupt blocking register or if the priority input (PRIN) is low. A low PRIN indicates an interrupt in a unit of higher priority.

The highest priority interrupt in the PI register is encoded as one-of-eight, and the 3-bit value is output on BIO_{2-0}. Input 0 (highest priority) will output a code of 111. The inverted value of MSID is output on BIO_3, and zeroes are output to BIO_{7-4}. If no interrupts are pending, the BIO_{7-0} is 0.

The GP517 is under microcontrol by a 4-bit instruction field, CB_{3-0}, and an enable signal, CBEN. If CBEN is low, no operation is done. If CBEN is high, the four-bit field is decoded to determine which of 16 functions is to be executed.

The timer is an 8-bit counter that can be concatenated (Fig. 1(a)). The counter consists of a master section, an incrementer, a slave section, and a holding register. The master section accepts data from the slave when the counter clock is high.

The slave accepts data from the master through the incrementer when the counter clock is low. The holding register accepts data from the master when the clock is high. The design prevents the holding register from changing while the counter is being read to the bus.

Loading of the various sections is controlled by the clock and the count enable register. The latter is set by the start count instruction and is cleared by the stop count or load counter instructions. The count enable register can also be set if the trigger enable register is set by a negative edge transition at the external trigger input.

The interrupt handler performs eleven microcoded functions and the timer five. These functions are summarized in Table II.

Table I - Definition of Interrupts For Mil-Std-1750A

Interrupt Number	Definitions
0 (Highest Priority)	Power Down (cannot be masked or disabled)
1	Machine Error (cannot be disabled)
2	Spare
3	Floating Point Overflow
4	Fixed Point Overflow
5	Executive Call (cannot be masked or disabled)
6	Floating Point Underflow
7	Timer A (if implemented)
8	Spare
9	Timer B (if implemented)
10	Spare
11	Spare
12	Input/Output Level 1 (if implemented)
13	Spare
14	Input/Output Level 2 (if implemented)
15	Spare

Table II - Functions of the Interrupt Handler

Instruction Field	Action
0 or 1	No operation
2	Load 1-bit interrupt-enable register from INEN
3	Load interrupt mask register with value of bus: BIO_{7-0}
4	Reset pending interrupt for each bit set of corresponding bit in BIO_{7-0}
5	Set pending interrupt for each corresponding bit set of BIO_{7-0}
6	Clear interrupt flag - INTFLG goes low - PROUT goes high
7	Strobe interrupt flag - Load interrupt flag register with $\overline{PROUT}$
8	Output vector, and clear pending interrupt - 3-bit encoded value is output on BIO_{2-0} - $\overline{MSID}$ is output on BIO_3
9	Read pending interrupt - Output of blocking register goes to BIO_{7-0}
A_H	Read interrupt mask register - Contents go to BIO_{7-0}
B_H	Read counter - Output goes to BIO_{7-0}
C_H	Load counter - Loads from BIO_{7-0} into master, slave and holding register - Clears count enable and trigger enable registers
D_H	Stop counter - Clears count enable and trigger enable registers
E_H	Start counter - Sets count enable register
F_H	Arm trigger Go - Sets trigger enable register

The following list elaborates on Table II.

Details of Micro-operations

a: The interrupt handler performs the following microcoded functions:

CB_{3-0} Effect

0, 1 **No operation**

2 **Load interrupt enable register** - When the CPU clock is high, loads the one-bit register from the INTEN input. If this input is high, all eight interrupts are enabled. If INTEN is low, all interrupts are disabled. If U1750 is high, interrupts 0, 1 and 5 are not affected by the interrupt enable register.

3 **Load interrupt mask register** - When the CPU clock is high, loads the register with the value of BIO_{7-0}. An interrupt may pass on to the interrupt blocking register if its mask register bit is set. Note that interrupt 0 connects to the mask bit loaded from BIO_7. If the input U1750 is high, interrupts 0 and 5 are not affected by the mask.

4 **Reset pending interrupt** - When the CPU clock is high, each bit in the register is reset for which the corresponding bit of BIO_{7-0} is set. If a bit of the PIR is being reset, and its interrupt input goes low, that bit of the PIR will not be set.

5 **Set pending interrupt** - When the CPU clock is high, each bit in the register is set for which the corresponding bit of BIO_{7-0} is set.

6 **Clear interrupt flag** - When the CPU clock is high, clears the interrupt flag register. This will force INTFLG low. Also, when the CPU clock is high, this sets PROUT.

7 **Strobe interrupt flag** - When the CPU clock is high, loads the interrupt flag register with PROUT inverted. The interrupt flag output (INTFLG) will always output the value of this register. A high level indicates that an interrupt has been loaded into the interrupt blocking register of either this ICT or in an ICT of higher priority.

8 **Output vector and clear pending interrupt** - The highest priority interrupt in the pending interrupt register is encoded as one of eight, and the three-bit encoded value is output on BIO_{2-0}. Input 0 (the highest priority) would output a code of 111. The inverted value of MSID is output on BIO_3. Zeros are output to BIO_{7-4}. If no interrupt is pending, zeros are output to BIO_{7-0}. When the CPU clock is high, the encoded interrupt is cleared in the PIR, and PROUT is forced high. The interrupt blocking register will not change during this instruction in order to prevent a late arriving interrupt from affecting the priority encoder. If the interrupt input for the encoded interrupt goes low during this instruction, it will not set the PIR.

9 **Read pending interrupt** - The contents of the interrupt blocking register are output on BIO_{7-0}. If the PIR changes during this instruction (i.e., an interrupt is received), neither the blocking register nor BIO_{7-0} will change. (NOTE: Executing this instruction on consecutive microcycles may not give the correct value of the PIR on the second microcycle).

A **Read interrupt mask register** - The contents of the register are output on BIO_{7-0}.

b: The following microcoded instructions are performed by the timer:

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CB_{3-0} Effect

B **Read counter** - Outputs the contents of the counter holding register to BIO_{7-0}.

C **Load counter** - When the CPU clock is high, loads the value of BIO_{7-0} into the master, slave, and holding register sections of the counter. Clears the count enable register and clears the trigger enable register.

D **Stop counter** - When the CPU clock is high, clears the count enable register and clears the trigger enable register.

E **Start counter** - When the CPU clock is high, sets the count enable register.

F **Arm trigger Go** - When the CPU clock is high, sets the trigger enable register. This will allow the next 1 → 0 transition of the external trigger input to set the count enable register.

Timer

The timer is an 8-bit concatenated counter. The counter consists of a master section, an incrementer, a slave section, and a holding register. The count enable register and counter clock control loading of the various sections. The count enable register is set by the start count instruction and is cleared by the stop count or load counter instructions. It may be set by a 1 → 0 transition of the external trigger input if the trigger enable register is set.

The counter clock will be high if CIN is low (MS IC only), if the TIMER input is high or if the counter is being loaded. (Note that CIN is not used by the LS IC.) If none of these three conditions is met, the counter clock will be low if the count enable register is set. Once the counter clock is low, it cannot go high again until TIMER is high, the counter is loaded, or CIN is low. (Note that loading a count will stop the current count and load a new value; however, stopping a count will allow the current count to complete.)

The master section accepts data from the slave when the counter clock is high. The slave accepts data from the master through the incrementer when the counter clock is low. The holding register accepts data from the master when the counter clock is high, if the IC is not reading the counter, and if the counter clock was high when the CPU clock was last high. This keeps the holding register from changing while the counter is read to BIO. When the counter is loaded, the master, slave, and holding registers are all loaded.

Random Logic

The random logic consists of five functions. The first function is a transmission gate. If TGEN is high, the bus pins TG1 and TG2 are connected by the transmission gate. If TGEN is low, TG1 and TG2 are isolated. Two functions are simple inverters. The output $\overline{INVO1}$ is the complement of the input INVI1. The output INVO2 is the complement of the input INVI2. The other two functions derive the outputs AZO and D1. The logical equations for each are:

$$AZO = \overline{G2AZD\ (G1AZD + \overline{DPO})}$$
$$D1 = \overline{AZO} * \overline{G2MXHO}$$

The random logic was designed to be used in architectures using the GP001.

D1 is a 3-state output which is enabled when the CCRF (condition code register flag) input is high. D1 is a function of AZO.

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Pin Functions for the GP517
48-Contact Leadless Chip Carrier

Pin No.	Signal Name	Mnemonic	I/O	Pin No.	Signal Name	Mnemonic	I/O
1	Interrupt Enable Input	INTEN	I	25	Double Precision Operation Input	DPO	I
2	Bidirectional Data Bus 6	BIO_6	I/O	26	Data 1 Output	D1	O
3	Counter Carry Input	CIN	I	27	All Zero Detect Output	AZO	O
4	Timer Input	TIMER	I	28	GPU2 Multiplexer High 0 Input	G2MXH0	I
5	Most Significant IC Identifier	MSID	I	29	Condition Code Register Flag Input	CCRF	I
6	External Trigger Input	TRIGR	I	30	GPU2 All Zero Detect Input	G2AZD	I
7	Control Bit Enable Input	CBEN	I	31	Interrupt Input 7	$\overline{INT7}$	I
8	Control Bit Input 3	CB3	I	32	Interrupt Input 6	$\overline{INT6}$	I
9	Control Bit Input 2	CB2	I	33	Interrupt Input 5	$\overline{INT5}$	I
10	CPU Clock	CLK	I	34	Interrupt Flag Output	INTFLG	O
11	Control Bit Input 0	CB0	I	35	Bidirectional Data Bus 3	BIO_3	I/O
12	Bidirectional Data Bus 4	BIO_4	I/O	36	Interrupt Input 4	$\overline{INT4}$	I
13	Control Bit Input 1	CB1	I	37	Interrupt Input 3	$\overline{INT3}$	I
14	Bidirectional Data Bus 2	BIO_2	I/O	38	Interrupt Input 2	$\overline{INT2}$	I
15	Priority Output	PROUT	O	39	Bidirectional Data Bus 5	BIO_5	I/O
16	Counter Carry Output	COUT	O	40	Interrupt Input 1	$\overline{INT1}$	I
17	Inverter Input 2	INVI2	I	41	Upper IC for 1750 Architecture Input	U1750	I
18	Inverter Output 2	INVO2	O	42	Interrupt Input 0	$\overline{INT0}$	I
19	GPU1 All Zero Detect Input	G1AZD	I	43	Priority Input	PRIN	I
20	Inverter Input 1	INVI1	I	44	Transmission Gate Enable Input	TGEN	I
21	Inverter Output 1	INVO1	O	45	Transmission Gate Bus 2	TG2	I/O
22	Bidirectional Data Bus 0	BIO_0	I/O	46	Transmission Gate Bus 1	TG1	I/O
23	Bidirectional Data Bus 1	BIO_1	I/O	47	Bidirectional Data Bus 7	BIO_7	I/O
24	Ground	V_{SS}	—	48	Power	V_{DD}	—

Pin Functions for the GP517
64-Lead Flat Pack

Pin No.	Signal Name	Mnemonic	I/O	Pin No.	Signal Name	Mnemonic	I/O
1	No Connection	NC	—	33	No Connection	NC	—
2	No Connection	NC	—	34	No Connection	NC	—
3	Priority Input	PRIN	I	35	GPU1 All Zero Detect Input	G1AZD	I
4	Transmission Gate Enable Input	TGEN	I	36	Inverter Input 1	INVI1	I
5	Transmission Gate Bus 2	TG2	I/O	37	Inverter Output 1	INVO1	O
6	Transmission Gate Bus 1	TG1	I/O	38	Bidirectional Data Bus 0	BIO_0	I/O
7	Bidirectional Data Bus 7	BIO_7	I/O	39	Bidirectional Data Bus 1	BIO_1	I/O
8	Power	V_{DD}	—	40	Ground	V_{SS}	—
9	Interrupt Enable Input	INTEN	I	41	Double Precision Operation Input	DPO	I
10	Bidirectional Data Bus 6	BIO_6	I/O	42	Data 1 Output	D1	O
11	Counter Carry Input	CIN	I	43	All Zero Detect Output	AZO	O
12	Timer Input	TIMER	I	44	GPU2 Multiplexer High 0 Input	G2MXH0	I
13	Most Significant IC Identifier	MSID	I	45	Condition Code Register Flag Input	CCRF	I
14	External Trigger Input	TRIGR	I	46	GPU2 All Zero Detect Input	G2AZD	I
15	No Connection	NC	—	47	No Connection	NC	—
16	No Connection	NC	—	48	No Connection	NC	—
17	No Connection	NC	—	49	No Connection	NC	—
18	No Connection	NC	—	50	No Connection	NC	—
19	Control Bit Enable Input	CBEN	I	51	Interrupt Input 7	$\overline{INT7}$	I
20	Control Bit Input 3	CB3	I	52	Interrupt Input 6	$\overline{INT6}$	I
21	Control Bit Input 2	CB2	I	53	Interrupt Input 5	$\overline{INT5}$	I
22	CPU Clock	CLK	I	54	Interrupt Flag Output	INTFLG	O
23	Control Bit Input 0	CB0	I	55	Bidirectional Data Bus 3	BIO_3	I/O
24	Bidirectional Data Bus 4	BIO_4	I/O	56	Interrupt Input 4	$\overline{INT4}$	I
25	Control Bit Input 1	CB1	I	57	Interrupt Input 3	$\overline{INT3}$	I
26	Bidirectional Data Bus 2	BIO_2	I/O	58	Interrupt Input 2	$\overline{INT2}$	I
27	Priority Output	PROUT	O	59	Bidirectional Data Bus 5	BIO_5	I/O
28	Counter Carry Output	COUT	O	60	Interrupt Input 1	$\overline{INT1}$	I
29	Inverter Input 2	INVI2	I	61	Upper IC for 1750 Architecture Input	U1750	I
30	Inverter Output 2	INVO2	O	62	Interrupt Input 0	$\overline{INT0}$	I
31	No Connection	NC	—	63	No Connection	NC	—
32	No Connection	NC	—	64	No Connection	NC	—

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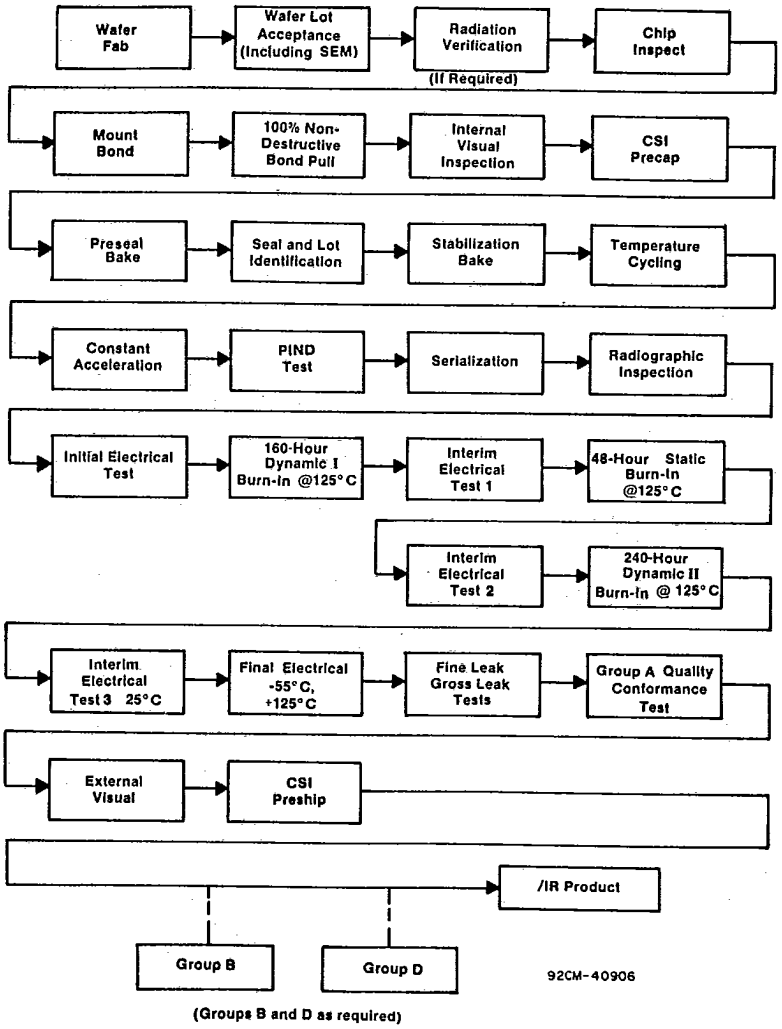
Flowchart for Modified Class S Screening per Mil-Std-883 Method 5004



(Groups B and D as required)

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Modified Class S Screening for GP517/1RZ
Per Mil-Std-883 Method 5004

SCREEN	METHOD	REQMT.	NOTES
Wafer Lot Acceptance Incl. SEM	5007	100%	
Radiation Verification (If Req'd)	1019	Sample	
Nondestructive Bond Pull	1019	100%	
Internal Visual	2010 Cond. A (Modified)	100%	See "Visual Inspection"
Pre-Seal Bake	—	100%	
Stabilization Bake	1008 Cond. C 24 Hours Min, 150° C Min	100%	
Temperature Cycling	1010 Cond. C (-65° C to 150° C)	100%	
Constant Acceleration	2001 Cond. E Y1 Dir., 30,000 g	100%	
Particle Impact Noise Detection (PIND)	2020 Cond. A 20g peak at 60 Hz	100%	
Serialization	—	100%	
Radiographic, 1-View	2012	100%	
Initial (Pre Burn-In) Electrical Parameters at 25° C	Per Applicable Device Spec.	100%	See Table IV
Burn-In Test (Dynamic I) 160 Hours at 125° C	1015	100%	See Table V
Interim Electrical Test 1 % Defective Allowable (10%)	—	100% All Tests	See Table IV
48-Hour Static Burn-In at 125° C (With Delta Requirements) Interim Electrical Test 2 % Defective Allowable (5%) Functional (3%)	—	100% 100% All Tests	
240-Hour Dynamic Burn-In (Dynamic II) (With Delta Requirements)	1015	100%	See Tables V, VI and VII
Interim Electrical Test 3 Electrical Parameters at 25° C % Defective Allowable (5%) Functional (3%)	Per Applicable Device Spec.	100% All Tests	See Table IV
Final Elect. Test @ -55/+125° C	—	100%	See Table IV
Seal A) Fine B) Gross	1014 Cond. A or B Cond. C	 100% 100%	
Group A Quality Conformance	5005 - Class S	100%	See Table IV
External Visual	2009	100%	
Group B Quality Conformance	5005 - Class S	Optional	See Table IV
Group D Quality Conformance	5005 - Class S	Optional	See Table IV
CSI and/or GSI (Optional)			

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Table IV - Electrical Tests

For individual tests, refer to the Static and Dynamic Characteristics charts.

Post Radiation	Post Radiation, 25°C
Initial Electrical Tests	Same as above 25°C
Interim Electrical Tests I	Same as above 25°C
Interim Electrical Tests II	Same as above 25°C
Interim Electrical Tests III	Same as above 25°C
Final Electrical Tests	Same as above -55°C, 25°C, 125°C
Quality Conformance:	
Group A	Same as above -55°C, 25°C, 125°C
Group B	Same as above 25°C
Group D	Same as above 25°C

Table V—Burn-In and Life-Test Circuits and Timing Waveforms

Test	Temperature	Duration Min.	V_{DD} Min.
Dynamic I	125°C	160 hrs.	11 V
Static	125°C	48 hrs.	11 V
Dynamic II	125°C	240 hrs.	11 V
Life Test	125°C	1000 hrs.	10.5 V

Table VI—Delta Limits

Test	Symbol	Delta* Limits
Quiescent Device Current	I_{DD}	±100 μA
Output Low Current	I_{OL}	±25%†
Output High Current	I_{OH}	±25%†

V_{DD} = 10 V ± 5%.
*Limits apply at +25°C.
†Measured from initial value.

Table VII—Delta Calculations

Delta Calculation	Initial Reading	Final Reading
I	Interim Electrical Tests 1	Interim Electrical Tests 2
II	Interim Electrical Tests 1	Interim Electrical Tests 3

See Screening Flowchart, page 12.

VISUAL INSPECTION

Visual Inspection for Class S is performed to MIL-STD-883, Method 2010, Condition A except as follows:

Use:

3.2.1.1 - Metallization Scratches
3.2.1.2 - Metallization Voids
3.2.1.6 - Metallization Bridging
3.2.1.7 - Metallization Alignment
3.2.3 - Scribing and Die Defects. In addition, semi-circular cracks that point away from the active circuit area are acceptable.
3.2.3c - A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line.
3.1.7b - Lifting or Peeling of Glassivation, add NOTE of 3.2.7b to 3.1.7b.

Notes:

A. High magnification inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required.
B. Criteria 3.2.1.1a Metallization Scratches, and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed.
C. Criteria 3.2.1.7 Metallization Alignment and 3.1.2 Diffusion and Passivation(s) Faults are applied to the center and two opposite corners of the chip. Areas of sufficient complexity are viewed to assure general alignment and contact coverage and shall consist only of the area exposed to the immediate field of view.
D. SOS Technology Devices
   1. Diffusion faults 3.1.2.1 are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
   2. The 1-mil wire clearance criteria is not applicable.
   3. Passivation faults are not applicable when a second free-flow oxide is used prior to metallization.
   4. Oxide gate bridge inspection is not applicable.
   5. Semicircular cracks not in an active area which start and end at the pellet edge are acceptable.

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