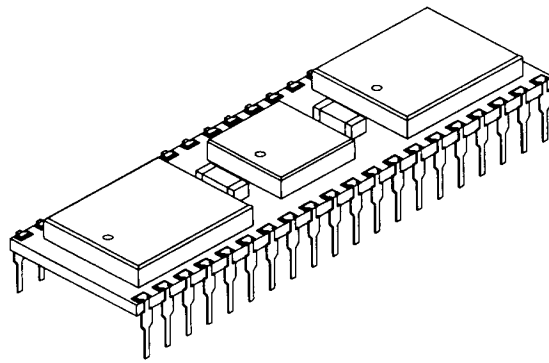
DPS8M656

16K X 16 CMOS SRAM MODULE



DESCRIPTION:

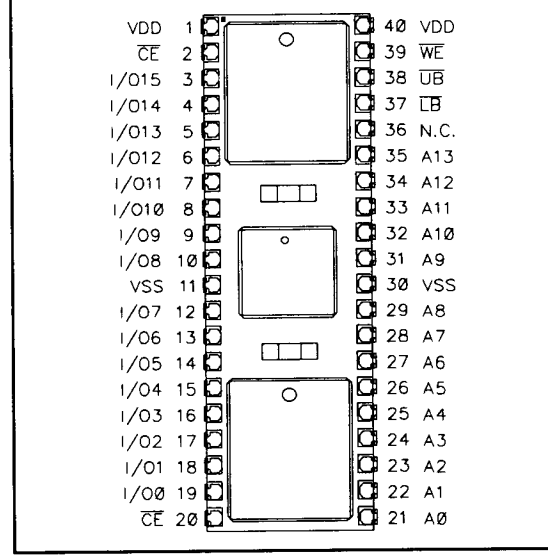
The DPS8M656 is a 256K bit Static Random Access Memory (SRAM), complete with memory interface logic and on-board capacitors, organized as 16K X 16 bits.

The DPS8M656 is ideally suited for high performance applications where either fast access time or low power consumption is required.

FEATURES:

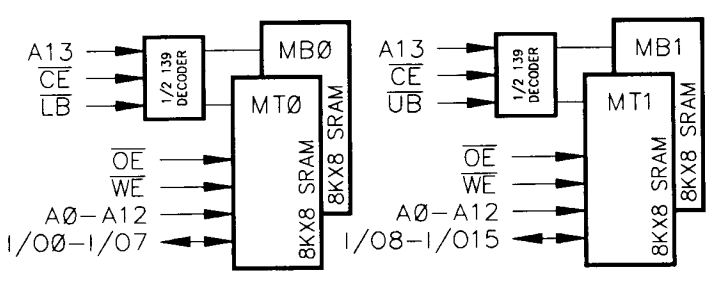
- Fast Access Times:
  35, 45, 55, 70, 85, 100, 120, 150ns (max.)
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible
- Common Data Input and Output
- Low Data Retention Voltage: 2.0V min.
- Single +5V Power Supply, ±10% Tolerance
- JEDEC Standard 40-Pin DIP Package
- Military Version Available with Devices Fully Compliant to MIL -STD-883C

PIN-OUT DIAGRAMS



PIN NAMES	
A0 - A13	Address Inputs
I/O0 - I/O15	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CE}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	I/O0 - I/O7	I/O8 - I/O15	Supply Current
Not Selected	H	X	X	X	X	HIGH-Z	HIGH-Z	Standby
Not Selected	X	H	H	X	X	HIGH-Z	HIGH-Z	Standby
D_{OUT} Disable	L	L	L	H	H	HIGH-Z	HIGH-Z	Active
Read Lower Block	L	L	H	H	L	D_{OUT}	HIGH-Z	Active
Read Upper Block	L	H	L	H	L	HIGH-Z	D_{OUT}	Active
Read All	L	L	L	H	L	D_{OUT}	D_{OUT}	Active
Write Lower Block	L	L	H	L	X	D_{IN}	HIGH-Z	Active
Write Upper Block	L	H	L	L	X	HIGH-Z	D_{IN}	Active
Write All	L	L	L	L	X	D_{IN}	D_{IN}	Active

H = HIGH, L = LOW and is X = Don't Care.

DPS8M656-35, -45, -55, -70, -85 DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-20	+20	-20	+20	-20	+20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	+20	-20	+20	-20	+20	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA Cycle = 0		400		400		400	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA,		640		640		640	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$\overline{CE}$ ≥ V_{DD} -0.2V, V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ 0.2V		70		70		70	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, Cycle = min.		120		120		120	mA
I_{CCDR2}	Data Retention Supply Current	$\overline{CE}$ ≥ V_{DR} -0.2V, V_{DR} = 2V		1.2		1.2		1.2	mA
I_{CCDR3}	Data Retention Supply Current	$\overline{CE}$ ≥ V_{DR} -0.2V, V_{DR} = 3V		2.4		2.4		2.4	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

DPS8M656-100, -120, -150 DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA, Cycle = 0		160		180		200	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		240		260		280	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$\overline{CE}$ ≥ V_{DD} -0.2V, V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ 0.2V		0.48		0.60		1.10	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, Cycle = min.		8		8		8	mA
I_{CCDR2}	Data Retention Supply Current	$\overline{CE}$ ≥ V_{DR} -0.2V, V_{DR} = 2V		100		200		400	µA
I_{CCDR3}	Data Retention Supply Current	$\overline{CE}$ ≥ V_{DR} -0.2V, V_{DR} = 3V		120		240		440	µA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V

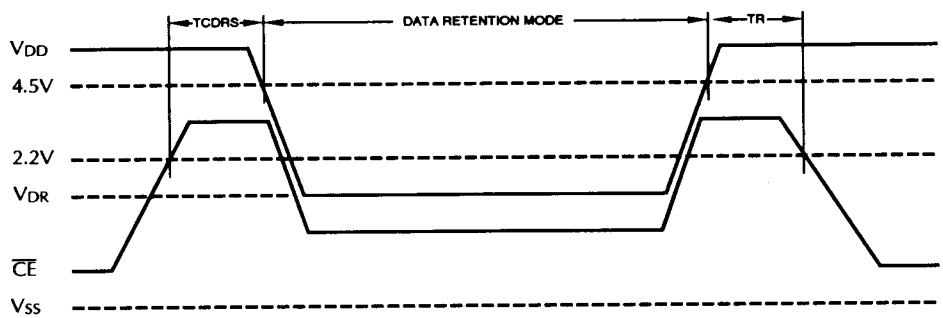
CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	45	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	45		
C_{OE}	Output Enable	40		
$C_{I/O}$	Data Input/Output	50		

ABSOLUTE MAXIMUM RATINGS[3]		
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	°C
V_{DD}	Supply Voltage	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5 to V_{DD} + 0.5	V

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA	-	0.4	V

DATA RETENTION CHARACTERISTICS						
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DD}$ -0.2V	2.0	5.0	5.5	V
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	t_{RC}			ns

DATA RETENTION CHARACTERISTICS



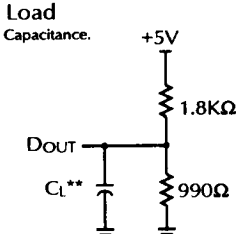
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input Timing Reference Levels	1.5V

* Transition measured from0.8V and 2.2V.

AC TEST CONDITIONS		
Load	C_L	Parameters Measured
1	100pF	except t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{WLZ}, t_{OLZ} and t_{OHZ}
2	5pF	t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{WLZ}, t_{OLZ} and t_{OHZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.

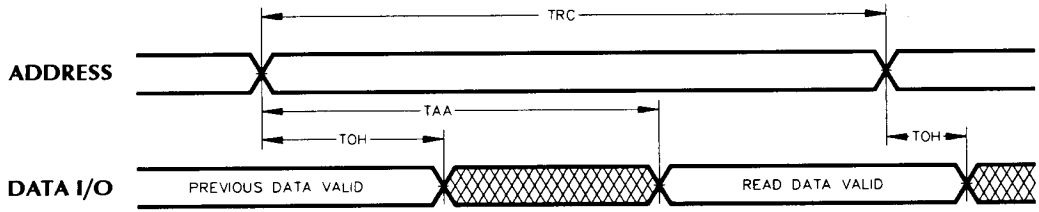


AC OPERATING CONDITIONS AND CHARACTERISTICS												
READ CYCLE: Over operating ranges												
No.	**Symbol**	**Parameter**	**-35**		**-45**		**-55**		**-70**		**-85**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
1	t_{RC}	Read Cycle Time	35		45		55		70		85		ns
2	t_{AA}	Address Access Time		35		45		55		70		85	ns
3	t_{CO}	Chip Enable to Output Valid		35		45		55		70		85	ns
4	t_{OV}	Output Enable to Output Valid		20		25		35		40		50	ns
5	t_{OH}	Output Hold from Address Change	3		3		3		3		5		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		15		20		25		30		35	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		15		20		25		30		35	ns
WRITE CYCLE: Over operating ranges [7]													
10	t_{WC}	Write Cycle Time	35		45		55		70		85		ns
11	t_{AW}	Address Valid to End of Write	30		40		50		65		75		ns
12	t_{CW}	Chip Enable to End of Write	30		40		50		65		75		ns
13	t_{DW}	Data Valid to End of Write	20		20		25		30		35		ns
14	t_{DH}	Data Hold Time	3		0		0		0		0		ns
15	t_{WP}	Write Pulse Width	30		40		45		55		65		ns
16	t_{AS}	Address Set-up Time**	0		0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		5		5		5		5		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		15		15		20		25		30	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS										
READ CYCLE: Over operating ranges										
No.	**Symbol**	**Parameter**	**-100**		**-120**		**-150**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
1	t_{RC}	Read Cycle Time	100		120		150		ns
2	t_{AA}	Address Access Time		100		120		150	ns
3	t_{CO}	Chip Enable to Output Valid		100		120		150	ns
4	t_{OV}	Output Enable to Output Valid		60		70		80	ns
5	t_{OH}	Output Hold from Address Change	10		10		10		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	10		10		10		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		45		50		55	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		35		40		50	ns
WRITE CYCLE: Over operating ranges [7]									
10	t_{WC}	Write Cycle Time	100		120		150		ns
11	t_{AW}	Address Valid to End of Write	90		100		120		ns
12	t_{CW}	Chip Enable to End of Write	90		100		120		ns
13	t_{DW}	Data Valid to End of Write	50		55		60		ns
14	t_{DH}	Data Hold Time	0		0		0		ns
15	t_{WP}	Write Pulse Width	70		75		80		ns
16	t_{AS}	Address Set-up Time**	0		0		0		ns
17	t_{AH}	Address Hold Time	5		5		5		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		35		40		45	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		ns

** Valid for both Read and Write Cycles.

READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



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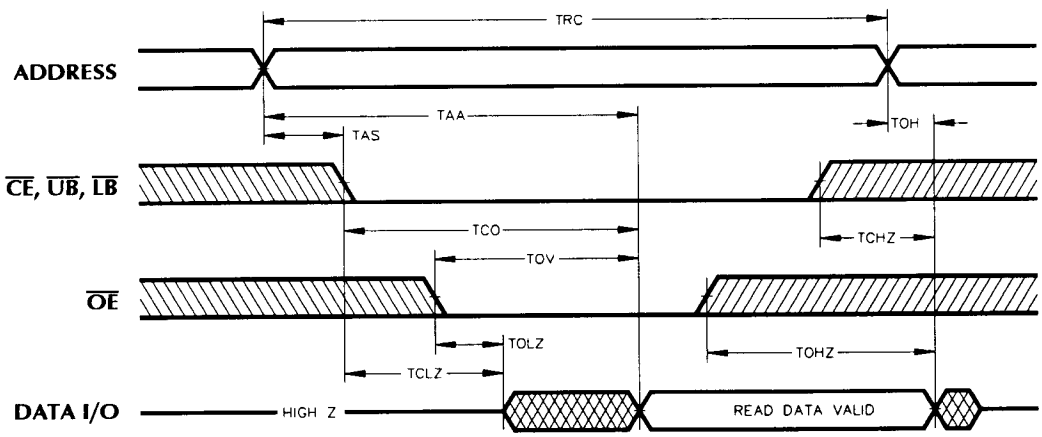
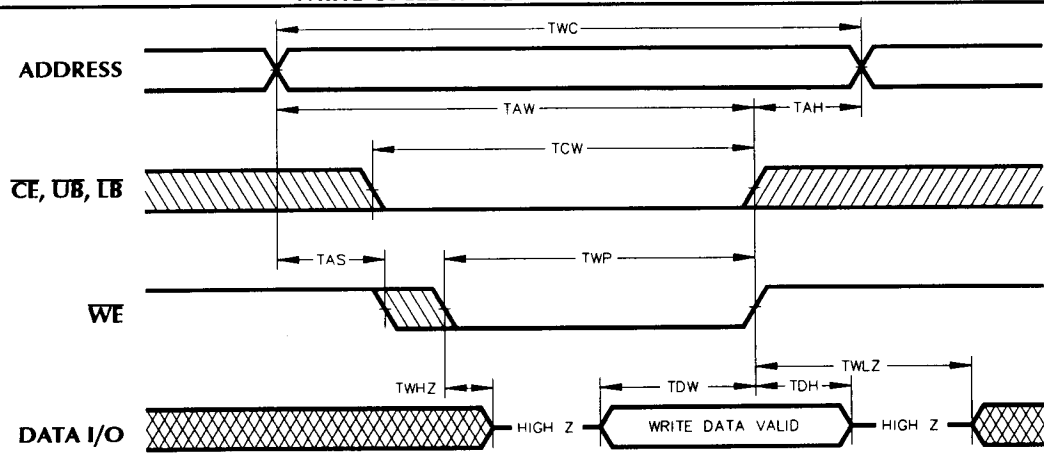
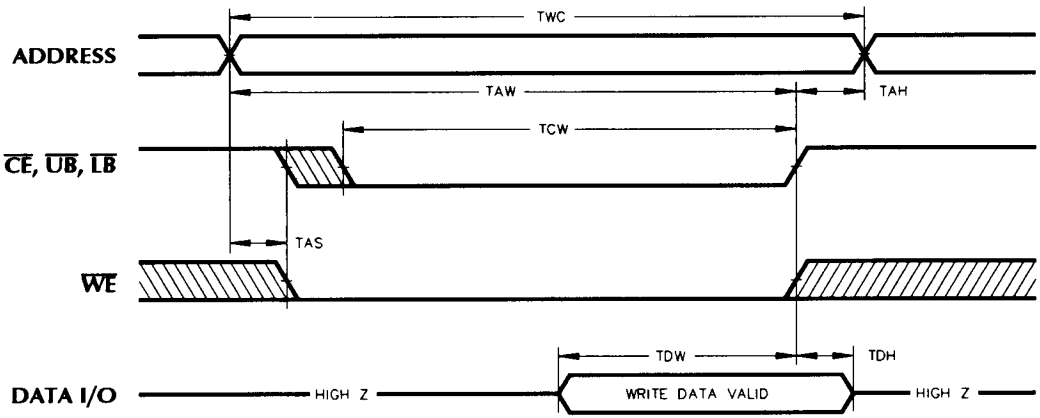
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min.= -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

ORDERING INFORMATION

DP — PREFIX

S8M656 – XXX X

S8M656 — DEVICE TYPE

XXX — SPEED

X — GRADE

C	COMMERCIAL	Ø°C to +7Ø°C
I	INDUSTRIAL	–4Ø°C to +85°C
M	MILITARY	–55°C to +125°C
B *	MIL–PROCESSED	–55°C to +125°C

35	35ns
45	45ns
55	55ns
7Ø	7Øns
85	85ns
1ØØ	1ØØns
12Ø	12Øns
15Ø	15Øns

16Kx16 CMOS SRAM 4Ø–PIN CERAMIC DIP

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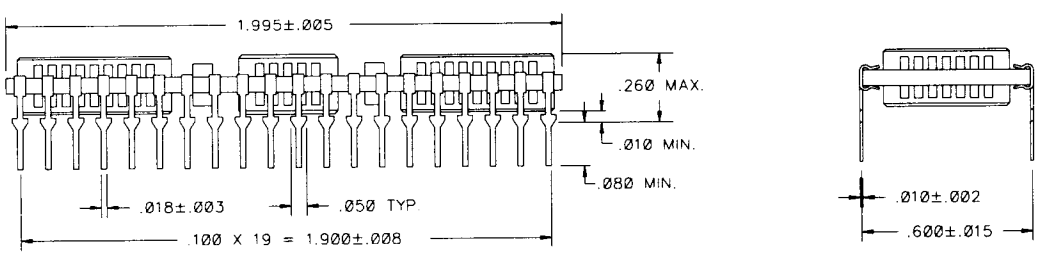
* B grade modules can be constructed with 883 devices.

MECHANICAL DRAWING



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