

Am7968/Am7969

T-75-37-05

TAXIchip™ Integrated Circuits
 (Transparent Asynchronous Xmitter - Receiver Interface)
 PRELIMINARY

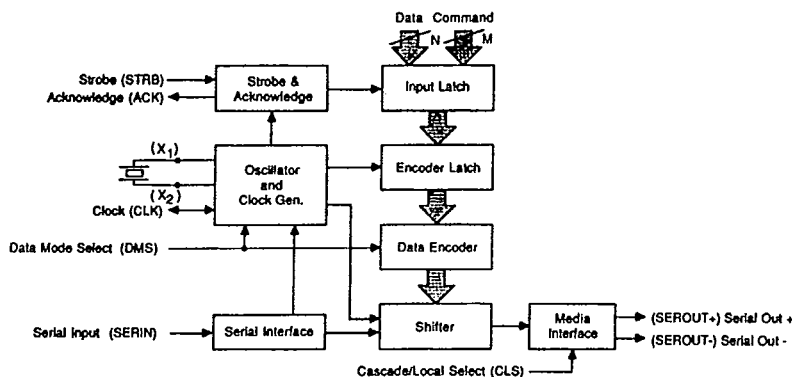
Am7968/Am7969

DISTINCTIVE CHARACTERISTICS

- Parallel TTL bus interface
 - Eight Data and four Command Pins
 - or nine Data and three Command Pins
 - or ten Data and two Command Pins
- Transparent synchronous serial link
 - +5 V ECL Serial I/O
 - AC or DC coupled
 - NRZI 4B/5B, 5B/6B encoding/decoding
- Drive coaxial cable directly or interface with fiber optic data links
- 32-100 Mbps (4-12.5 Mbytes/sec) data throughput
- Asynchronous input using STRB/ACK
- Automatic MUX/DEMUX of Data and Command
- Cascadable for longer patterns
- Complete on-chip PLL, Crystal Oscillator
- Single +5-V supply operation
- 28-pin PLCC, LCC or DIP

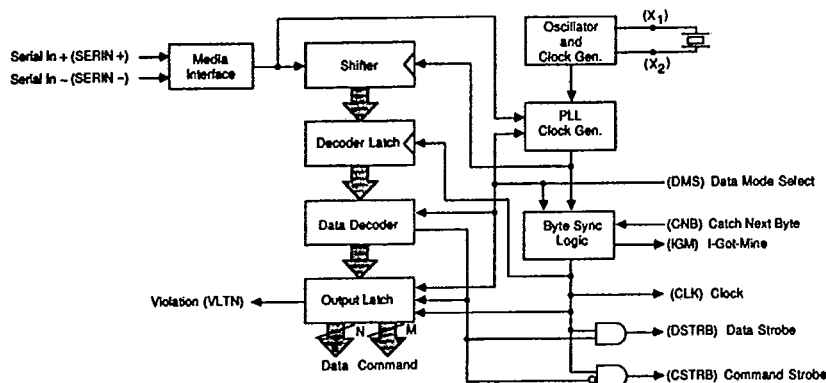
BLOCK DIAGRAMS

Am7968 TAXIchip Transmitter



BD007281

Am7969 TAXIchip Receiver



BD007291

Note: N can be 8, 9, or 10 bits
 Total of N + M = 12
 TAXIchip is a trademark of Advanced Micro Devices

To receive complete data sheet,
 order publication number at right

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 07370 C /0
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GENERAL DESCRIPTION

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The Am7968 TAXIchip Transmitter and Am7969 TAXIchip Receiver Chipset is a general-purpose interface for very high-speed (4-12.5 Mbytes/sec, 40-125 Mbaud serially) point-to-point communications over coaxial or fiber-optic media. TAXIs emulate a pseudo-parallel register. They load data into one side and output it on the other, except in this case, the "other" side is separated by a long serial link.

The speed of a TAXIchip system is adjustable over a range of frequencies, with parallel bus transfer rates of 4 Mbytes/sec at the low end, and up to 12.5 Mbytes/sec at the high end. The TAXIchip's flexible bus interface scheme accepts bytes that are either 8, 9, or 10 bits wide. Multiple TAXIs can also be cascaded to accommodate a wider data bus. Byte transfers can be Data or Command signalling.

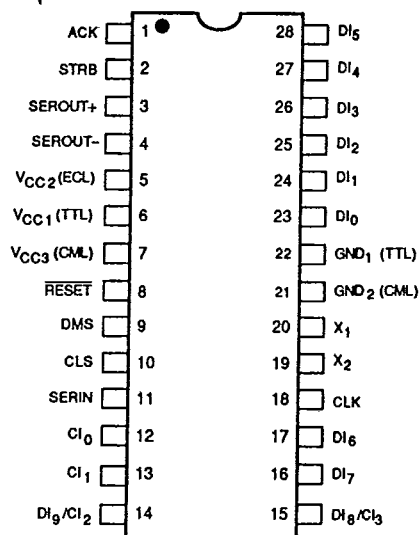
CONNECTION DIAGRAMS
Top View

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Am7968

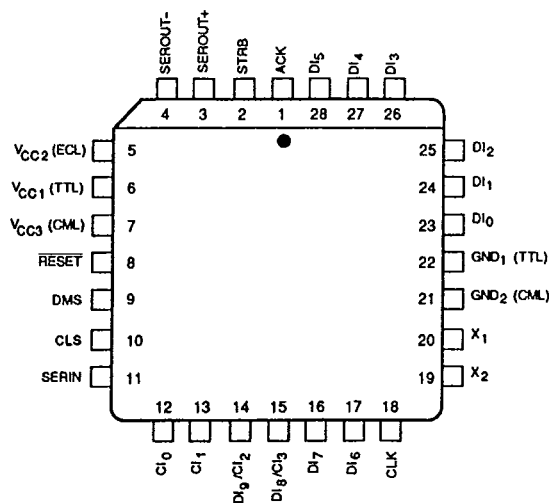
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DIPs



CD010772

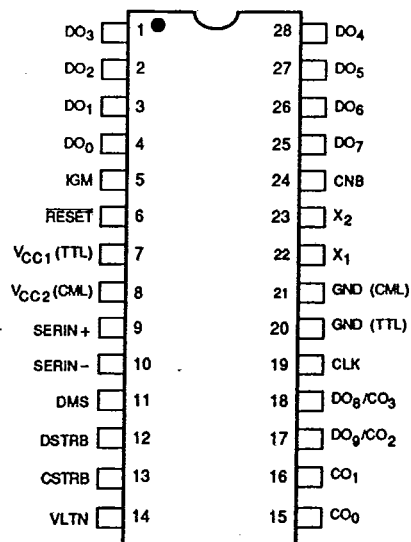
PLCC*



CD010782

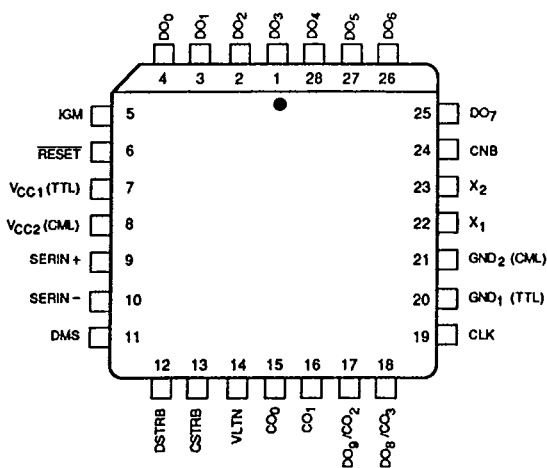
Am7969

DIPs



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PLCC*

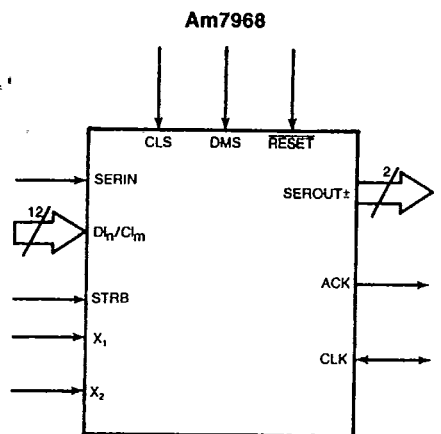


CD010802

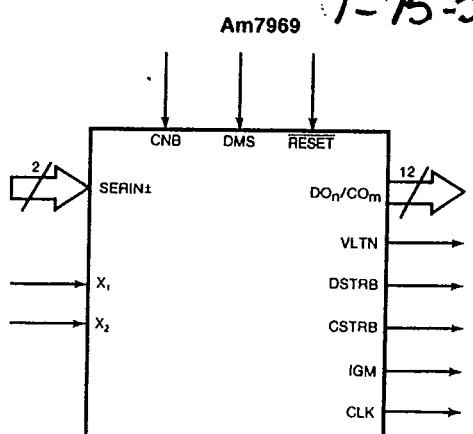
Note: Pin 1 is marked for orientation.

* Also available in 28-Pin Ceramic Leadless Chip Carrier; pinout identical to PLCC.

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VCC = Power Supply (3)
GND = Ground (2)

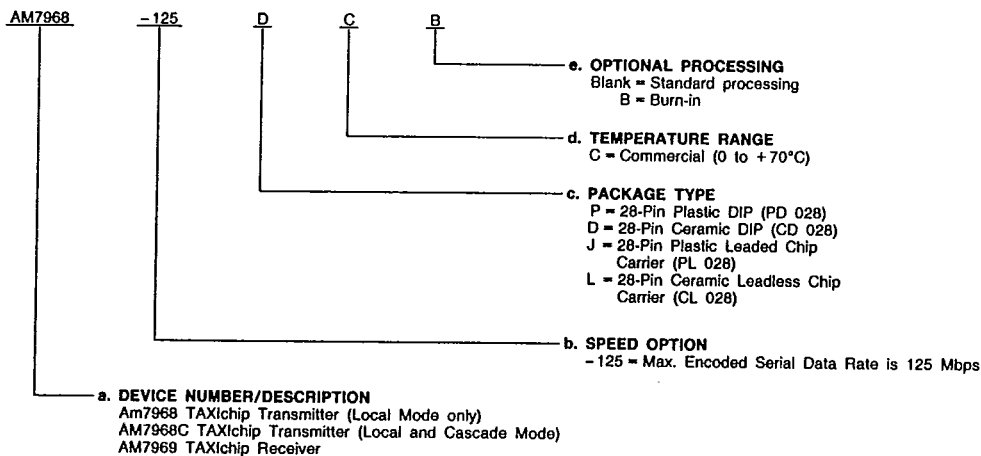


VCC = Power Supply (2)
GND = Ground (2)

ORDERING INFORMATION**Standard Products**

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM7968-125	PC, PCB, DC, DCB, JC
AM7969-125	PC, DC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

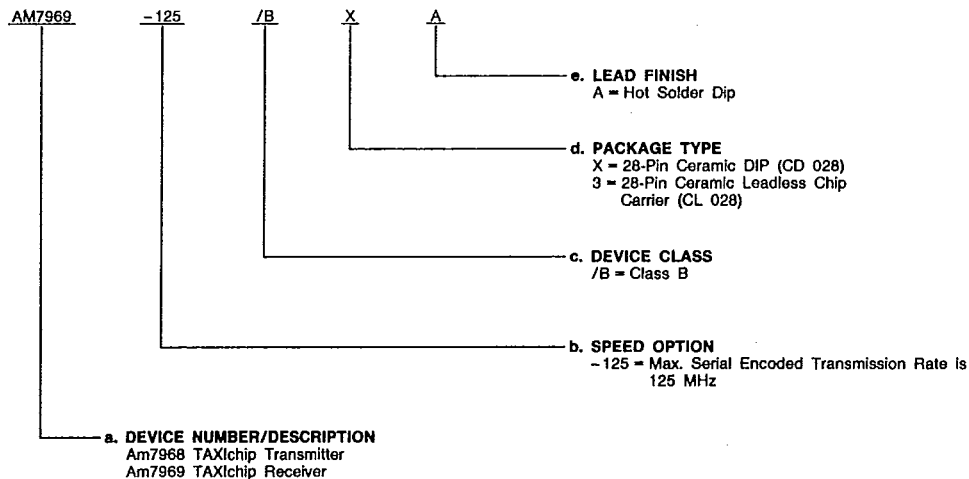
ORDERING INFORMATION (Cont'd.)

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APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM7968-125	/BXA, /B3A
AM7969-125	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.