1.1 Scope.

This specification covers the detail requirement for a complete, monolithic 16-bit digital-to-analog converter (DACPORT®) with an on-board reference and output amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD669SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-28

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{LL} to DGND ..... −0.3 V to +7 V
V_{CC} to AGND ..... −0.3 V to +17.0 V
V_{EE} to AGND ..... +0.3 V to −17.0 V
AGND to DGND ..... ±1 V
Digital Inputs (Pins 5–23) to DGND ..... −1.0 V to +7.0 V
REF IN to AGND ..... ±10.5 V
Span/Bipolar Offset to AGND ..... ±10.5 V
Ref Out, V_{OUT} ..... Indefinite Short to AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power Dissipation
To +60°C ..... 1000 mW
Derates above +60°C ..... 8.7 mW/°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JA} = 60°C/W
θ_{JC} = 27°C/W

DACPORT is a registered trademark of Analog Devices, Inc.

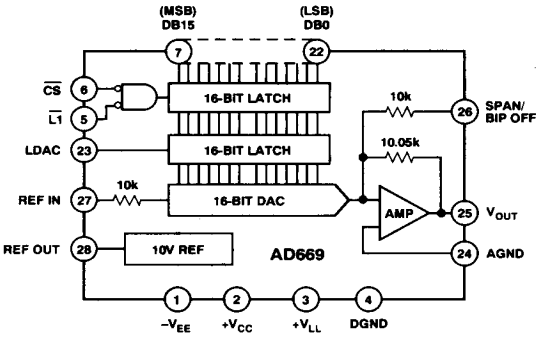
AD669—SPECIFICATIONS

Table 1.

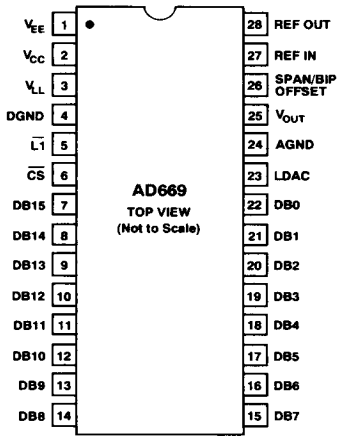
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition[1]	Units
Resolution	RES	−1	16				Bits
Relative Accuracy	RA	−1	2	2	4		±LSB max
Differential Nonlinearity	DNL	−1	2	2	4	Major Carry Errors	±LSB max
Gain Error[2, 4]	A_E	−1	0.10	0.10		All Bits On	±% of FSR max
Gain Drift[2]	TCA_E	−1			15	All Bits On	±ppm/°C max
Unipolar Offset Error	V_{OS}	−1	5	5		All Bits Off	±mV max
Unipolar Offset Tempco	TCV_{OS}	−1			3	All Bits Off	ppm/°C max
Bipolar Zero Error	B_{PZE}	−1	15	15		MSB On, All Others Off	±mV max
Bipolar Zero Tempco	TCB_{PZE}	−1			10	MSB On, All Others Off	ppm/°C max
Reference Output Voltage	V_{REF}	−1	9.98	9.98			V min
			10.02	10.02			V max
Reference Output Drift	TCV_{REF}	−1			15		ppm/°C
Reference Output External Current[3]	IV_{REF}	−1	2				mA min
Reference Output Capacitive Load	CLV_{REF}	−1	1000				pF max
Reference Input Resistance	R_{IN}	−1	7				kΩ min
			13				kΩ max
Bipolar Offset Input Resistance	$R_{IN}BPO$	−1	7				kΩ min
			13				kΩ max
Output Voltage Range	V_{OUT}	−1	0			Unipolar Range	V min
			+10				V max
			−10			Bipolar Range	V min
			+10				V max
Output Current	I_{OUT}	−1	5				mA min
Capacitive Load	C_L	−1	1000				pF max
Output Voltage Settling Time	t_{SL}	−1	13			20 V Step, T_A = +25°C	µs max
			8			20 V Step, T_A = +25°C	µs typ
			10			20 V Step, T_A = −55°C to +125°C	µs typ
			6			10 V Step, T_A = +25°C	µs typ
			8			10 V Step, T_A = −55°C to +125°C	µs typ
			2.5			LSB Step, T_A = −55°C to +125°C	µs typ
Digital Input High Voltage	V_{IH}	−1	2.0	2.0	2.0		V min
Digital Input Low Voltage	V_{IL}	−1	0.8	0.8	0.8		V max
Digital Input High Current	I_{IH}	−1	10	10	10	V_{IH} = +5.5 V	±µA max
Digital Input Low Current	I_{IL}	−1	10	10	10	V_{IL} = 0 V	±µA max
Power Supply Current	I_{LL}	−1	2	2		V_{IH} = +5.5 V, V_{IL} = 0.0	mA max
			7.5	7.5		V_{IH} = 2.4, V_{IL} = 0.4	
	I_{CC}	−1	18	18			
	I_{EE}	−1	−18	−18			
Power Supply Rejection Ratio	PSRR	−1	3	3		+14.25 V ≤ V_{CC} ≤ +15.75 V	±ppm/%
			3	3		−14.25 V ≤ V_{EE} ≤ −15.75 V	
			3	3		+4.5 V ≤ V_{LL} ≤ +5.5 V	

NOTES
[1]T_A = +25°C, @ V_{LL} = +5 V, V_{CC} = +15 V, V_{EE} = −15 V unless otherwise stated). For 16-bit resolution, 1 LSB = 0.0015% or FSR = 15 ppm of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR = 30 ppm of FSR. For 14-bit resolution 1 LSB = 0.006% of FSR = 60 ppm of FSR. FSR stands for Full-Scale Range and is 10 V for a 0 to +10 V span and 20 V for a −10 V to +10 V span.
[2]Gain error and gain drift are measured using the internal reference.
[3]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD669.
[4]Measured with fixed 50 Ω resistors. Eliminating these resistors increases the gain error by 0.25% (Unipolar Mode) or 0.50% (Bipolar Mode).

3.2.1 Functional Block Diagram and Terminal Assignments.

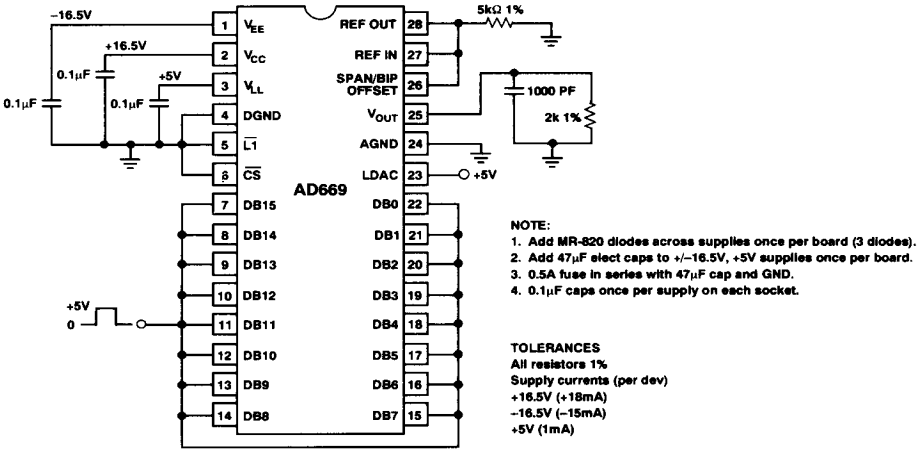


Q-Package



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).



4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

TIMING CHARACTERISTICS

V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V, V_{HI} = 2.4 V, V_{LO} = 0.4 V

Parameter	Limit +25°C	Limit −40°C to +85°C	Limit −55°C to +125°C	Units
(Figure 1a)				
$t_{\overline{CS}}$	40	50	55	ns min
$t_{\overline{L1}}$	40	50	55	ns min
t_{DS}	30	35	40	ns min
t_{DH}	10	10	15	ns min
t_{LH}	90	110	120	ns min
t_{LW}	40	45	45	ns min
(Figure 1b)				
t_{LOW}	130	150	165	ns min
t_{HIGH}	40	45	45	ns min
t_{DS}	120	140	150	ns min
t_{DH}	10	10	15	ns min

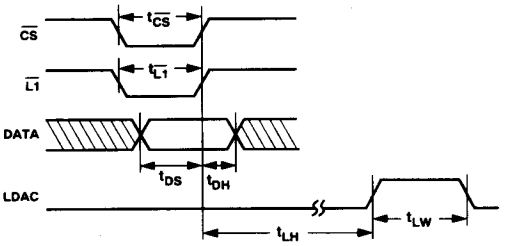


Figure 1a. AD669 Level Triggered Timing Diagram

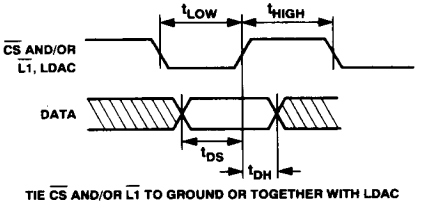


Figure 1b. AD669 Edge Triggered Timing Diagram

Table 2. AD669 Truth Table

$\overline{CS}$	$\overline{L1}$	LDAC	Operation
0	0	X	First Rank Enabled
X	1	X	First Rank Latched
1	X	X	First Rank Latched
X	X	1	Second Rank Enabled
X	X	0	Second Rank Latched
0	0	1	All Latches Transparent

"X" = Don't Care