

1.1 Scope.

This specification covers the detail requirements for a complete monolithic sample-and-hold circuit with internal holding capacitor and matched application resistors.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
– 1	AD585S(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-14	14-Pin Cerdip
E	E-20A	20-Pin LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supplies ($+V_S$, $-V_S$)	$\pm 18\text{V}$
Logic Inputs	$\pm V_S$
Analog Inputs	$\pm V_S$
R_{IN} , R_{FB} Pins	$\pm V_S$
Output Short Circuit to Ground	Indefinite
TTL Logic Reference Short Circuit to Ground	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C}/\text{W}$
 $\theta_{JA} = 110^\circ\text{C}/\text{W}$

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Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Test Condition ¹	Units
Offset Voltage	V _{OS}	−1	2	3	3	2		V _{OUT} = 0V	± mV max
Bias Current ²	I _B	−1	2	2	50			V _{IN} = 0V	± nA max
TTL Reference Output ³	V _{LREF}	−1	0.2	0.2	0.6			50μA Load	± V max
Logic Input High Voltage	V _{IH}	−1	2.0	2.0	2.0			Hold = V _{LREF}	V min
Logic Input Low Voltage	V _{IL}	−1	0.8	0.8	0.7			Hold = V _{LREF}	− V max
Logic Input Current	I _{IL}	−1	50	50	50			V _S = 18V	μA max
Supply Current	I _{SS}	−1	10	10	10			R _L = Infinite	mA max
Power Supply Rejection	PSRR	−1	70	70				+ V _S = 5V to 18V − V _S = −12V to −18V	dB min
Acquisition Time	t _{ACQ}	−1	3				3	10V step to 0.01%	μs max
Acquisition Time	t _{ACQ}	−1	5					20V step to 0.01%	μs max
Droop Rate ⁴	V _{DRP}	−1	1			1		V _{IN} = 0V	mV/ms max
Sample-to-Hold Offset	SH _{OS}	−1	3			3		V _{IN} = 0V	mV max
Application Resistor Mismatch	ΔRM	−1	0.3	0.3	0.3				% max
Common-Mode Rejection	CMRR	−1	80	80	77			V _{CM} = ±10V	dB min
Slew Current ⁵	I _{SL}	−1	850		600	850			μA min
Output Resistance ⁶	R _{OUT}	−1	0.05	0.05	0.1			I _{OUT} = ±10mA	Ω max
Output Current	I _{OUT}	−1	12 50	12 50				R _L = 100Ω	mA min mA max

NOTES

¹V_S = ±15V, C_H = Internal, R_L = Infinite, A = +1 unless otherwise noted.

²Not tested at −55°C.

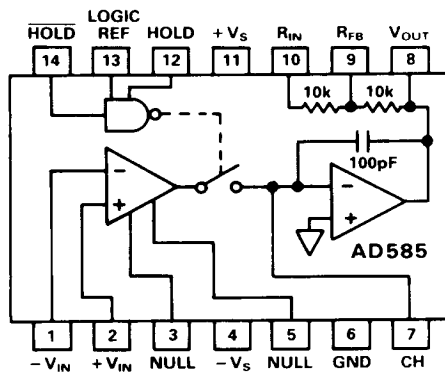
³Nominally 1.4V.

⁴Doubles every 10°C.

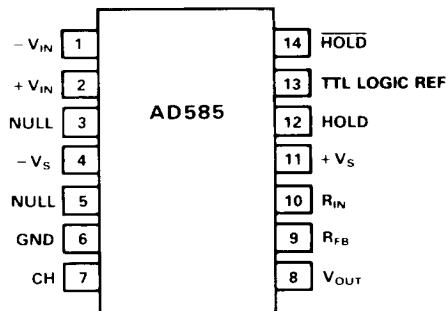
⁵V_{OUT} = 20V p-p. Slew rate = Slew Current/C_H.

⁶Tested in sample mode.

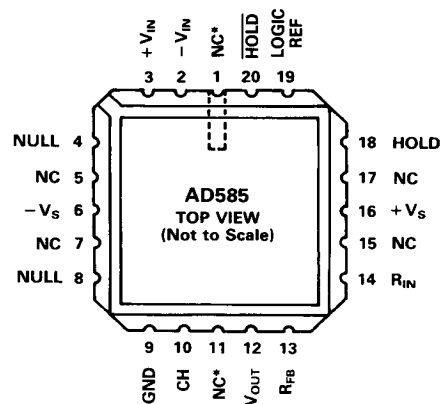
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)



*PERFORMANCE IS ENHANCED IF PINS 1 AND 11 ARE CONNECTED TO GROUND.

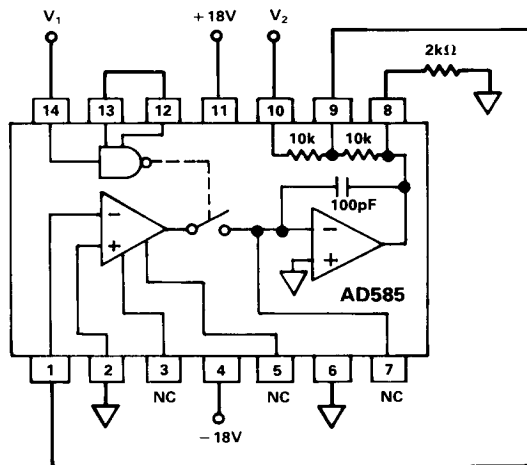
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (60).

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4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



$V_1 = 0 \text{ TO } 5\text{V}, 1\text{kHz SQUARE WAVE.}$
 $V_2 = 7\text{V rms}, F = 60\text{Hz}$