REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET	35																		
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS OF SHEETS				REV																
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary L. Gross

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
95-12-08

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 16-MEG, USER CONFIGURABLE FLASH EEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95625**

SHEET 1 OF 35

DESC FORM 193
JUL 94

5962-E252-95

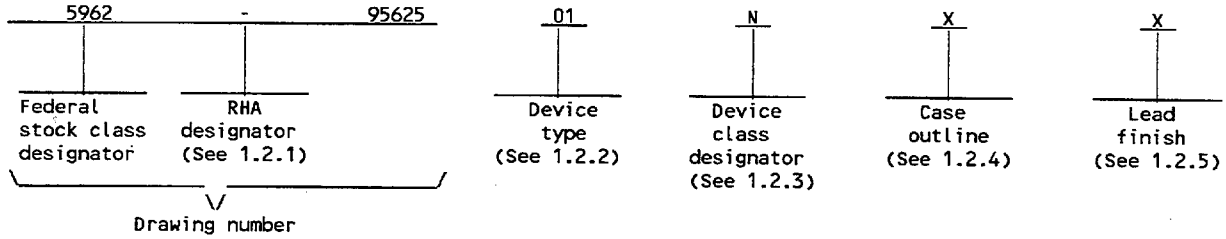
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0016229 730

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Three product assurance classes consisting of space application (device class V), military high reliability (device classes M and Q), and non-traditional military (device class N) with a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices." For device class N, the user is cautioned to assure that the device is appropriate for the application environment. When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes N, Q, and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function 2/	Access time	Endurance	Operating temp. range
01	28F016	16 MEG CMOS FLASH EEPROM	85 ns	100,000 cycles	-55°C to +125°C
02	28F016	16 MEG CMOS FLASH EEPROM	100 ns	100,000 cycles	-55°C to +125°C
03	28F016	16 MEG CMOS FLASH EEPROM	85 ns	100,000 cycles	-40°C to +125°C
04	28F016	16 MEG CMOS FLASH EEPROM	100 ns	100,000 cycles	-40°C to +125°C

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
N	Certification and qualification to MIL-I-38535 with a non-traditional performance environment 3/
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	56	plastic shrink small-outline package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-I-38535 for device classes N, Q, and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin and will also be listed in MIL-BUL-103 and QML-38535.
2/ This device is user configurable to either a 1 Meg X 16 or 2 Meg X 8 organization.
3/ Any device outside the traditional performance environment (i.e., an operating temperature range of -55°C to +125°C and which requires hermetic packaging).

1.3 Absolute maximum ratings. 4/

Supply voltage range (V_{CC}) 5/	-2.0 V dc to +7.0 V dc
Storage temperature range (T_{stg})	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 6/	+150°C
Thermal resistance, junction-to-case (Θ_{JC}) (case outline X)	20°C/W
Voltage on any pin with respect to ground 5/	-2.0 V dc to +7.0 V dc
V_{PP} supply voltage with respect to ground 5/ 7/	-0.2 V dc to +14.0 V dc
Output short circuit current 8/	100 mA
Data retention	10 years, minimum
Endurance (All device types)	100,000 cycles/byte, minimum

1.4 Recommended operating conditions. 9/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Alternate supply voltage range (V_{CC})	+3.15 V dc to +3.45 V dc
Device type 01 and 02 operating temperature range (T_{case})	-55°C to +125°C
Device type 03 and 04 operating temperature range (T_{case})	-40°C to +125°C
Low level input voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
High level input voltage range (V_{IH})	+2.0 V dc to V_{CC} +0.5 V dc
High level input voltage range, CMOS (V_{IH})	+2.0 V dc to V_{CC} +0.5 V dc
VPP supply voltage with respect to ground	11.4 V dc to 12.6 V dc

1.5 Digital logic testing for device classes N, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	99 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MICROCIRCUIT

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MICROCIRCUIT

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
5/ Minimum dc voltage on input or output pins is -0.5 V. During voltage transitions, inputs may undershoot to -2.0 V for periods less than 20 ns. Maximum dc voltage on input or output pins is V_{CC} +0.5 V. During voltage transitions outputs may overshoot to V_{CC} +2.0 V for periods less than 20 ns.
6/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
7/ Maximum dc input voltage on V_{PP} may overshoot to +14.0 V for periods less than 20 ns.
8/ No more than one output shorted at a time. Duration of short circuit should not be greater than 1 second.
9/ All voltages are referenced to V_{SS} (ground).

BULLETIN

MICROCIRCUIT

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

HANDBOOK

MICROCIRCUIT

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes N, Q, and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3 herein. When required, in screening (see 4.2 herein), or quality conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this document.

3.2.3.3 Command definitions. The command definitions table shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Switching test circuits and waveforms. The switching test circuits and waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes N, Q, and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes N, Q, and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes N, Q, and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-I-38535, appendix A).

3.11 Processing of flash EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Conditions of the supplied devices. Devices will be supplied in an unprogrammed or clear state. No provision will be made for supplying programmed devices.

3.11.2 Erasure of flash EEPROMs. When specified, devices shall be erased in accordance with procedures and characteristics specified in 4.5.1.

3.11.3 Programming of flash EEPROMs. When specified, devices shall be programmed in accordance with procedures and characteristics specified in 4.5.2.

3.11.4 Verification of state of flash EEPROMs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ or $4.75\ V \le V_{CC} \le 5.25\ V$ or $3.15\ V \le V_{CC} \le 3.45\ V$ unless otherwise specified. Also see note 1/.	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Input leakage current	I_{LI}	$V_{CC} = V_{CC}$ max, $V_{IN} = V_{CC}$ or GND 2/	1, 2, 3	All	-1	+1.0	µA
Output leakage current	I_{LO}	$V_{CC} = V_{CC}$ max, $V_{OUT} = V_{CC}$ or GND 2/	1, 2, 3	All	-10	+10	µA
V_{CC} standby current (TTL)	I_{CCS1}	$V_{CC} = V_{CC}$ max, CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP# = V_{IH} or V_{IL} 2/ 3/	1, 2, 3	All		4	mA
V_{CC} standby current (CMOS)	I_{CCS2}	CE_0#, CE_1#, RP# = V_{CC} ±0.2 V 2/ 3/ $V_{CC} = V_{CC}$ max, BYTE#, WP# = V_{CC} ±0.2 V or GND ±0.2 V	1, 2, 3	All		130	µA
V_{CC} read current	I_{CCR1}	CMOS: CE_0#, CE_1# = GND ±0.2 V, BYTE# = GND ±0.2 V or V_{CC} ±0.2 V, inputs = GND ±0.2 V or V_{CC} ±0.2 V $V_{CC} = V_{CC}$ max 2/ 3/ 4/ f = 10.0 Mhz, I_{OUT} = 0 mA	1, 2, 3	All		135	mA
		same as above except f = 8.0 Mhz and $3.15\ V \le V_{CC} \le 3.45\ V$				60	
		TTL: CE_0#, CE_1# = V_{IL}, f = 10.0 Mhz BYTE# = V_{IL} or V_{IH}, I_{OUT} = 0 mA, inputs = V_{IL} or V_{IH} $V_{CC} = V_{CC}$ max 2/ 3/ 4/		All		135	
		same as above except f = 8.0 Mhz and $3.15\ V \le V_{CC} \le 3.45\ V$				60	
V_{CC} read current	I_{CCR2}	Same as I_{CCR1} conditions except f = 5.0 MHz 2/ 3/ 4/ 5/	1, 2, 3	All		90	mA
		same as above except f = 4.0 Mhz and $3.15\ V \le V_{CC} \le 3.45\ V$				40	
V_{CC} deep powerdown current	I_{CCD}	RP# = GND ± 0.2 V BYTE# = V_{CC} ±0.2 V or GND ±0.2 V 2/	1, 2, 3	All		50	µA
V_{CC} write current	I_{CCW}	Word/Byte in progress V_{PP} = 12.0 V ± 5% 2/ 5/	1, 2, 3	All		35	mA
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$				12	
		Word/Byte in progress V_{PP} = 5.0 V ± 10% 2/ 5/		All		40	
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$				17	
V_{CC} block erase current	I_{CCE}	Word/Byte in progress V_{PP} = 12.0 V ± 5% 2/ 5/	1, 2, 3	All		25	mA
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$				12	
		Word/Byte in progress V_{PP} = 5.0 V ± 10% 2/ 5/		All		30	
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$				17	
V_{CC} erase suspend current	I_{CCES}	CE_0#, CE_1# = V_{IH} Block erase suspended 2/ 6/	1, 2, 3	All		10	mA
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$				6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ or $4.75\ V \le V_{CC} \le 5.25\ V$ or $3.15\ V \le V_{CC} \le 3.45\ V$ unless otherwise specified.	Group A Subgroups	Device type	Limits		Units
					Min	Max	
V_{PP} standby/read current	I_{PPS}	$V_{PP} \le V_{CC}$ 2/	1, 2, 3	All	-100	+100	µA
	I_{PPR}	$V_{PP} > V_{CC}$ 2/				200	
V_{PP} deep powerdown current	I_{PPD}	RP# = GND ± 0.2 V 2/	1, 2, 3	All		50	µA
V_{PP} write current	I_{PPW}	Word/Byte write in progress V_{PP} = 12.0 V ± 5% 2/ 5/	1, 2, 3	All		12	mA
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$				15	
		Word/Byte write in progress V_{PP} = 5.0 V ± 10% 2/ 5/				20	
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$				25	
V_{PP} block erase current 2/ 5/	I_{PPE}	Block erase in progress V_{PP} = 12.0 V ± 5%	1, 2, 3	All		10	mA
		Block erase in progress V_{PP} = 5.0 V ± 10%				20	
V_{PP} erase suspend current 2/	I_{PPES}	Block erase suspended $V_{PP} = V_{PPH1}$ or V_{PPH2}	1, 2, 3	All		200	µA
Low level input voltage 5/	V_{IL}		1, 2, 3	All	-0.5	0.8	V
		$3.15\ V \le V_{CC} \le 3.45\ V$			-0.3		
High level input voltage 5/	V_{IH}		1, 2, 3	All	2.0	V_{CC} + 0.5	V
		$3.15\ V \le V_{CC} \le 3.45\ V$				V_{CC} + 0.3	
Low level output voltage 5/	V_{OL}	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ min	1, 2, 3	All		0.45	V
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$				0.4	
High level output voltage 5/	V_{OH1}	I_{OH} = -2.5 mA, $V_{CC} = V_{CC}$ min	1, 2, 3	All	0.85 V_{CC}		V
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$			2.4 V_{CC}		
	V_{OH2}	I_{OH} = 100 µA, $V_{CC} = V_{CC}$ min		All	V_{CC} - 0.4		
		same as above except $3.15\ V \le V_{CC} \le 3.45\ V$			V_{CC} - 0.2		
V_{PP} write/erase lock voltage	V_{PPLK}	5/ 7/	1, 2, 3	All	0	1.8	V
V_{PP} during write/ erase operations	V_{PPH1}	7/	1, 2, 3	All	4.5	5.5	V
V_{PP} during write/ erase operations	V_{PPH2}	7/	1, 2, 3	All	11.4	12.6	V
V_{CC} write/erase lock voltage	V_{LKO}		1, 2, 3	All	1.8		V
Input capacitance 8/	C_{IN}	V_{IN} = 0 V, see 4.4.1c	4	All		8	pF
Output capacitance 8/	C_{OUT}	V_{OUT} = 0 V, see 4.4.1c	4	All		12	pF
Functional tests		See 4.4.1d	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ As specified below.	Group A Subgroups	Device type	Limits Min	Limits Max	Units
Read only operations; see figure 5 as applicable. 9/							
Read cycle time	t_{AVAV}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	80		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03	85		
				02,04	100		
		3.15 V ≤ V_{CC} ≤ 3.45 V		All	120		
Chip enable access time 10/	t_{ELQV}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		80	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03		85	
				02,04		100	
		3.15 V ≤ V_{CC} ≤ 3.45 V		All		120	
Address access time	t_{AVQV}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		80	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03		85	
				02,04		100	
		3.15 V ≤ V_{CC} ≤ 3.45 V		All		120	
Output enable access time 5/	t_{GLQV}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		30	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03		35	
				02,04		40	
		3.15 V ≤ V_{CC} ≤ 3.45 V		All		45	
Chip enable to output in low Z 5/	t_{ELQX}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V					
Chip disable to output in high Z 5/	t_{EHQZ}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		25	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03		30	
				02,04		35	
		3.15 V ≤ V_{CC} ≤ 3.45 V		All		50	
Output enable to output in low Z 5/	t_{GLQX}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V					
Output disable to output in high Z 5/	t_{GHQZ}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		25	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03		30	
				02,04		35	
		3.15 V ≤ V_{CC} ≤ 3.45 V		All		30	
Output hold from addresses, CE# or OE# change 5/ (whichever occurs first)	t_{OH}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V					
Address setup to CE# going low 5/	t_{AVEL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V					
Address setup to OE# going low 5/	t_{AVGL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V					
RP# to output delay	t_{PHQV}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		400	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03		480	
				02,04		480	
		3.15 V ≤ V_{CC} ≤ 3.45 V		All		620	
Byte enable to output delay 5/	t_{FLQV} t_{FHQV}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		80	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03		85	
				02,04		100	
		3.15 V ≤ V_{CC} ≤ 3.45 V		All		120	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ As specified below.	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Byte enable low to output in high Z 5/	t_{FLQZ}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		25	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03		30	
				02,04		35	
		3.15 V ≤ V_{CC} ≤ 3.45 V		All		30	
Chip enable low to byte enable high or low 5/	t_{ELFL} t_{ELFH}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		5	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
Power-up and reset timings; see figure 5 as applicable. 11/							
RP# low to V_{CC} at 4.5 v minimum (to V_{CC} at 3.15 v minimum) 12/	t_{PL5V} t_{PL3V}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		µs
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
Address valid to data valid for V_{CC} 13/	t_{AVQV}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		80	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All		85	
		3.15 V ≤ V_{CC} ≤ 3.45 V				120	
RP# high to data valid for V_{CC} 13/	t_{PHQV}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		480	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V				620	
RP# low to 3/5# low (high) 14/	t_{PLYL} t_{PLYH}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		µs
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V					
3/5# low (high) to RP# high 14/	t_{YLPH} t_{YHPH}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	2		µs
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V					
RP# high to CE# low (3.3 V V_{CC}) 13/	t_{PHEL3}	3.15 V ≤ V_{CC} ≤ 3.45 V	9, 10, 11	All	405		ns
RP# high to CE# low (5.0 V V_{CC}) 13/	t_{PHEL5}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	330		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ As specified below.	Group A Subgroups	Device type	Limits Min	Limits Max	Units
WE# controlled command write operations; see figure 5 as applicable. 9/ 15/							
Write cycle time	t_{AVAV}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	80		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		01,03	85		
				02,04	100		
		$3.15\ V \le V_{CC} \le 3.45\ V$		All	120		
V_{PP} setup to WE# going high 5/	t_{VPWH1} t_{VPWH2}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	100		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
RP# setup to CE# going low 8/	t_{PHEL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	480		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
CE# setup to WE# going low 5/	t_{ELWL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	0		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		All			
		$3.15\ V \le V_{CC} \le 3.45\ V$			10		
Address setup to WE# going high 16/ 17/	t_{AVWH}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	50		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		All			
		$3.15\ V \le V_{CC} \le 3.45\ V$			75		
Data setup to WE# going high 16/ 17/	t_{DVWH}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	50		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		All			
		$3.15\ V \le V_{CC} \le 3.45\ V$			75		
WE# pulse width	t_{WLWH}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	50		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		01,03	60		
				02,04	70		
		$3.15\ V \le V_{CC} \le 3.45\ V$		All	75		
Data hold from WE# high 16/	t_{WHDX}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	10		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
Address hold from WE# high 16/	t_{WHAX}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	10		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
CE# hold from WE# high 5/	t_{WHEH}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	10		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
WE# pulse width high	t_{WHWL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	30		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		All			
		$3.15\ V \le V_{CC} \le 3.45\ V$			45		
Read recovery before write 5/	t_{GHWL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	0		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
WE# high to RY/BY# going low 5/	t_{WHRL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03		100	ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
RP# hold from valid status register (CSR, GSR, BSR) data and RY/BY# high 5/	t_{RHPL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	0		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
RP# high recovery to WE# going low 5/	t_{PHWL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	1		µs
		$4.5\ V \le V_{CC} \le 5.5\ V$		All			
		$3.15\ V \le V_{CC} \le 3.45\ V$			480		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ As specified below.	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Write recovery before read 5/	t_{WHGL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	60		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		All	65		
		$3.15\ V \le V_{CC} \le 3.45\ V$			95		
V_{PP} hold from valid status register (CSR, GSR, BSR) data and RY/BY# high 5/	t_{QVVL1} t_{QVVL2}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	0		
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
Duration of word/byte write operation 5/ 18/ 19/	t_{WHQV1}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	4.5		µs
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
Duration of block erase operation 5/ 18/	t_{WHQV2}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	0.3	10	sec
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
CE# controlled command write operations; see figure 5 as applicable. 9/ 15/							
Write cycle time	t_{AVAV}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	80		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		01,03	85		
				02,04	100		
		$3.15\ V \le V_{CC} \le 3.45\ V$		All	120		
V_{PP} setup to CE# going high 5/	t_{VPEH1} t_{VPEH2}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	100		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
RP# setup to WE# going low 5/	t_{PHWL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	480		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
WE# setup to CE# going low 5/	t_{WLEL}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	0		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			
Address setup to CE# going high 16/ 20/	t_{AVEH}	$4.5\ V \le V_{CC} \le 5.5\ V$	9, 10, 11	All	50		ns
		$4.75\ V \le V_{CC} \le 5.25\ V$		01,03			
		$3.15\ V \le V_{CC} \le 3.45\ V$		All	75		
Data setup to CE# going high 16/ 20/	t_{DVEH}	$4.5\ V \le V_{CC} \le 5.5\ V$	9, 10, 11	All	50		ns
		$4.75\ V \le V_{CC} \le 5.25\ V$		01,03			
		$3.15\ V \le V_{CC} \le 3.45\ V$		All	75		
CE# pulse width	t_{ELEH}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	50		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		01,03	60		
				02,04	70		
		$3.15\ V \le V_{CC} \le 3.45\ V$		All	75		
Data hold from CE# high 16/	t_{EHDX}	$4.75\ V \le V_{CC} \le 5.25\ V$ $4.5\ V \le V_{CC} \le 5.5\ V$	9, 10, 11	01,03	0		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$		02,04	10		
		$3.15\ V \le V_{CC} \le 3.45\ V$		All			
Address hold from CE# high 16/	t_{EHAX}	$4.75\ V \le V_{CC} \le 5.25\ V$	9, 10, 11	01,03	10		ns
		$4.5\ V \le V_{CC} \le 5.5\ V$ $3.15\ V \le V_{CC} \le 3.45\ V$		All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ As specified below.	Group A Subgroups	Device type	Limits		Units
					Min	Max	
WE# hold from CE# high 5/	t_{EHWH}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	10		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
CE# pulse width high	t_{EHEL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	30		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V			45		
Read recovery before write 5/	t_{GHEL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
CE# high to RY/BY# going low 5/	t_{EHRL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03		100	ns
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
RP# hold from valid status register (CSR, GSR, BSR) data and RY/BY# high 5/	t_{RHPL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
RP# high recovery to CE# going low 5/	t_{PHEL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	1		µs
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V			480		ns
Write recovery before read	t_{EHGL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	60		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		01,03			
				02,04	65		
		3.15 V ≤ V_{CC} ≤ 3.45 V		All	95		
V_{PP} hold from valid status register (CSR, GSR, BSR) data at RY/BY# high 5/	t_{QVVL1} t_{QVVL2}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0		µs
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
Duration of word/byte write operation 5/ 18/ 19/	t_{EHQV1}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	4.5		µs
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
					5		
Duration of block erase operation 5/ 18/	t_{EHQV2}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	0.3	10	sec
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			
WE# controlled page buffer write operations; see figure 5 as applicable. 9/ 21/ 22/							
Address setup to WE# going low	t_{AVWL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	15		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V		All			
		3.15 V ≤ V_{CC} ≤ 3.45 V			25		
CE# controlled page buffer write operations; see figure 5 as applicable. 9/ 22/ 23/							
Address setup to CE# going low	t_{AVEL}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	01,03	15		ns
		4.5 V ≤ V_{CC} ≤ 5.5 V 3.15 V ≤ V_{CC} ≤ 3.45 V		All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ All device types are capable of being operated at 5.0 V ± 10%, 5.0 V ± 5%, or 3.3 V ± 5% except devices 02 and 04, which are not available at the 5.0 V ± 5% option. When these options present differences in timing and electrical limits, it will be noted. For device types 01 and 03, T_C = -55°C to +125°C; for device types 02 and 04, T_C = -40°C to +125°C. Case temperatures are instant on.
2/ All currents are in RMS unless otherwise noted.
3/ CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL inputs are either V_{IL} or V_{IH}.
4/ Automatic power saving reduces I_{CCR} to less than 1 mA in static operation.
5/ Periodically sampled and not 100-percent tested, but shall be guaranteed to the limits specified in table I.
6/ I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
7/ Block erases, word/byte writes, and lock block operations are inhibited when $V_{PP} \leq V_{PPLK}$ and not guaranteed in the ranges between V_{PPLK} (max) and V_{PPH1} (min), between V_{PPH1} (max) and V_{PPH2} (min) and above V_{PPH2} (max).
8/ Parameters shall be tested as part of device initial characterization and after design and process change and shall be guaranteed to the limits specified in table I for all lots not specifically tested.
9/ CE_*# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
10/ OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE#, without impacting t_{ELQV}.
11/ CE_0#, CE_1#, and OE# are switched low after power-up.
12/ The power supply may start to switch concurrently with RP# going low.
13/ The address access time and RP# high to data valid time are shown for 5.0 V V_{CC} operation. Refer to the ac characteristics-read-only operations, 3.3 V V_{CC}.
14/ The t_{5VPH} and/or t_{3VPH} times must be strictly followed to guarantee all other read and write specifications for the device.
15/ Read timings during write and erase are the same as for normal read.
16/ Refer to command definitions table for valid address and data values.
17/ Address and data are latched on the rising edge of WE# for all command write operations.
18/ Write/erase durations are measured to valid status data.
19/ Word/byte write operations are typically performed with one programming pulse.
20/ Address and data are latched on the rising edge of CE# for all command write operations.
21/ Address must be valid during the entire WE# low pulse.
22/ See the high speed ac input/output reference waveforms and ac testing load circuit.
23/ Address must be valid during the entire CE# low pulse.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the specified temperature range (see 1.2.2). The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the specified temperature range (see 1.2.2). The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes N, Q, and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.5.2 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot.

c. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D) using the circuit referenced (see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. After the completion of all screening, the device shall be erased and verified prior to delivery.

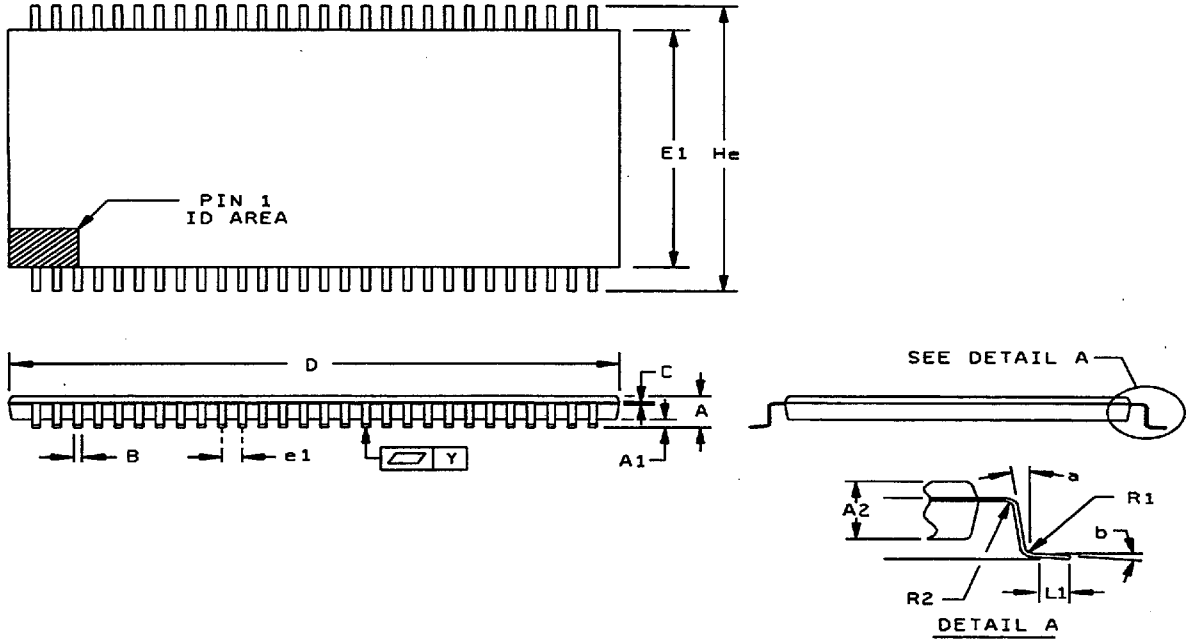
4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

Case X



Symbol	Millimeters		Symbol	Millimeters	
	Minimum	Maximum		Minimum	Maximum
A		1.90	H_e	15.70	16.30
A1	0.47		N	56 pins	
A2	1.18	1.38	L_1	0.75	0.85
B	0.25	0.40	Y		0.10
C	0.13	0.20	a	2°	4°
D	23.40	24.00	b	3°	5°
E	13.10	13.50	R1	0.15	0.25
e_1	0.80 basic		R2	0.15	0.25

NOTES:
1. Terminal one shall be identified by a mechanical index on the lead or body, or a mark on the top surface within the region shown.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 millimeters per side.
3. Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 millimeters per side.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 millimeters total in excess of the "b" dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 millimeters for 0.4 and 0.5 millimeter pitch packages.

FIGURE 1. Case outline.

Device types	All		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CE_0#	33	DQ_2
2	A_{12}	34	NC
3	A_{13}	35	NC
4	A_{14}	36	BYTE#
5	A_{15}	37	A_0
6	3/5#	38	DQ_0
7	CE_1#	39	DQ_8
8	NC	40	DQ_1
9	A_{20}	41	DQ_9
10	A_{19}	42	V_{CC}
11	A_{18}	43	A_8
12	A_{17}	44	V_{SS}
13	A_{16}	45	A_7
14	V_{CC}	46	A_6
15	V_{SS}	47	A_5
16	DQ_6	48	A_4
17	DQ_{14}	49	A_3
18	DQ_7	50	A_2
19	DQ_{15}	51	A_1
20	RY/BY#	52	A_9
21	OE#	53	A_{10}
22	WE#	54	A_{11}
23	WP#	55	RP#
24	DQ_{13}	56	V_{PP}
25	DQ_5		
26	DQ_{12}		
27	DQ_4		
28	V_{CC}		
29	V_{SS}		
30	DQ_{11}		
31	DQ_3		
32	DQ_{10}		

FIGURE 2. Terminal connections.

Bus operations for word-wide mode (BYTE# = V_{IH})

Operation	Notes	A_1	RP#	CE_1#	CE_0#	OE#	WE#	RY/BY#	DQ_0 - DQ_{15}
Read	1/ 2/ 3/	X	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	Data out
Output disable	1/ 4/ 3/	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	3-state
Standby	1/ 4/ 3/	X	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	3-state
Deep power-down	1/ 5/	X	V_{IL}	X	X	X	X	V_{OH}	3-state
Manufacturer code	6/	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{OH}	0089H
Device code	6/	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{OH}	66A0H
Write	1/ 4/ 7/	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	Data in

Bus operations for byte-wide mode (BYTE# = V_{IL})

Operation	Notes	A_0	RP#	CE_1#	CE_0#	OE#	WE#	RY/BY#	DQ_0 - DQ_7
Read	1/ 2/ 3/	X	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	Data out
Output disable	1/ 4/ 3/	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	3-state
Standby	1/ 4/ 3/	X	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	3-state
Deep power-down	1/ 5/	X	V_{IL}	X	X	X	X	V_{OH}	3-state
Manufacturer code	6/	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{OH}	89H
Device code	6/	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{OH}	A0H
Write	1/ 4/ 7/	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	Data in

1/ X can be V_{IL} or V_{IH} for control pins and addresses except for RY/BY# , which is either V_{OL} or V_{OH}.
2/ RY/BY# output is open drain. When the WSM is ready, erase is suspended or the device is in deep power-down mode. RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
3/ RY/BY# may be at V_{OL} while the WSM is busy performing various operations. For example, a status register read during a write operation.
4/ While the WSM is running, RY/BY# in level-mode (default) stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
5/ RP# at GND $\pm$ 0.2 V ensures the lowest deep power-down current.
6/ A_0 and A_1 at V_{IL} provide device manufacturer codes in x 8 and x 16 modes respectively. A_0 and A_1 at V_{IH} provide device identification codes in x 8 and x 16 modes respectively. All other addresses are set to zero.
7/ Commands for erase, data write, or lock-block operations can only be completed successfully when V_{PP} = V_{PPH1} or V_{PP} = V_{PPH2}.

FIGURE 3. Truth tables.

Command definitions 1/

Command	Mode	Notes	First BUS cycle			Second BUS cycle			Third BUS cycle		
			Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data
Read extended status register		2/	Write	X	XX71H	Read	RA	GSRD BSRD			
Page buffer swap		3/	Write	X	XX72H						
Read page buffer			Write	X	XX75H	Read	PA	PD			
Single load to page buffer			Write	X	XX74H	Write	PA	PD			
Sequential load to page buffer	x 8	4/5/6/	Write	X	XXE0H	Write	X	BCL	Write	X	BCH
	x 16	4/5/6/ 7/8/	Write	X	XXE0H	Write	X	WCL	Write	X	WCH
Page buffer write to flash	x 8	4/6/ 9/10/	Write	X	XX0CH	Write	A_0	BC(L,H)	Write	WA	BC(H,L)
	x 16	4/6/7/ 8/	Write	X	XX0CH	Write	X	WCL	Write	WA	WCH
Two-byte write	x 8	9/	Write	X	XXFBH	Write	A_0	WD(L,H)	Write	WA	WD(H,L)
Lock block/confirm			Write	X	XX77H	Write	BA	XXD0H			
Upload status bits/confirm		11/	Write	X	XX97H	Write	X	XXD0H			
Upload device information/confirm		12/	Write	X	XX99H	Write	X	XXD0H	Read	PA	PD
Erase all unlocked blocks/confirm			Write	X	XXA7H	Write	X	XXD0H			
RY/BY# enable to level-mode		13/	Write	X	XX96H	Write	X	XX01H			
RY/BY# pulse-on-write		13/	Write	X	XX96H	Write	X	XX02H			
RY/BY# pulse-on-erase		13/	Write	X	XX96H	Write	X	XX03H			
RY/BY# disable		13/	Write	X	XX96H	Write	X	XX04H			
RY/BY# pulse-on-write/erase		13/	Write	X	XX96H	Write	X	XX05H			
Sleep			Write	X	XXF0H						
Abort			Write	X	XX80H						

Address		Data	
BA =	Block address	AD =	Array data
PA =	Page buffer address	PD =	Page buffer data
RA =	Extended register address	BSRD =	BSR data
WA =	Write address	GSRD =	GSR data
X =	Don't care	WC(L,H) =	Word count (low, high)
		BC(L,H) =	Byte count (low, high)
		WD(L,H) =	Write data (low, high)

FIGURE 3. Truth tables - Continued.

NOTES:

1/ To ensure that the devices power consumption during sleep mode reaches the deep power-down current level, the system also needs to de-select the chip by taking either or both CE_0# or CE_1# high.
2/ RA can be the GSR address or any BSR address.
3/ This command allows the user to swap between available page buffers (0 or 1).
4/ BCH/WCH must be at 00H for this product because of the 256-byte (128-word) page buffer size, and to avoid writing the page buffer contents to more than one 256-byte segment within an array block. They are simply shown for future page buffer expandability.
5/ PA and PD (whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle, which is not shown.
6/ BCL = 00H corresponds to a byte count of 1. Similarly, WCL = 00H corresponds to a word count of 1.
7/ In x 16 mode, only the lower byte DQ_{0-7} is used for WCL and WCH. The upper byte DQ_{8-15} is a don't care.
8/ The upper byte of the data bus (DQ_{8-15}) during command writes is a "don't care" in x 16 operation of the device.
9/ A_0 is automatically complemented to load second byte of data. BYTE# must be at V_{IL}. A_0 value determines which WD/BC is supplied first: A_0 = 0 looks at the WDL/BCL, A_0 = 1 looks at the WDH/BCH.
10/ Write address, WA, is the destination address in the flash array which must match the source address in the page buffer.
11/ Upon device power-up, all BSR lock-bits come up locked. The upload status bits command must be written to reflect the actual lock-bit status.
12/ After writing the upload device information command and the confirm command, the following information is output at page buffer addresses specified below:

Address	Device information
06H, 07H (Byte mode)	Revision number
03H (Word mode)	Revision number
1EH (Byte mode)	Configuration code
0FH (DQ_{0-7}) (Word mode)	Configuration code
1FH (Byte mode)	Proliferation code (01H)
0FH (DQ_{8-15}) (Word mode)	Proliferation code (01H)

A page buffer swap followed by a page buffer read sequence is necessary to access this information. The contents of all other page buffer locations, after the upload device information command is written, are reserved for future implementation. See figure 3 for description of the device configuration code. This code also corresponds to data written to the device after writing the RY/BY# reconfiguration command.
13/ These commands reconfigure RY/BY output to one of two pulse-modes or enable and disable the RY/BY# function.

FIGURE 3. Truth tables - Continued.

Status register definitions

	Compatible status register 1/ 2/ 3/ 4/							
	7	6	5	4	3	2	1	0
	WRITE STATE MACHINE STATUS 1/ (WSMS)	ERASE SUSPEND STATUS (ESS)	ERASE STATUS 2/ (ES)	DATA WRITE STATUS (DWS)	V_{PP} STATUS 3/ (V_{PPS})	R	R	R
1 =	Ready	Erase suspended	Error in block erasure	Error in data write	V_{PP} error detect; operation abort	4/	4/	4/
0 =	Busy	Erase in progress/completed	Successful block erase	Successful data write	V_{PP} okay	4/	4/	4/

1/ RY/BY# output or the write state machine status bit must first be checked to determine completion of an operation (erase, erase suspend, or data write) before the appropriate status bit (ESS, ES, or DWS) is checked for success.
2/ If DWS and ES are set to "1's" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.
3/ The V_{PP} status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The write state machine interrogates the V_{PP} level only after the data write or erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} status bit is not guaranteed to report accurate feedback between V_{PPLK} (max.) and V_{PPH1} (min.) and between V_{PPH1} (max.) and V_{PPH2} (min.).
4/ Status registers 2 - 0 are reserved for future use and should be masked out when polling the CSR.

		Global status register 1/								
		7	6	5	4		3	2	1	0
		WRITE STATE MACHINE STATUS 2/ (WSMS)	OPERATION SUSPEND STATUS (OSS)	DEVICE OPERATION STATUS (DOS)	DEVICE SLEEP STATUS (DSS)	MATRIX 5/4	QUEUE STATUS (QS)	PAGE BUFFER AVAILABLE STATUS 7/ (PBAS)	PAGE BUFFER STATUS (PBS)	PAGE BUFFER SELECT STATUS (PBSS)
1 =	0 0 = 3/	Ready	Operation suspended	Operation unsuccessful	Device in sleep	Operation successful or currently running 4/	Queue full	One or two page buffers available	Selected page buffer ready	Page buffer 1 selected
	0 1 = 3/					Device in sleep mode or pending sleep 5/				
0 =	1 0 = 3/	Busy	Operation in progress/ completed	Operation successful or currently running	Device not in sleep	Operation unsuccessful	Queue available	No page buffer available	Selected page buffer busy 8/	Page buffer 0 selected
	1 1 = 3/					Operation unsuccessful or aborted 6/				

1/ When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.
2/ RY/BY# or the WSMS bit must be checked to determine completion of an operation (block lock, suspend, any RY/BY# reconfiguration, upload status bits, erase or data write) before the appropriate status bit (OSS or DOS)is checked for success.
3/ These logic outputs apply to MATRIX 5/4 only.
4/ If operation currently running, then GSR.7 = 0.
5/ If device pending sleep, then GSR.7 = 0.
6/ Operation aborted: unsuccessful due to abort command.
7/ The device contains two page buffers.
8/ Selected page buffer is currently busy with WSM operation.

FIGURE 3. Truth tables - Continued.

Status register definitions - continued.

		Block status register 1/								
		7	6	5	4		3	2	1	0
		BLOCK STATUS 2/ (BS)	BLOCK LOCK STATUS (BLS)	BLOCK OPERATION STATUS (BOS)	BLOCK OPERATION ABORT STATUS 3/ (BOAS)	MATRIX 5/4	QUEUE STATUS (QS)	V_{PP} STATUS (V_{PPS})	V_{PP} LEVEL 4/ (V_{PPL})	R
1 =	0 0 = 4/	Ready	Block unlocked for write/erase	Operation unsuccessful	Operation aborted	Operation successful or currently running	Queue full	V_{PP} error detect; operation abort	V_{PP} detected at 5.0 V ± 10%	5/
	0 1 = 4/					Not a valid combination				
0 =	1 0 = 4/	Busy	Block locked for write/erase	Operation successful or currently running	Operation not aborted	Operation unsuccessful	Queue available	V_{PP} okay	V_{PP} detected at 12.0 V ± 5%	5/
	1 1 = 4/					Operation aborted 6/				

1/ When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.
2/ RY/BY# output or the BS bit must be checked to determine completion of an operation (block lock, suspend, erase or data write) before the appropriate status bit (BOS or BLS)is checked for success.
3/ The BOAS bit will not be set until BSR.7 = 1.
4/ The BSR.1 is not guaranteed to report accurate feedback between the V_{PPH1} and V_{PPH2} voltage ranges. Writes and erases with V_{PP} between V_{PPLK} (max.) and V_{PPH1} (min.), between V_{PPH1} (max.) and V_{PPH2} (min.), and above V_{PPH2} (max.) produce spurious results and should not be attempted.
5/ These bits are reserved for future use; mask them out when polling the BSR's.
6/ Operation halted via abort command.

Device configuration code

	7	6	5	4	3	2	1	0
	R	R	R	R	R	RY/BY# CONFIGURATION	RY/BY# CONFIGURATION	RY/BY# CONFIGURATION
0 0 1 =	1/	1/	1/	1/	1/	Level mode (default)	Level mode (default)	Level mode (default)
0 1 0 =						Pulse-on-write	Pulse-on-write	Pulse-on-write
0 1 1 =						Pulse-on-erase	Pulse-on-erase	Pulse-on-erase
1 0 0 =						RY/BY# disabled	RY/BY# disabled	RY/BY# disabled
1 0 1 =						Pulse-on-write/erase	Pulse-on-write/erase	Pulse-on-write/erase

1/ These bits are reserved for future use; mask them out when reading the device configuration code. Set these bits to "0" when writing the desired RY/BY# configuration to the device.

FIGURE 3. Truth tables - Continued.

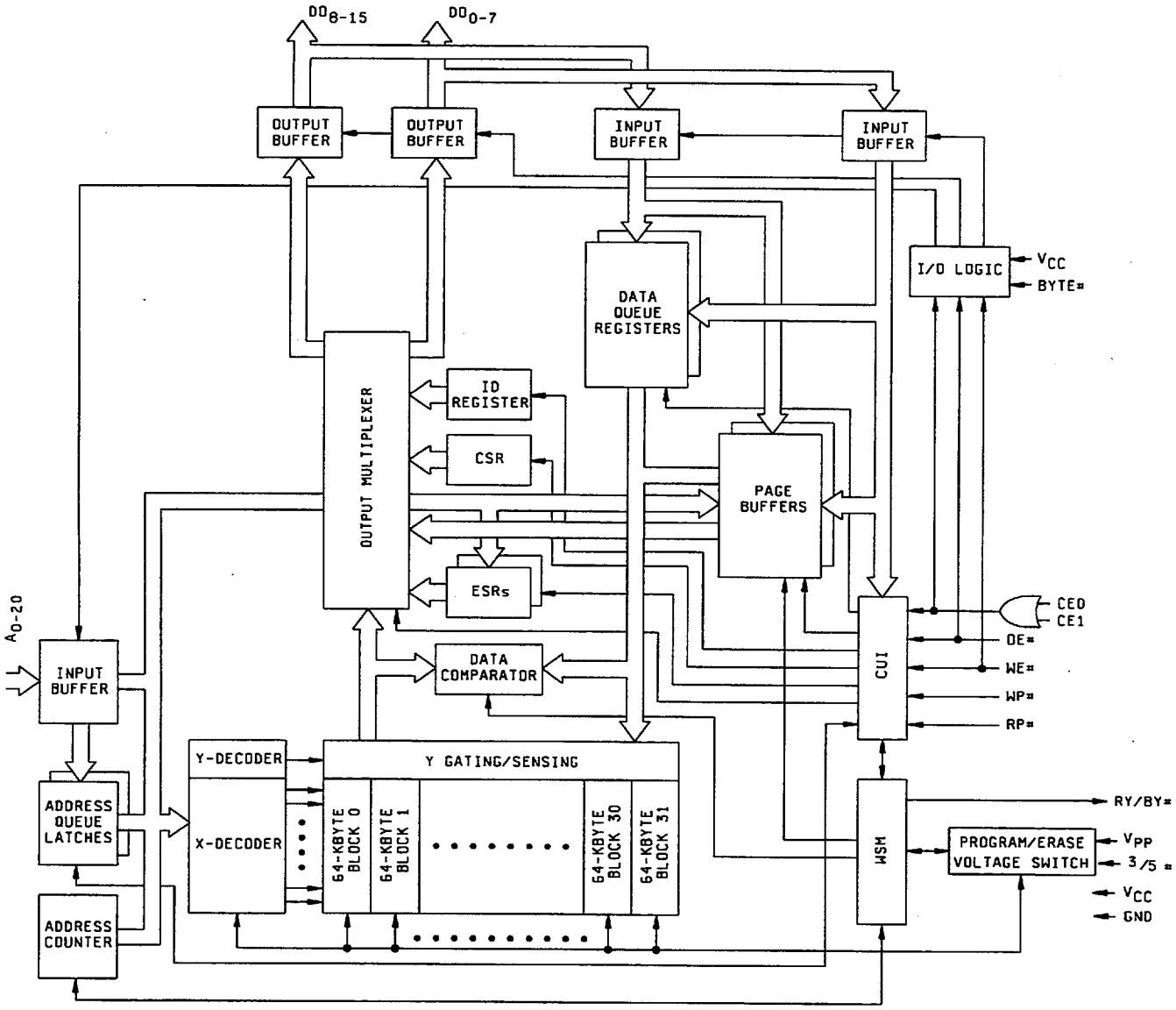
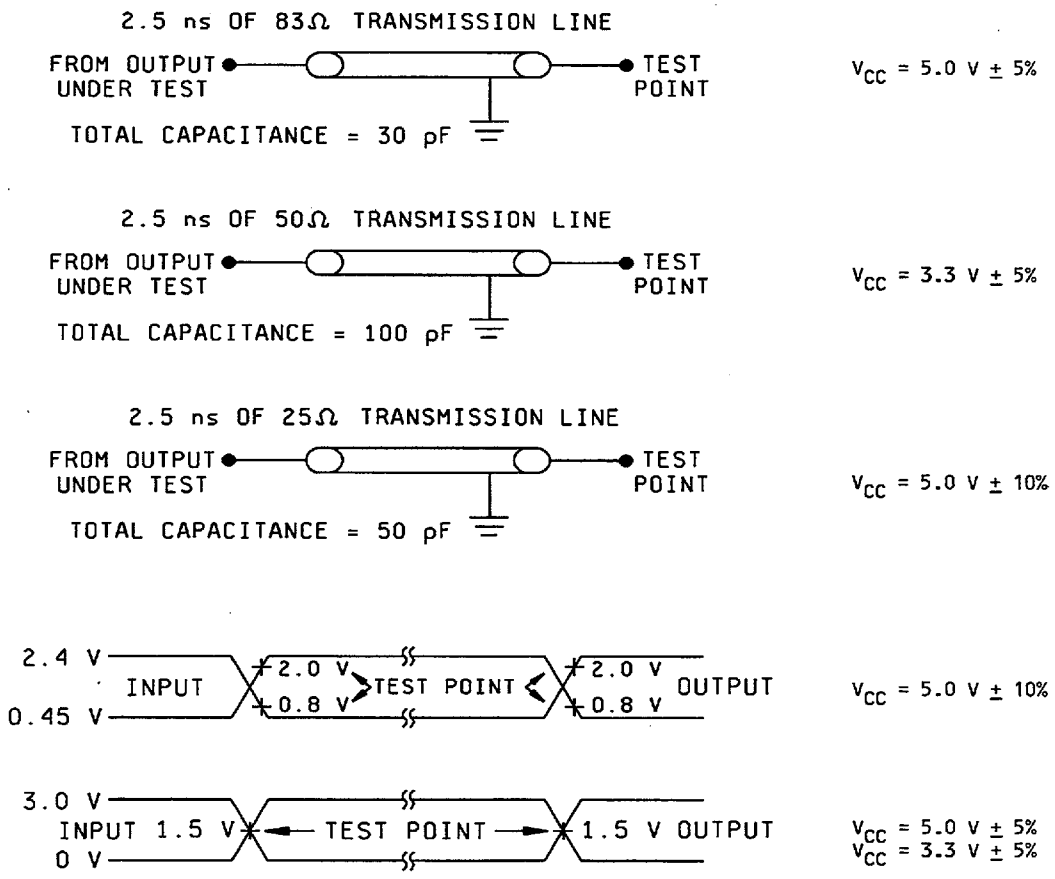


FIGURE 4. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-95625
		REVISION LEVEL	SHEET 22

9004708 0016250 240

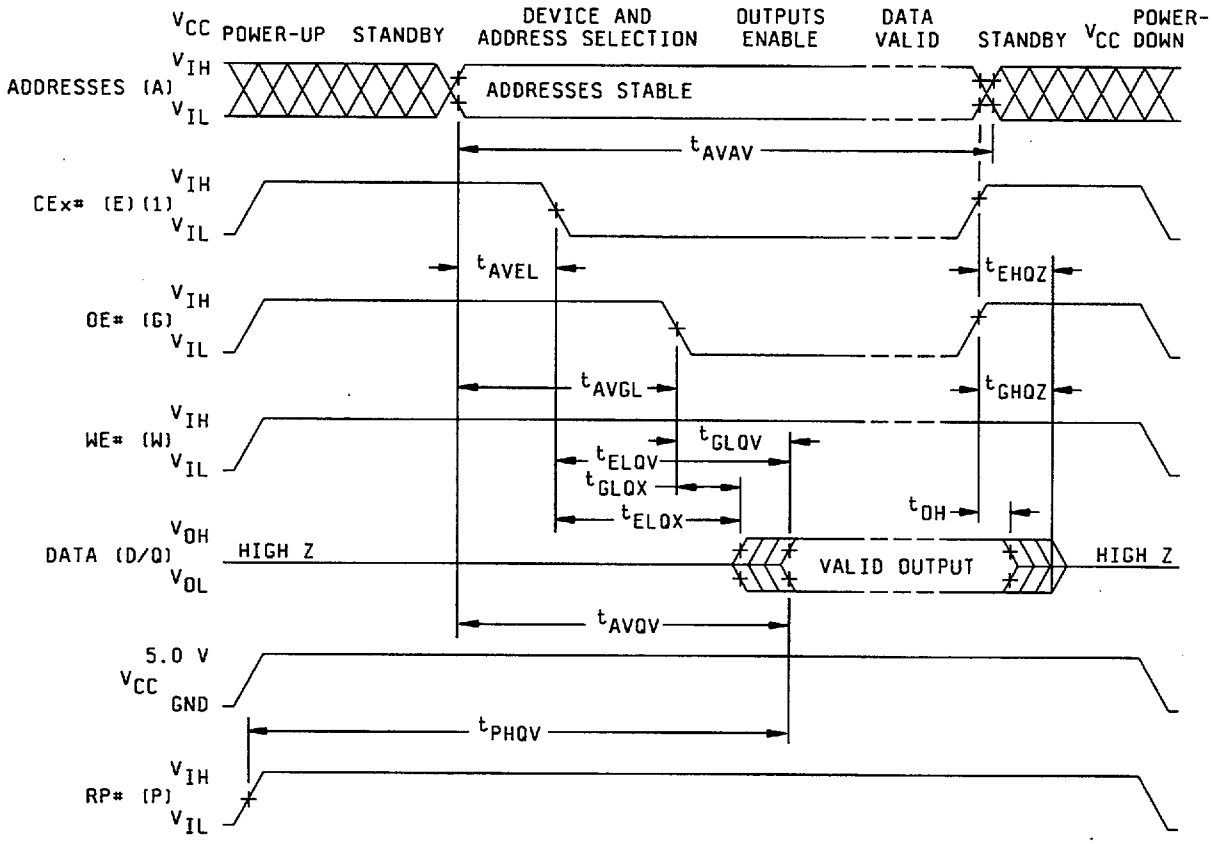


NOTES: AC testing (V_{CC} = 5.0 V ± 10%): Inputs are driven at V_{OH} (2.4 VTTL) for a logic "1" and (0.45 VTTL) for a logic "0". Input timing begins at V_{IH} (2.0 VTTL) and V_{IL} (0.8 VTTL). Output timing ends at VIH and VIL. Input rise and fall times (10% to 90%) < 10 ns.

AC testing (V_{CC} = 5.0 V ± 5% and 3.3 V ± 5%): Inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0". Input timing begins, and output timing ends, at 1.5 volts. Input rise and fall times (10% to 90%) < 10 ns.

FIGURE 5. Switching test circuit and waveforms.

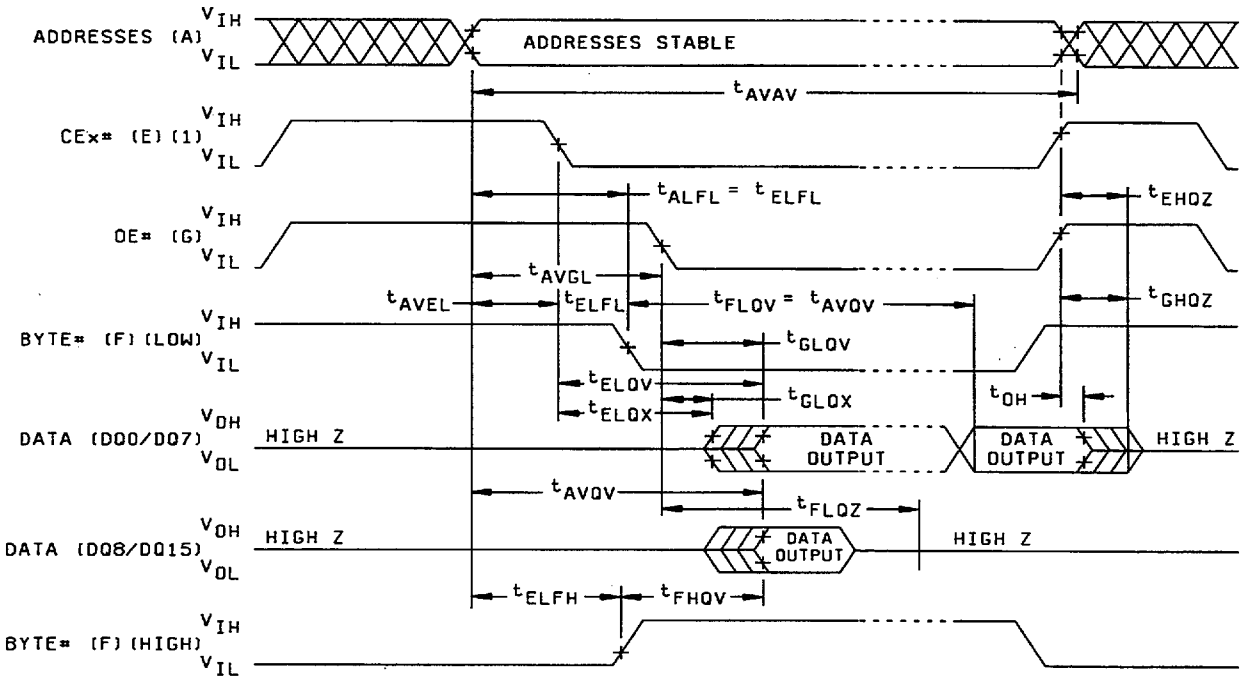
Read cycle timing waveform



NOTE: See note 4 on sheet 27.

FIGURE 5. Switching test circuit and waveforms - continued.

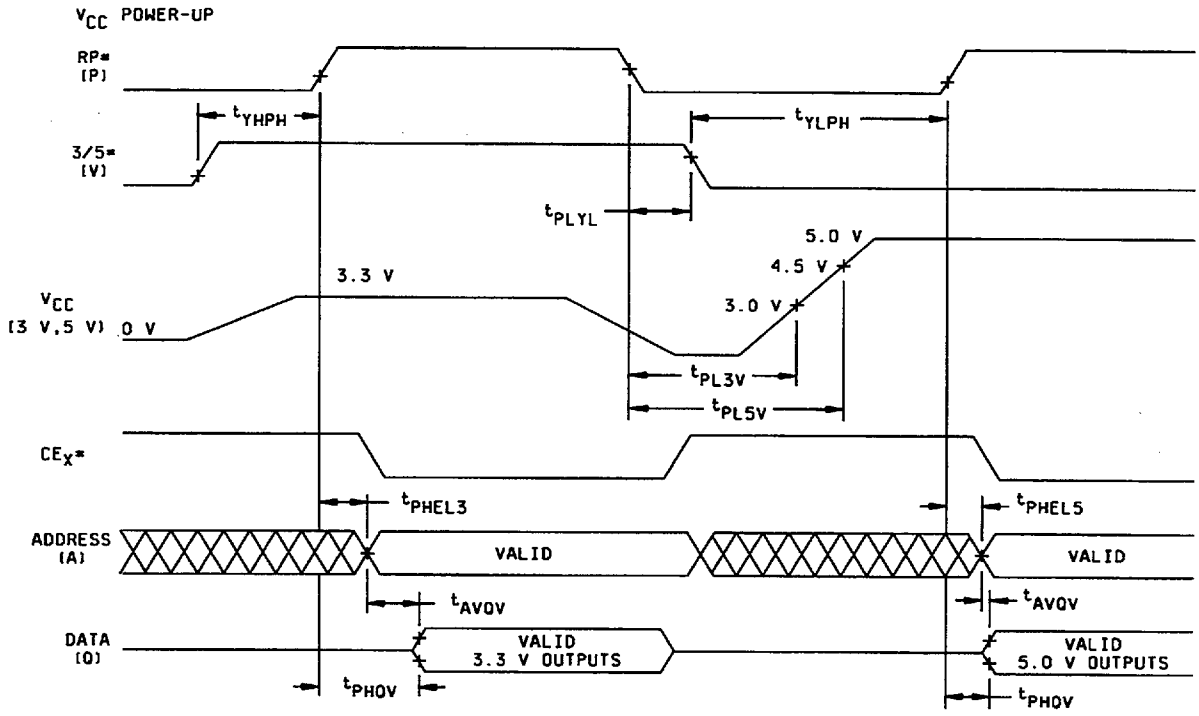
BYTE# timing waveform



NOTE: See note 4 on sheet 27.

FIGURE 5. Switching test circuit and waveforms - cntinued.

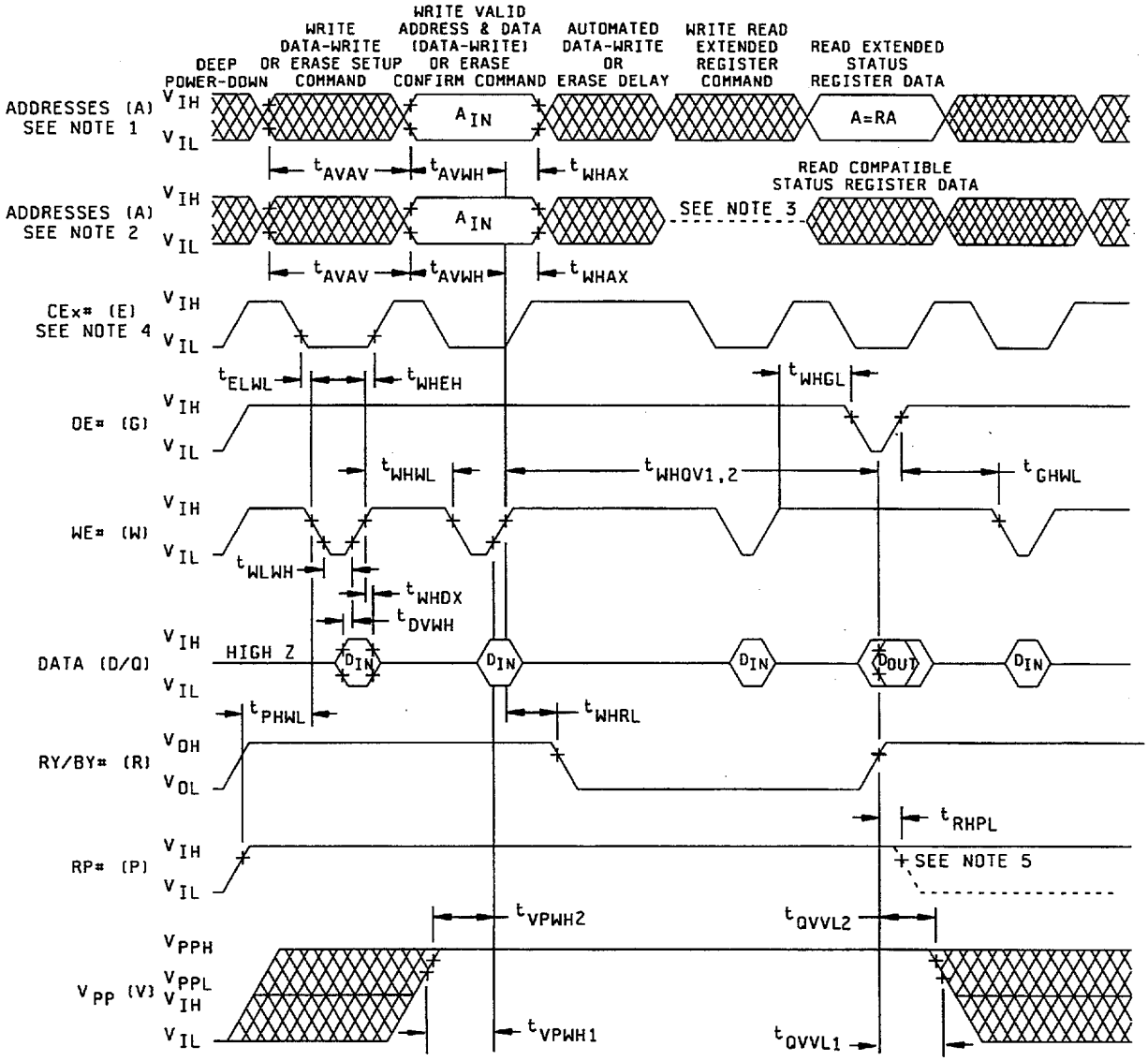
V_{CC} power-up and RP reset waveform



NOTE: CE_0#, CE_1# and OE# are switched low after power-up.

FIGURE 5. Switching test circuit and waveforms - continued.

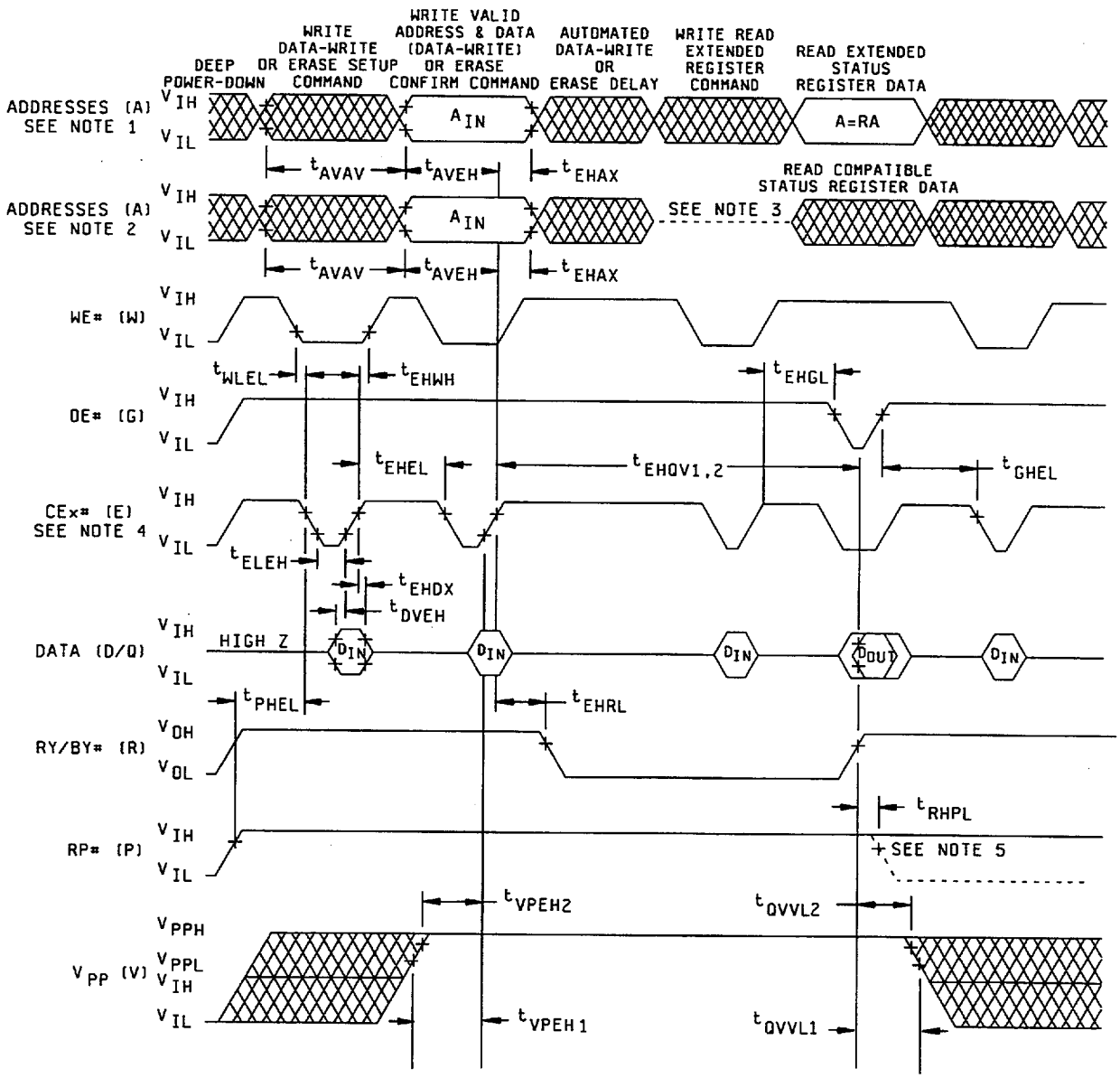
Command write waveform



NOTES:
1. This address string depicts Data-write/erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-write/erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data write/erase operations.
4. CE_x# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
5. RP# low transitiion is only to show t_{RHPL};it is not valid for the read and write cycles shown above.
6. V_{PP} voltage during write/erase operations is valid at both 12.0 volts and 5.0 volts.
7. V_{PP} voltage equal to or below V_{PPLK} provides complete flash memory array protection.

FIGURE 5. Switching test circuit and waveforms - cntinued.

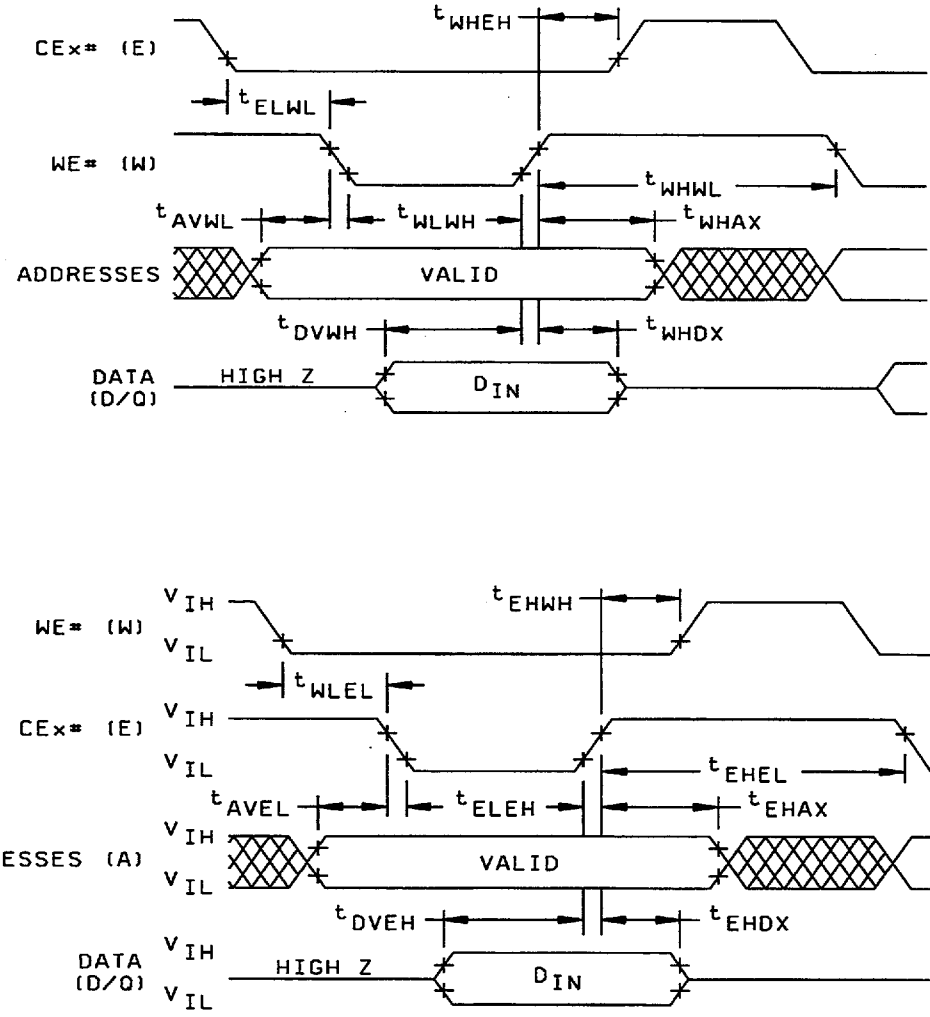
Alternate command write waveform



See notes on sheet 27.

FIGURE 5. Switching test circuit and waveforms - Continued.

WE# and CE# controlled page buffer write timing waveforms respectively



NOTE: See note 4 on sheet 26.

FIGURE 5. Switching test circuit and waveforms - Continued.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes N, Q, and V, performance of O/V (latch-up) testing shall be as specified in the manufacturer's QM plan, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups C and D testing and devices to be archived, i.e., devices not to be sold).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C and shall consist of test specified in table IIB herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The device selected for testing shall be programmed with a checkerboard pattern or equivalent.

(2) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. After the completion of all testing, the devices shall be cleared and verified prior to delivery (except devices submitted for group D testing and devices to be archived, i.e., devices not to be sold).

TABLE IIA. Elecrtical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-I-38535, table III)		
		Device class M	Device class N	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)				1,7,9 or 2,8A,10
2	Static burn-in I method 1015	Not required	Not required	Not required	Not required
3	Same as line 1				1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required
5	Same as line 1				1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,8A,10	2,8A,10	2,8A,10	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,8A,10	2,8A,10	2,8A,10	2,3,7 8A,8B
10	Group E end-point electrical parameters	179	179	179	179

1/ Blank spaces indicate test are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * Indicates PDA applies to subgroups 1 and 7.
5/ ** See 4.4.1c.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device class V, performance of delta tests and limits shall be as specified in the manufacturer's QM plan.
7/ See 4.4.1e.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices to be archived, i.e., devices not to be sold).

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes N, Q, and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE IIB. Delta limits at 25°C.

Test 1/	All device types
I_{CCS} standby	±10 percent of specified value in table I.
I_{LI}	±10 percent of specified value in table I.
I_{LO}	±10 percent of specified value in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine delta.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate figures and tables herein.

4.5.1 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be available upon request.

4.5.2 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes N, Q, and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

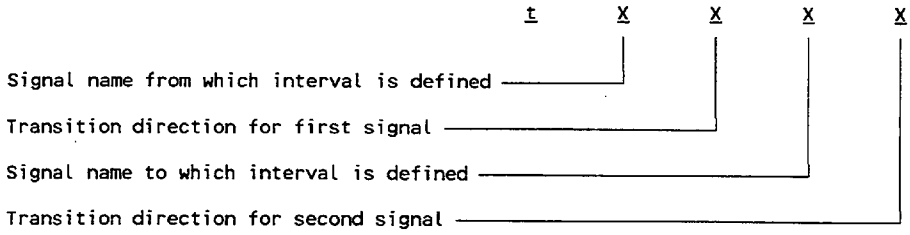
6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535.

C_{IN}, C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
V_H	Output enable and Write enable voltage during chip erase.
O/V	Latchup over-voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:



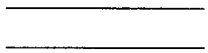
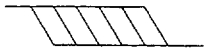
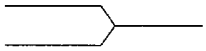
a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
G = Output enable
P = Reset/Deep powerdown

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.3 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WIIL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(N, Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.