REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change in accordance with NOR 5962-R076-96.	96-04-11	Monica L. Poelking
B	Add device type 03. Update boilerplate. Editorial changes throughout.- tvn	98-09-18	Monica L. Poelking

REV																			
SHEET																			
REV	B	B																	
SHEET	15	16																	

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
92-02-12

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, IMAGE RESAMPLING SEQUENCER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-89715**

SHEET 1 OF 16

DSCC FORM 2233
APR 97

5962-E493-98

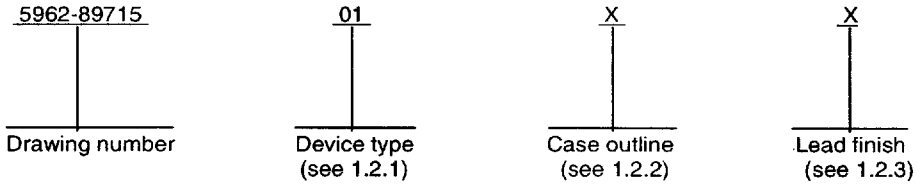
DISTRIBUTION STATEMENT A Approved for public release; distribution is unlimited.

9004708 0038780 173

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	TMC2301	CMOS image resampling sequencer	15 MHz
02	TMC2301	CMOS image resampling sequencer	18 MHz
03	LF2301	CMOS image resampling sequencer	18 MHz

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P68	68	Pin grid array package
Y	CQCC2-J68	68	Square chip carrier with unformed-lead package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7 V dc
DC voltage applied to outputs	-0.5 V to V_{DD} + 0.5 V 2/
Output applied voltage	-0.5 V to V_{DD} + 0.5 V 2/
Output forced current	-6.0 mA to +9.0 mA
Short circuit duration (single output in high state to ground)	1 s
Case operating temperature (T_C)	-60°C to +130°C
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Maximum power dissipation (P_D)	0.50 W
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-PRF-38535

1/ Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is not implied.
2/ Applied voltage must be current limited to specified range.

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Input high voltage (V_{IH})	2.0 V dc minimum
Input low voltage (V_{IL})	0.8 V maximum
Output high current (I_{OH})	-4.0 mA maximum
Output low current (I_{OL})	6.0 mA maximum
Case operating temperature range (T_C)	-55°C to +125°C
Clock pulse width low (t_{PWL}):	
Device type 01	25 ns minimum
Device types 02 and 03	22 ns minimum
Clock pulse width high (t_{PWH}):	
Device type 01	33 ns minimum
Device types 02 and 03	28 ns minimum
Input setup time (t_S):	
Device type 01	20 ns minimum
Device types 02 and 03	18 ns minimum
Input hold time (t_H)	2 ns minimum
Input hold time, INTER	10 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4. Image resampling geometry showing image rotation and expansion. Image resampling geometry showing image rotation and expansion shall be as specified on figure 3.

3.2.5 Waveforms and test circuit. The waveforms and test circuit are as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 tests shall consist of verifying the function of the device. These tests form a part of the vendor's test tape and shall be maintained and available for review from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = -4 mA V_{IN} = 2.0 V or 0.8 V	All	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 6 mA V_{IN} = 2.0 V or 0.8 V	All	1, 2, 3		0.4	V
High level input current	I_{IH}	V_{DD} = 5.5 V V_{IN} = V_{DD}	All	1, 2, 3	-10	+10	µA
Low level input current	I_{IL}	V_{DD} = 5.5 V V_{IN} = 0.0 V	All	1, 2, 3	-10	+10	µA
Supply current	I_{DD}	V_{DD} = 5.5 V f_{IN} = 15 MHz	All	1, 2, 3		75	mA
Quiescent supply current	I_{DDQ}	V_{DD} = 5.5 V, V_{IN} = 0.0 V	01, 02	1, 2, 3		10	mA
			03			5	
Short circuit output current 1/	I_{OS}	V_{DD} = 5.5 V V_{OUT} = 0.0 V	01, 02	1, 2, 3	0	-100	mA
			03		0	-250 2/	
High output leakage current	I_{OZH}	V_{DD} = 5.5 V, V_{IN} = V_{DD}	All	1, 2, 3	-40	+40	µA
Low output leakage current	I_{OZL}	V_{DD} = 5.5 V, V_{IN} = 0.0 V	All	1, 2, 3	-40	+40	µA
Input capacitance	C_{IN}	See 4.3.1c f_{IN} = 1 MHz	All	4		10	pF
Output capacitance	C_{OUT}	See 4.3.1c f_{IN} = 1 MHz	All	4		10	pF
Functional test 3/		V_{DD} = 4.5 V and 5.5 V See 4.3.1d	All	7, 8			
Cycle time	t_{CY}	V_{DD} = 4.5 V	01	9, 10, 11	66		ns
			02, 03	10	55		
Output delay 3/	t_D	V_{DD} = 4.5 V, C_L = 20 pF See figure 4	01, 02	9, 10, 11		35	ns
			03			25	
Output delay, END	$t_{D(E)}$	V_{DD} = 4.5 V, C_L = 20 pF See figure 4	01, 02	9, 10, 11		45	ns
			03			37	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output hold time	t_{HO}	V_{DD} = 4.5 V, C_L = 20 pF See figure 4	01, 02	9, 10, 11	5		ns
			03		2		
Output hold time, END	$t_{HO(E)}$	V_{DD} = 4.5 V, C_L = 20 pF See figure 4	01, 02	9, 10, 11	10		ns
			03		2		
Three-state output enable delay 2/ 3/	t_{ENA}	V_{DD} = 4.5 V, C_L = 40 pF See figure 4	01, 02	9, 10, 11		35	ns
			03			27	
Three-state output disable delay 2/ 3/	t_{DIS}	V_{DD} = 4.5 V, C_L = 40 pF See figure 4	01, 02	9, 10, 11		35	ns
			03			18	

1/ One output to ground, 1 second duration maximum, output high.
2/ Guaranteed, if not tested, to the specified limits.
3/ All transitions are measured at 1.5 V level. Inputs are driven at V_{IL} = 0.4 V and V_{IH} = 2.4 V during functional testing.

Case X							
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
A2	$\overline{WEN}$	B9	P4	F10	GND	K4	$\overline{CZERO}$
A3	B3	B10	P6	F11	X9	K5	CA1
A4	B1	B11	P7	G1	U5	K6	GND
A5	LDR	C1	END	G2	U4	K7	CA3
A6	V_{DD}	C2	INTER	G10	X7	K8	CA5
A7	CLK	C10	P9	G11	X8	K9	CA7
A8	P1	C11	P8	H1	U7	K10	X1
A9	P3	D1	U0	H2	U6	K11	X2
A10	P5	D2	DONE	H10	X5	L2	U11
B1	$\overline{OETA}$	D10	P11	H11	X6	L3	$\overline{ACC}$
B2	INIT	D11	P10	J1	U9	L4	CA0
B3	B2	E1	U2	J2	U8	L5	V_{DD}
B4	B0	E2	U1	J10	X3	L6	CA2
B5	$\overline{NOOP}$	E10	X10	J11	X4	L7	CA4
B6	GND	E11	X11	K1	GND	L8	CA6
B7	P0	F1	U3	K2	U10	L9	X0
B8	P2	F2	GND	K3	$\overline{UWRI}$	L10	GND

FIGURE 1. Terminal connections.

Case Y							
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	GND	18	GND	35	GND	52	GND
2	CA2	19	X9	36	V_{DD}	53	U3
3	CA3	20	X10	37	$\overline{NOOP}$	54	U4
4	CA4	21	X11	38	LDR	55	U5
5	CA5	22	P11	39	B0	56	U6
6	CA6	23	P10	40	B1	57	U7
7	CA7	24	P9	41	B2	58	U8
8	X0	25	P8	42	B3	59	U9
9	GND	26	P7	43	$\overline{WEN}$	60	GND
10	X1	27	P6	44	INIT	61	U10
11	X2	28	P5	45	$\overline{OETA}$	62	U11
12	X3	29	P4	46	INTER	63	$\overline{UWRI}$
13	X4	30	P3	47	END	64	$\overline{ACC}$
14	X5	31	P2	48	DONE	65	$\overline{CZERO}$
15	X6	32	P1	49	U0	66	CA0
16	X7	33	P0	50	U1	67	CA1
17	X8	34	CLK	51	U2	68	V_{DD}

FIGURE 1. Terminal connections - Continued.

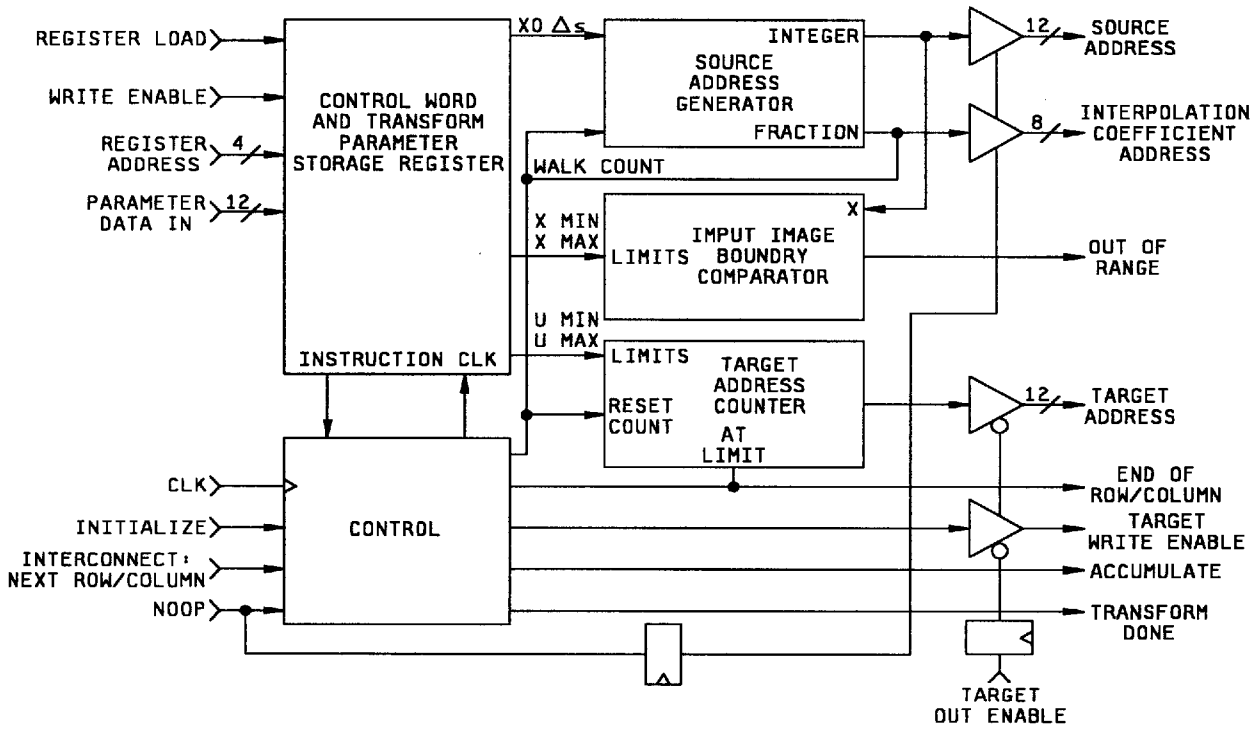
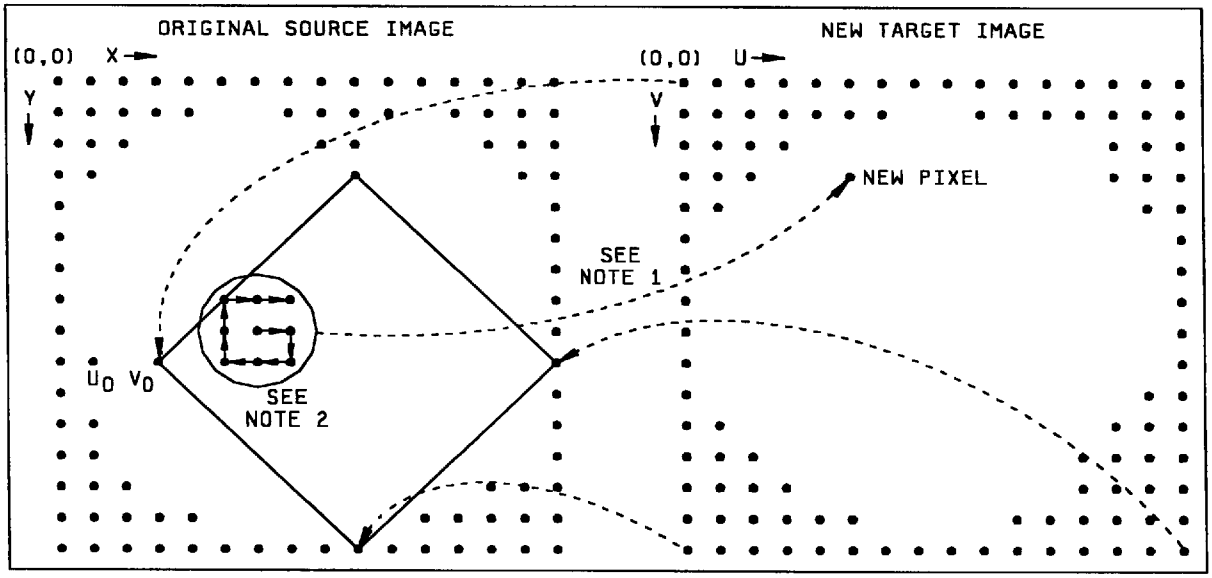
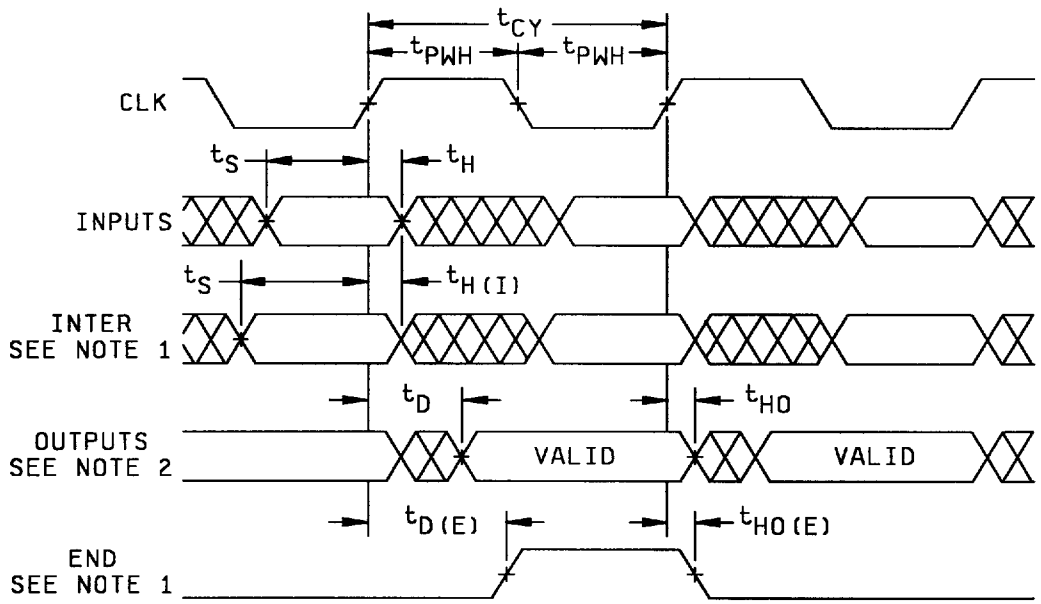


FIGURE 2. Block diagram.



NOTES:
1. Coordinate transformation U, V pixel mapped into X, Y coordinates.
2. Pixel interpolation walk new U, V pixel intensity calculated from surrounding X, Y pixel neighborhood.

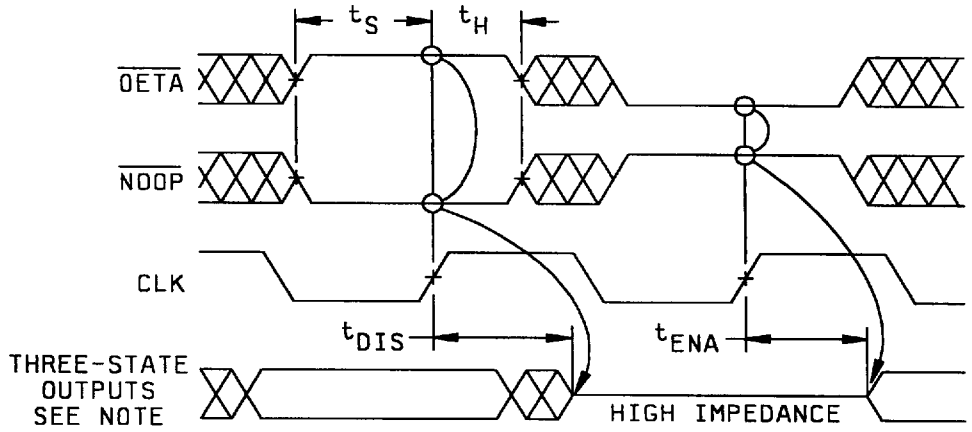
FIGURE 3. Image resampling geometry showing image rotation and expansion.



NOTES:
1. t_S and $t_{D(E)}$ are guaranteed to allow full speed operation in the standard two-device architecture.
2. All outputs except END.

FIGURE 4. Waveforms and test circuit.

Transition level for three-state measurement



NOTE: All outputs except $\overline{\text{CZERO}}$, $\overline{\text{ACC}}$, END, and DONE.

FIGURE 4. Waveforms and test circuit - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 7, 9

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Pin descriptions. The pin descriptions are shown in table III herein.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin descriptions.

Pin name	Pin description
V_{DD}, GND	The device operates from a single +5 V supply. All pins must be connected.
CLK	The device has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.
P11-P0	The coordinate transformation parameters are loaded through the registered 12-bit P input port. P11 is the most significant bit.
B3-B0	The write addresses for the individual coordinate transform parameters are presented at the registered 4-bit B input port. B3 is the most significant bit.
X11-X0	The current X (or Y) source pixel address of the image being resampled is indicated by the registered 12-bit X11-X0 output bus. This output is forced to the high impedance state when $\overline{\text{NOOP}}$ is low. X11 is the most significant bit.
CA7-CA0	The current interpolation kernel coefficient lookup table address is indicated by the registered 8-bit CA7-CA0 output bus. This output is forced to the high impedance state when $\overline{\text{NOOP}}$ is low. CA7 is the most significant bit.
$\overline{\text{WEN}}$	The registered write enable input allows the transformation parameters to be written into the preload register indicated by the address at the B input port when low.
LDR	The data held in all transformation parameter preload registers is latched into the storage registers when the registered input LDR is high. When LDR is low, the parameters remain unchanged.
$\overline{\text{ACC}}$	The accumulation register of the external multiplier-accumulator is initialized by the registered $\overline{\text{ACC}}$ output. $\overline{\text{ACC}}$ goes low for one cycle at the start of each interpolation "walk", effectively clearing the storage register by loading in only the new first product.
$\overline{\text{UWRI}}$	After the end of each interpolation "walk", the Target Memory (U or V) write enable goes low for one clock cycle. This registered output is forced to the high impedance state when $\overline{\text{OETA}}$ is high.
U11-U0	The U (or V) target address of the image being generated is indicated by the registered 12-bit U11-U0 output bus. This output is forced to the high impedance state when $\overline{\text{OETA}}$ is high. U11 is the most significant bit.
INIT	The control logic is cleared and initialized for the start of a new image transformation when the registered INIT input is high for a minimum of two clock cycles. Normal operation begins after INIT goes low.
$\overline{\text{NOOP}}$	The clock is overridden when the registered input $\overline{\text{NOOP}}$ is low, holding all address generators in their current state. Also, the output buffers for the address busses X11-X0 and CA7-CA0 are forced to the high impedance state. This allows the user access to all external memory. When $\overline{\text{NOOP}}$ goes high, normal operation resumes on the next clock cycle.
END	The registered END flag goes high during the last pixel of the last walk in a row in the case of the row chip, and the last pixel of the last walk in a column in the column chip, in the two-device architecture. This output is used as the end-of-line and end-of-frame indicator in conjunction with the INTER inputs of the device.

TABLE III. Pin descriptions - Continued.

Pin name	Pin description
DONE	In the standard two-device system, a row sequencer DONE flag high after the last walk at the end of the last row of an image (during $\overline{\text{UWRI}}$ low) indicates the end of the transform. This registered output is usually ignored on the column device. See the control parameter AUTOINIT.
INTER	In the common two-device system configuration, the interconnect inputs are connected to the END flag outputs. The END flag from the row (X) sequencer thus indicates an "end of line" to the column (Y) device, while the column sequencer in turn sends a "bottom of frame" signal to the row device, forcing a reset of the address counter.
$\overline{\text{OETA}}$	The target memory outputs $\overline{\text{UWRI}}$ and address bus U11-U0 are in the high-impedance state when the registered output enable input is high. When $\overline{\text{OETA}}$ is low, they are enabled on the next clock cycle.
$\overline{\text{CZERO}}$	The registered $\overline{\text{CZERO}}$ flag indicates whether the current X (or Y) source address is outside the image space as defined by XMIN or XMAX (or YMIN and YMAX). In the most common case, (see the XMIN, XMAX definitions) $\overline{\text{CZERO}}$ goes low if the source address is out-of-bounds. This signal may be used to force a zero on the coefficient input to the external multiplier-accumulator. In the standard two-device IRS system, the $\overline{\text{CZERO}}$ flags are ANDed together for the above case.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-09-18

Approved sources of supply for SMD 5962-89715 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8971501XX	3/	
5962-8971502XX	3/	
5962-8971501YX	3/	
5962-8971502YX	3/	
5962-8971503XA	65896	LF2301GMB55
5962-8971503XC	65896	LF2301GMB55

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65896	Logic Devices, Inc. 1320 Orleans Drive Sunnyvale, CA 94089

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.