PRELIMINARY

Pentium® OverDrive® PROCESSOR WITH MMX™ TECHNOLOGY FOR Pentium PROCESSOR-BASED SYSTEMS

200-MHz Pentium® OverDrive® Processor with MMX™ Technology to upgrade 100/133/166-MHz Pentium Processor-Based Systems

180-MHz Pentium OverDrive Processor with MMX Technology to upgrade 90/120/150-MHz Pentium Processor-Based Systems and upgrades 75-MHz Pentium Processor-Based Systems to 150-MHz

166-MHz Pentium OverDrive Processor with MMX Technology to upgrade 100/133-MHz Pentium Processor-Based Systems

- **Support for MMX™ Technology**
- **Powerful Processor Upgrades for Upgradable Pentium® Processor-Based Systems**
- **Superscalar Architecture**
  - **Enhanced pipelines**
  - **Two Pipelined Integer Units Capable of 2 Instructions/Clock**
  - **Pipelined MMX Unit**
  - **Pipelined Floating-Point Unit**
- **Separate Code and Data Caches**
  - **Deeper Write Buffers, "Pool" Configuration**
  - **Enhanced Branch Prediction**
  - **Virtual Mode Extensions**
- **32-Bit CPU with 64-Bit Data Bus**
- **.35μM CMOS Silicon Technology**
- **On-package Voltage Regulation and Voltage Filtering**
- **Integrated Fan/Heatsink Thermal Solution**
- **Compatible with Installed Software Base**
  - **MS-DOS*, Windows*, Windows 95, Windows NT, OS/2*, UNIX***
- **Product Line Supports Socket 5 & Socket 7 Designs**
- **320 pin SPGA Package**
- **Bus/Core Ratio, Hard-Bonded in 2/5 and 1/3 Modes**
- **Easy Installation**
- **Supports 50, 60, 66-MHz Bus Speeds**
- **Single 3.3 Volt Supply**

June 1997 Order Number: 290607-001

The Pentium® OverDrive® processor with MMX™ technology is an end-user, single chip, Pentium processor upgrade product. The end user is able to add support for Intel's new MMX technology and increase the performance of their PC by simply replacing the existing 75, 90, 100, 120, 133, 150, and 166-MHz Pentium processor with a Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology provides the performance needed for today's mainstream desktop applications and workstations. The Pentium OverDrive processor with MMX technology is binary compatible with the Pentium processor and compatible with the entire installed base of applications for MS-DOS*, Windows*, Windows 95, Windows NT, OS/2*, and UNIX*.

The 200-MHz Pentium OverDrive processor with MMX technology is designed to upgrade 100, 133, and 166-MHz Pentium processor-based systems. All most all of these systems use ZIF sockets that allow easy end user installation of the processor upgrade.

The 180/150-MHz Pentium OverDrive processor with MMX technology is designed to upgrade 75, 90, 120, and 150-MHz Pentium processor-based systems.

The 166-MHz Pentium OverDrive processor with MMX technology is designed to upgrade 100 and 133-MHz Pentium processor-based systems.

The Pentium OverDrive processor with MMX technology for Pentium processor-based systems has 4.5 million transistors and is built on Intel's advanced 0.35-micron silicon technology. The Pentium OverDrive processor with MMX technology is equipped with high reliability, integrated fan/heatsinks.

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The Pentium OverDrive processor with MMX technology may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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1.0. INTRODUCTION

This datasheet describes Intel's Pentium OverDrive processor with MMX technology for upgradable Pentium processor-based systems. The Pentium OverDrive processor with MMX technology currently includes upgrades for 75, 90, 100, 120, 133, 150, and 166-MHz Pentium processors. Technical descriptions of other Pentium OverDrive processors are available in *Intel OverDrive® Processors* datasheet (Order #290436).

This datasheet is intended to be used in conjunction with the *Pentium® Family User's Manual* (Order #241428), which describes the Pentium family architecture and functionality. All enhancements or differences between the Pentium OverDrive processor with MMX technology and the original Pentium processor (i.e., 75/90/100/120/133/150/166-MHz Pentium processor vs. 200/180/166-MHz Pentium OverDrive processor with MMX technology) are described in this datasheet. Pentium processor-based systems that are compatible with the Pentium OverDrive processor with MMX technology must be designed to both the original processor specifications and the Pentium OverDrive processor with MMX technology specifications.

1.1. Product Overview

The Pentium OverDrive processor with MMX technology, for upgradable 75, 90, 100, 120, 150, and 166-MHz Pentium systems, allows users to upgrade to more advanced Pentium processor technology and adds Intel's new MMX technology.

Figure 1 contains the block diagram of the Pentium OverDrive processor with MMX technology. Figure 2 lists some of the enhancements of the Pentium OverDrive processor with MMX technology. Figure 3 describes the upgrade choices available for an existing Pentium processor system.

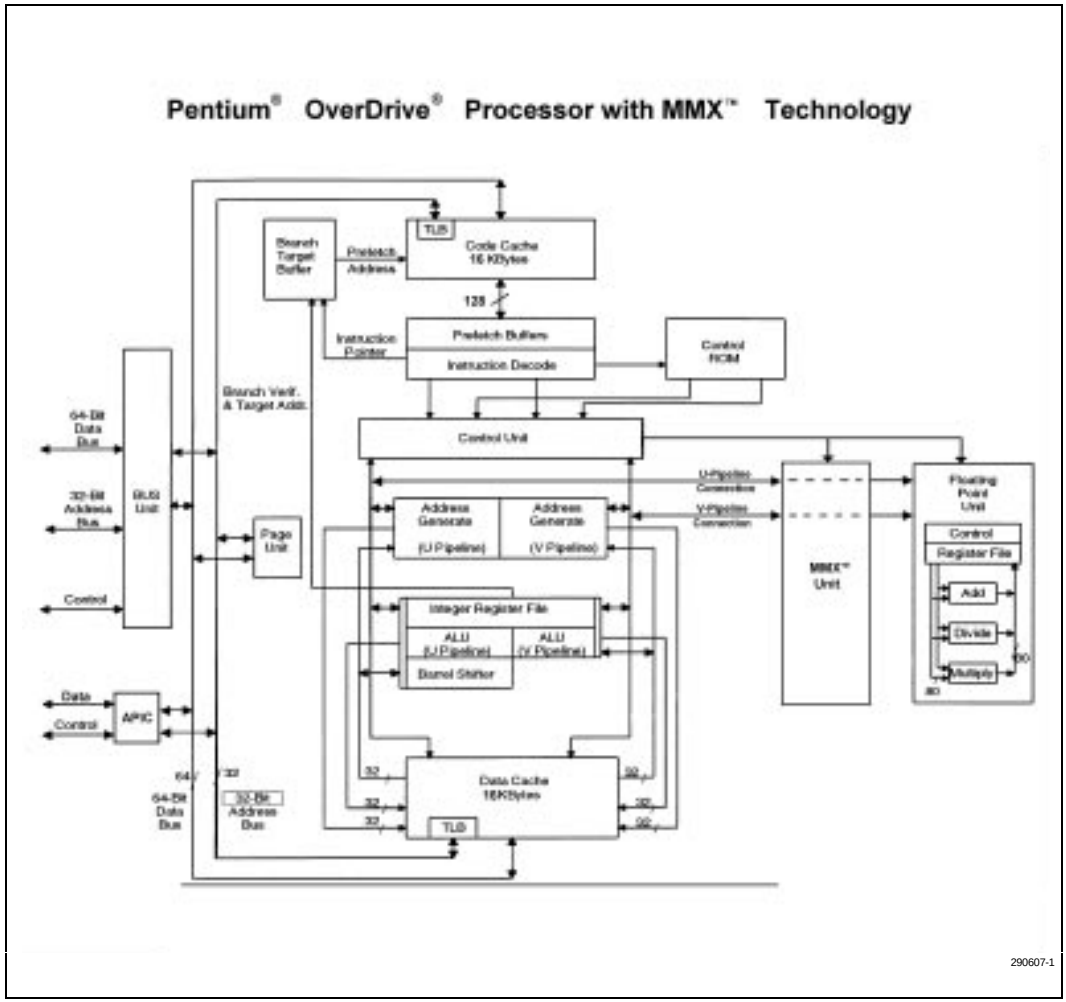

Figure 1. Pentium® OverDrive® Processor with MMX™ Technology Block Diagram

- Based on Advanced Pentium® Processor with MMX™ Technology
- Superscalar Architecture
- Pipelined Floating-Point Unit
- Separate 16K Code and 16K Data caches
- 64 Bit Data Bus
- Address Parity
- Virtual Mode Extensions
- System Management Mode
- Fractional Bus Operation

200, 180, and 166-MHz Pentium OverDrive® Processors with MMX Technology

- .35µM CMOS Silicon Technology
- Dynamic Branch prediction
- Improved Execution Time
- Writeback MESI Protocol in the Data Cache
- Bus Cycle Pipelining
- Internal Parity Checking
- Performance Monitoring
- Execution Tracing
- Active Fan/Heatsink

- For 75, 90, and 100-MHz Pentium Processor-Based Systems

- 320 Pin SPGA Pinout
- On-package Voltage Regulation

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Figure 2. Pentium® OverDrive® Processor with MMX™ Technology Key Features

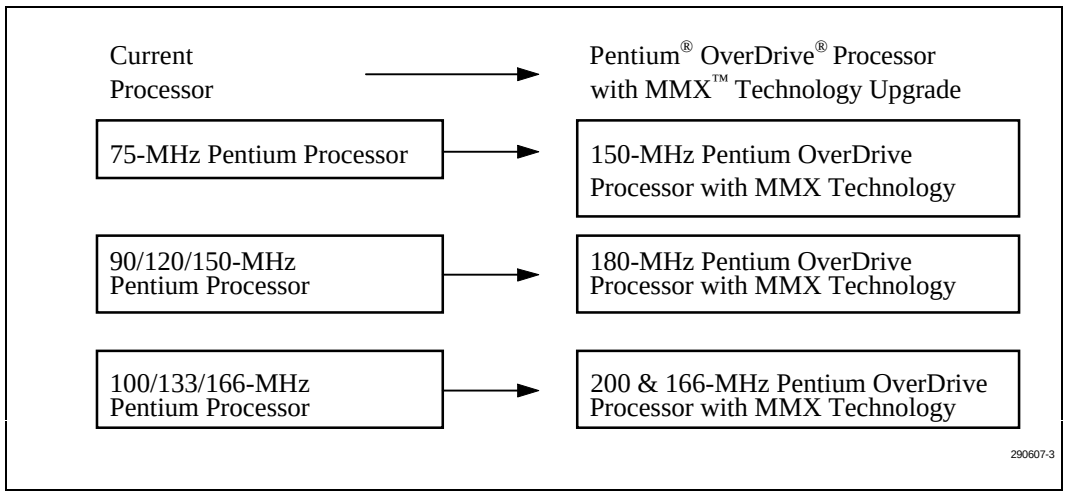


Figure 3. Pentium® OverDrive® Processor with MMX™ Technology Upgrade Choices

1.2. Product Description

The Pentium OverDrive processor with MMX technology comes in a 320-pin SPGA package and is a drop-in replacement for the 75, 90, 100, 120, 133, 150 and 166-MHz Pentium processor. It comes with on-package voltage regulation to provide the required 2.8 volts for the core and a fan/heatsink for a complete thermal solution. The internal core operates at 3.0 and 2.5 times the speed of the system bus for respective 200MHz and 166-MHz Pentium OverDrive processor with MMX technology. For dual socket systems the original processor must be removed and the Pentium OverDrive processor with MMX technology should be installed in the secondary socket since it does not support dual processing.

1.3. Purpose of this Document

This document describes the system architecture and physical environment of Pentium OverDrive processor with MMX technology. It also outlines differences between the originally installed Pentium processor and the Pentium OverDrive processor with MMX technology.

1.4. Compatibility Note

In this document some register bits are shown as "Intel Reserved" (RES) and some pins are marked as "No Connects" (NC) or "Reserved" (RES). When reserved bits are called out, treat them as fully undefined. This is essential for software compatibility with current and future processors. When a pin is marked as a "NC" or "RES" it is important to not connect any other signals to such pins to ensure proper operation. Intel strongly recommends following the guidelines below:

1. Do not depend on the states of any undefined bits when testing the values of defined register. Mask them out when testing.
2. Do not depend on the states of any undefined bits when storing them to memory or another register.
3. Do not depend on the ability to retain information written into any undefined bits.
4. When loading registers always load the undefined bits as zeros.
5. Never connect signals to device pins marked "NC" or "RES".
6. **INC** pins are Internal No-Connects. This means that the pin is not connected to the processor internally. For example; the CPUTYP signal pin on the Pentium OverDrive processor with MMX technology is internally not connected to the package pin. The core is internally tied to V_{SS}. The pin on the package is defined as INC. Any external connections to the package pin will not affect the processor core because the core is physically disconnected from the package pin.

2.0. PINOUT AND PIN DESCRIPTION

2.1. Pinout

The Pentium OverDrive processor with MMX technology has a 320-pin SPGA pinout and is designed to be installed into Socket 5 or Socket 7. See Section 6.3 for more details on Socket 5 and Socket 7. Figure 4 and Figure 5 are illustrations of each side of the SPGA package.

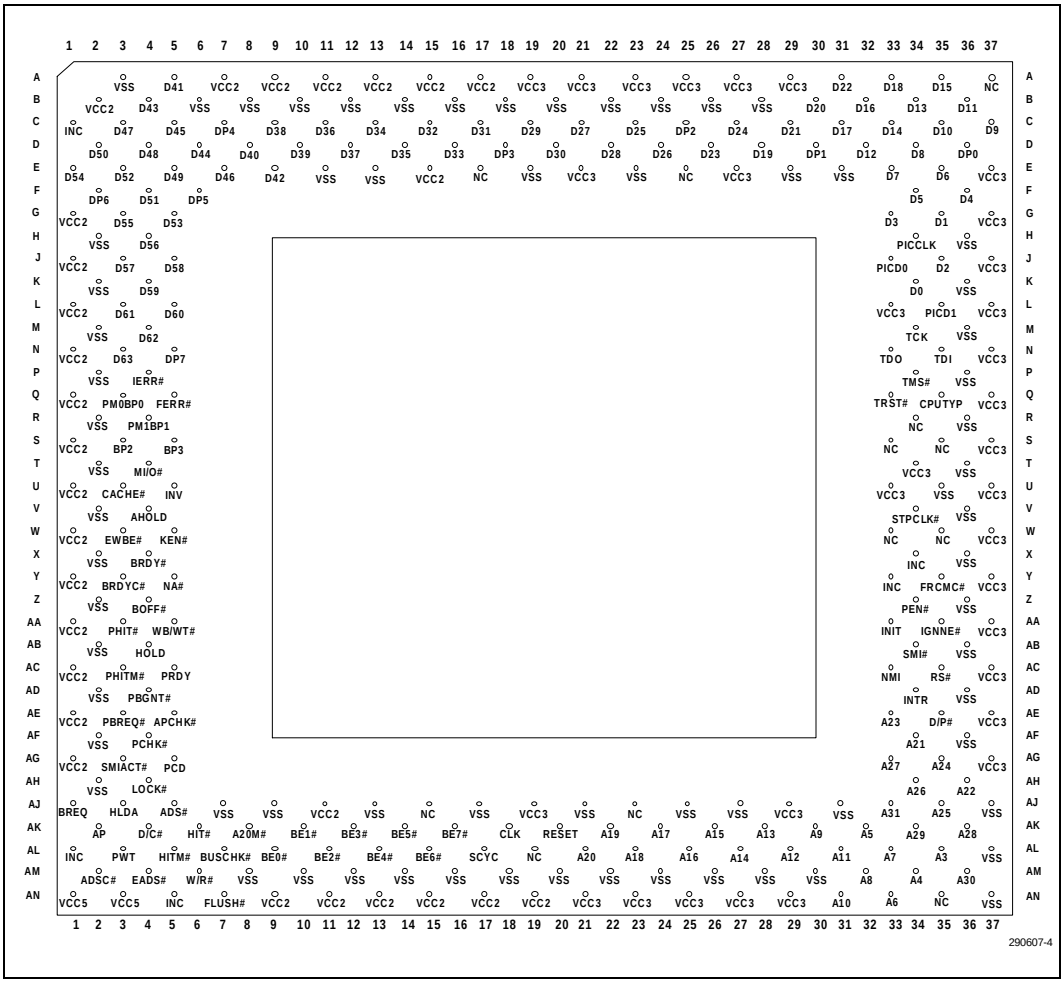


Figure 4. Pentium® OverDrive® Processor with MMX™ Technology Pinout—Top Side View

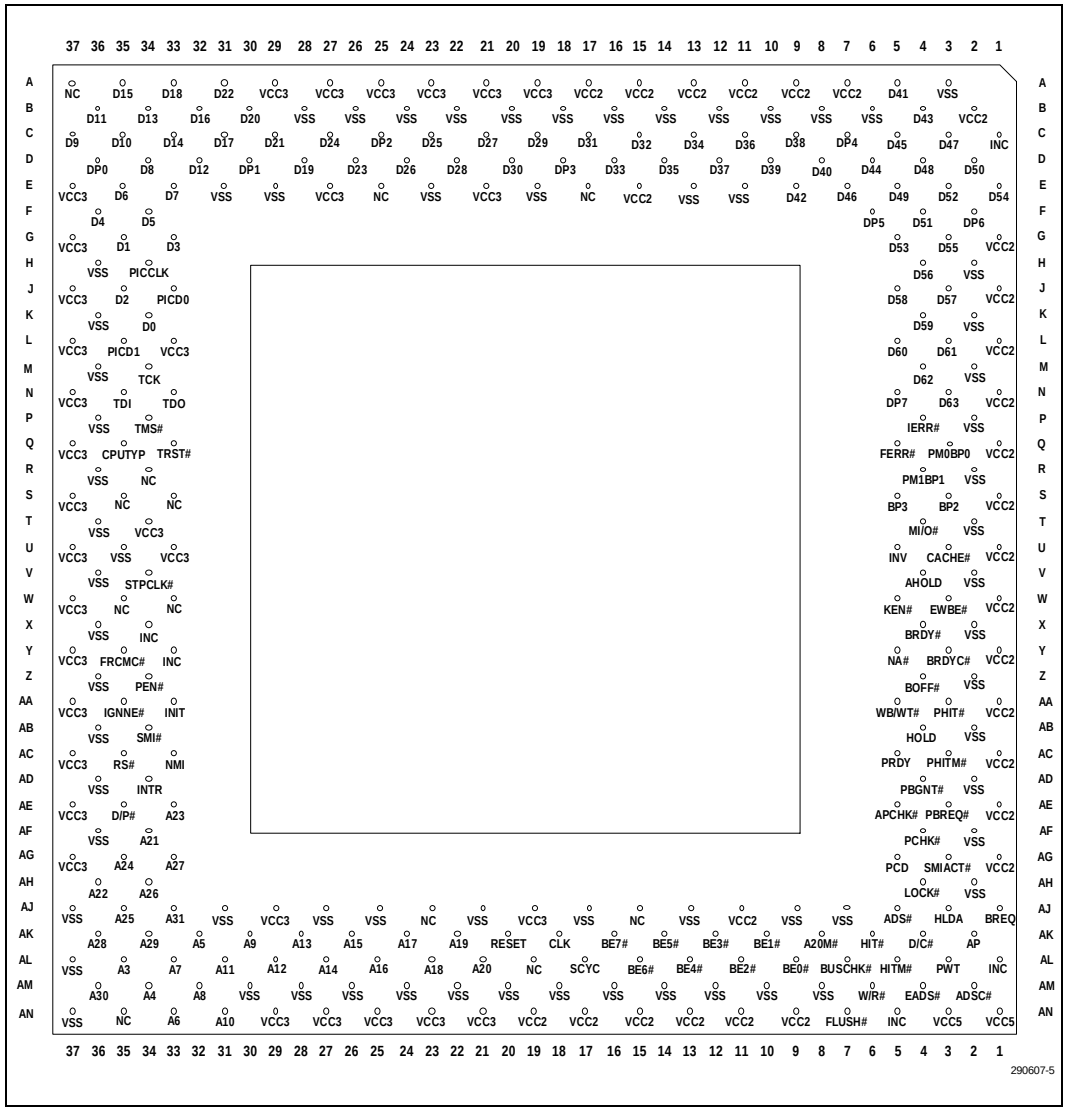


Figure 5. Pentium® OverDrive® Processor with MMX™ Technology Pinout—Pin Side View

2.2. Pin Cross Reference

Table 1. 320-Pin SPGA Pin Cross Reference by Pin Name

Address									
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 1. 320-Pin SPGA Pin Cross Reference by Pin Name (Continued)

Control							
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**	**Signal**	**Location**
A20M#	AK08	BRDYC#	Y03	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BREQ	AJ01	FRCMC#	Y35	PM0/BP0	Q03
ADSC#	AM02	BUSCHK#	AL07	HIT#	AK06	PM1/BP1	R04
AHOLD	V04	CACHE#	U03	HITM#	AL05	PRDY	AC05
AP	AK02	CPUTYP**	Q35	HLDA	AJ03	PWT	AL03
APCHK#	AE05	D/C#	AK04	HOLD	AB04	R/S#	AC35
BE0#	AL09	D/P#*	AE35	IERR#	P04	RESET	AK20
BE1#	AK10	DP0	D36	IGNNE#	AA35	SCYC	AL17
BE2#	AL11	DP1	D30	INIT	AA33	SMI#	AB34
BE3#	AK12	DP2	C25	INTR/LINT0	AD34	SMIACT#	AG03
BE4#	AL13	DP3	D18	INV	U05	TCK	M34
BE5#	AK14	DP4	C07	KEN#	W05	TDI	N35
BE6#	AL15	DP5	F06	LOCK#	AH04	TDO	N33
BE7#	AK16	DP6	F02	M/IO#	T04	TMS	P34
BOFF#	Z04	DP7	N05	NA#	Y05	TRST#	Q33
BP2	S03	EADS#	AM04	NMI/LINT1	AC33	W/R#	AM06
BP3	S05	EWBE#	W03	PCD	AG05	WB/WT#	AA05
BRDY#	X04	FERR#	Q05	PCHK#	AF04		

APIC		Clock Control		Dual Processor Private Interface	
Signal	**Location**	**Signal**	**Location**	**Signal**	**Location**
PICCLK	H34	CLK	AK18	PBGNT#	AD04
PICD0	J33	BF **	Y33	PBREQ#	AE03
[DPEN#]		BF1**	X34	PHIT#	AA03
PICD1 [APICEN]	L35	STPCLK#	V34	PHITM#	AC03

NOTES:

The shaded pin definitions on the Pentium® OverDrive® processor with MMX™ technology are dual processing pins and are not supported by the Pentium OverDrive processor with MMX technology in Table 2.

• The D/P# signal in the 75, 90, 100, 120, 133, 150, and 166-MHz Pentium processor is always driven. Low indicates primary processor has the bus and high indicates the secondary processor is driving the bus. In the Pentium OverDrive processor with MMX technology this pin is defined internal no connect.

** These signals are internally set and are not connected to the Pentium OverDrive processor with MMX technology pins. The pins are defined as Internal No-Connects.

Table 1. 320-Pin SPGA Pin Cross Reference by Pin Name (Continued)

V_{CC}									
A07	A19	B02	G37	N01	T34	Y01	AE01	AJ29	AN19
A09	A21	E15	J01	N37	U01	Y37	AE37	AN09	AN21
A11	A23	E21	J37	Q01	U33	AA01	AG01	AN11	AN23
A13	A25	E27	L01	Q37	U37	AA37	AG37	AN13	AN25
A15	A27	E37	L33	S01	W01	AC01	AJ11	AN15	AN27
A17	A29	G01	L37	S37	W37	AC37	AJ19	AN17	AN29
V_{SS}									
A03	B20	E23	M36	V02	AD02	AJ17	AM10	AM26	
B06	B22	E29	P02	V36	AD36	AJ21	AM12	AM28	
B08	B24	E31	P36	X02	AF02	AJ25	AM14	AM30	
B10	B26	H02	R02	X36	AF36	AJ27	AM16	AN37	
B12	B28	H36	R36	Z02	AH02	AJ31	AM18	AL01	
B14	E11	K02	T02	Z36	AJ07	AJ37	AM20		
B16	E13	K36	T36	AB02	AJ09	AL37	AM22		
B18	E19	M02	U35	AB36	AJ13	AM08	AM24		
NC/INC								**V_{CC5}**	
A37	E25	S33	W33	C01	AJ23	AN35		AN01	
E17	R34	S35	W35	AJ15	AL19	AN05		AN03	

NOTE:

The shaded V_{CC}/V_{SS}/NC pins are new pin definitions (additions) on the Pentium® OverDrive® processor with MMX™ technology with the exception of A03 and B02.

2.3. Quick Pin Reference

Table 2. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, Pentium® OverDrive® processor with MMX™ technology emulates the address wraparound at 1 Mbyte which occurs on the 8086. When A20M# is asserted, the Pentium OverDrive processor with MMX technology masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31-A3	I/O	As outputs, the address lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A3.
ADS#	O	The address status indicates that a new valid bus cycle is currently being driven by the Pentium OverDrive processor with MMX technology.
ADSC#	O	ADSC# is functionally identical to ADS#.
AHOLD	I	In response to the assertion of address hold, Pentium OverDrive processor with MMX technology will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	Address parity is driven by the Pentium OverDrive processor with MMX technology with even parity information on all the Pentium OverDrive processor with MMX technology generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium OverDrive processor with MMX technology during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium OverDrive processor with MMX technology
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium OverDrive processor with MMX technology has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	The APIC is not supported by the Pentium OverDrive processor with MMX technology.
BE7#-BE5# BE4#-BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3).
[BF] [BF1]	I	**Bus Frequency** determines the bus-to-core frequency ratio on the Pentium processor. These are Internal No Connects on the Pentium OverDrive processor with MMX technology which has a preset bus fraction of 5/2 for 166-MHz OverDrive Processor and 3/1 for 200-MHz OverDrive Processor core/bus ratio.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
BOFF#	I	The backoff input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium OverDrive processor with MMX technology will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time Pentium OverDrive processor with MMX technology restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The breakpoint pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the performance monitoring pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The burst ready input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium OverDrive processor with MMX technology data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	This signal has the same functionality as BRDY#.
BREQ	O	The bus request output indicates to the external system that Pentium OverDrive processor with MMX technology has internally generated a bus request. This signal is always driven whether or not the Pentium OverDrive processor with MMX technology is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, Pentium OverDrive processor with MMX technology will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium OverDrive processor with MMX technology will vector to the machine check exception.
CACHE#	O	For Pentium OverDrive processor with MMX technology-initiated cycles the cache pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, Pentium OverDrive processor with MMX technology will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The clock input provides the fundamental timing for Pentium OverDrive processor with MMX technology. The clock frequency is the operating frequency of the Pentium OverDrive processor with MMX technology external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK.
CPUTYP	I	CPUTYP is internally tied to ground and is a Internal No-Connect (INC) to the package pin on the Pentium OverDrive processor with MMX technology.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
D/C#	O	The data/code output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D/P#	O	The Pentium OverDrive processor with MMX technology does not support dual processing.
D63-D0	I/O	These are the 64 data lines for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the data parity pins for the processor. There is one for each byte of the data bus. They are driven by Pentium OverDrive processor with MMX technology with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium OverDrive processor with MMX technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium OverDrive processor with MMX technology. DP7 applies to D63-D56, DP0 applies to D7-D0.
[DPEN#] PICD0	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
EADS#	I	This signal indicates that a valid external address has been driven onto the Pentium OverDrive processor with MMX technology address pins to be used for an inquire cycle.
EWBE#	I	The external write buffer empty input, when inactive (high), indicates that a write cycle is pending in the external system. When Pentium OverDrive processor with MMX technology generates a write, and EWBE# is sampled inactive, the Pentium OverDrive processor with MMX technology will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The floating-point error pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I	When asserted, the cache flush input forces the Pentium OverDrive processor with MMX technology to writeback all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the Pentium OverDrive processor with MMX technology indicating completion of the writeback and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered.
FRCMC#	I	The Pentium OverDrive processor with MMX technology does not support functional redundancy checking.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
HIT#	O	The hit indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either Pentium OverDrive processor with MMX technology data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium OverDrive processor with MMX technology cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The hit to a modified line output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The bus hold acknowledge pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that Pentium OverDrive processor with MMX technology has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and Pentium OverDrive processor with MMX technology will resume driving the bus. If the Pentium OverDrive processor with MMX technology has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the bus hold request, Pentium OverDrive processor with MMX technology will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium OverDrive processor with MMX technology will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium OverDrive processor with MMX technology will recognize HOLD during reset.
IERR#	O	The internal error pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the Pentium OverDrive processor with MMX technology will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the ignore numeric error input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium OverDrive processor with MMX technology will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium OverDrive processor with MMX technology will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium OverDrive processor with MMX technology will stop execution and wait for an external interrupt.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
INIT	I	The Pentium OverDrive processor with MMX technology **initialization** input pin forces the Pentium OverDrive processor with MMX technology to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the Pentium OverDrive processor with MMX technology will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active maskable interrupt input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium OverDrive processor with MMX technology will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The invalidation input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The cache enable pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium OverDrive processor with MMX technology generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The bus lock pin indicates that the current bus cycle is locked. Pentium OverDrive processor with MMX technology will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back to back locked cycles.
M/IO#	O	The memory/input-output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active next address input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium OverDrive processor with MMX technology will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium OverDrive processor with MMX technology supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The non-maskable interrupt request signal indicates that an external non-maskable interrupt has been generated.
PBGNT#	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.

Table 2. Quick Pin Reference

Symbol	Type	Name and Function
PCD	O	The page cache disable pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	The parity check output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The parity enable input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium OverDrive processor with MMX technology will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to “1”, the Pentium OverDrive processor with MMX technology will vector to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
PHITM#	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
PICCLK	I	The Pentium OverDrive processor with MMX technology does not support dual processing.
PICD0-1 [DPEN#] [APICEN]	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
PBREQ#	I/O	The Pentium OverDrive processor with MMX technology does not support dual processing.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The probe ready output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active, or Probe Mode being entered.
PWT	O	The page write through pin reflects the state of the PWT bit in CR3, the Page Directory Entry, or the Page Table Entry. The PWT pin is used to provide an external writeback indication on a page by page basis.
R/S#	I	The run / stop input is an asynchronous, edge sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.

Table 2. Quick Pin Reference

Symbol	Type	Name and Function
RESET	I	**RESET** forces the Pentium OverDrive processor with MMX technology to begin execution at a known state. All Pentium OverDrive processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH#, and INIT are sampled when RESET transitions from high to low to determine if tristate test mode mode will be entered, or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode (SMM).
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium OverDrive processor with MMX technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When STPCLK# is asserted, the Pentium OverDrive processor with MMX technology will still respond to external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for Pentium OverDrive processor with MMX technology boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium OverDrive processor with MMX technology during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium OverDrive processor with MMX technology on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of Pentium OverDrive processor with MMX technology on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the test mode select input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC2}	I	These 28 **power** inputs are defined separately so they may be used in a split voltage plane motherboard design. These pins **must** be supplied with 3.3V for the Pentium OverDrive processor with MMX technology to function.

Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
V_{CC3}	I	These 32 **power** inputs must be connected to 3.3V in either single or split voltage systems.
V_{CC5}	I	The Pentium OverDrive processor with MMX technology has two 5V **power** inputs.
V_{SS}	I	The Pentium OverDrive processor with MMX technology has 68 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line by line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

NOTE:
Highlighted items in Table 2 are signals not supported on the Pentium® OverDrive® processor with MMX™ technology.

2.4. Pin Descriptions

2.4.1. INPUT PINS

Table 3. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#	Low	Asynchronous		
AHOLD	High	Synchronous		
BF	N/A	Synchronous/RESET	Pulldown	
BF1	N/A	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous		Bus State T2,T12,T2P
BRDYC#	Low	Synchronous	Pullup	Bus State T2,T12,T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
CPUTYP	N/A	Synchronous/RESET	Pulldown	
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
FRCMC#	N/A	Asynchronous	Pullup	
HOLD	High	Synchronous		
IGNNE#	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PICCLK	N/A	Asynchronous	Pullup	
PEN#	Low	Synchronous		BRDY#
R/S#	n/a	Asynchronous	Pullup	

Table 3. Input Pins (Continued)

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

NOTE:

Highlighted signals are original Pentium® processor 75/90/100/120/133/150/166 MHz signals and are not supported by the Pentium OverDrive® processor with MMX™ technology.

2.4.2. OUTPUT PINS

Table 4. Output Pins

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
D/P#	n/a	
FERR#	Low	
HIT#	Low	
HITM#	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO# , D/C# , W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTES:

All output pins are floated during tristate test mode (except TDO).

Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processor with MMX™ technology.

2.4.3. INPUT/OUTPUT PINS

Table 5. Input/Output Pins

Name	Active Level	When Floated	Qualified (When an Input)	Internal Resistor
A31-A3	n/a	Address hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address hold, Bus Hold, BOFF#	EADS#	
BE4#-BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown
D63-D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7-DP0	n/a	Bus Hold, BOFF#	BRDY#	
PICD0[DPEN#]				Pullup
PICD1[APICEN]				Pulldown

NOTES:

All input/output pins are floated during tristate test.

Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processor with MMX™ technology.

Table 6. Interprocessor I/O Pins

Name	Active Level	Internal Resistor
PHIT#	n/a	Pullup
PHITM#	n/a	Pullup
PBGNT#	n/a	Pullup
PBREQ#	n/a	Pullup

NOTE:

Signals are original Pentium® processor signals and are not used by the Pentium OverDrive® processor with MMX™ technology.

2.4.4. PIN GROUPING ACCORDING TO FUNCTION

Table 7 organizes the pins with respect to their function.

Table 7. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT
Address Bus	A31-A3, BE7# - BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Clock Control	STPCLK#
Probe Mode	R/S#, PRDY

Table 8. Pin Functional Groupings Not Supported by Pentium® OverDrive® Processor with MMX™ Technology

Function	Pins
APIC Support	PICCLK, PICD0-1
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Functional Redundancy Checking	FRCMC#
Miscellaneous Dual Processing	CPUTYP, D/P#
Execution Tracing	BT3-BT0, IU, IV, IBT

3.0. COMPONENT OPERATION

3.1. Core to Bus Ratio for Higher Speed

The Pentium OverDrive processor with MMX technology incorporates an internal Phase Lock Loop (PLL) and clock multiplier to generate the higher internal speeds. This allows the internal processor core to operate synchronously and at higher frequencies than the external bus.

On the 200/180-MHz Pentium OverDrive processor with MMX technology, the bus fraction configuration will be preset to 3/1 internally and 166-MHz to 5/2. See Table 9 for details.

Table 9. Core/Bus Frequencies

Internal Speed	Bus Speed	Replaces (Core/Bus)
150-MHz	50-MHz	75/50-MHz
180-MHz	60-MHz	90/60-MHz
		120/60-MHz
		150/60-MHz
166-MHz	66-MHz	100/66-MHz
		133/66-MHz
200-MHz	66-MHz	100/66-MHz
		133/66-MHz
		166/66-MHz

3.2. Hardware Interface Differences

The Pentium OverDrive processor with MMX technology is pin-for-pin compatible with the respective original Pentium processors, except for the additional pins defined by Socket 5 and 7 for the Pentium OverDrive processor with MMX technology. Some minor differences are discussed in this section and are referenced in tables in previous section. These differences represent features that are not required for an end-user CPU upgrade.

3.2.1. CPUTYP SIGNAL

The Pentium OverDrive processor with MMX technology CPUTYP signal is internally tied to ground and the signal pin on the package is an internal no-connect (INC). The original Pentium processor must be removed for the Pentium OverDrive processor with MMX technology to function properly.

3.3. Processor Initialization

3.3.1. POWER UP SPECIFICATION

The Pentium OverDrive processor with MMX technology will boot like the respective original Pentium processors. If the Pentium OverDrive processor with MMX technology is installed in a second socket of dual socket system the primary CPU must be removed or the system will not boot properly.

3.3.2. TEST AND CONFIGURATION FEATURES (BIST, FRC, TRISTATE TEST MODE)

The Pentium OverDrive processor with MMX technology will execute the Built In Self Test (BIST) and Tristate Test Mode same as the respective original Pentium processor. Functional Redundancy Checking is not supported.

3.3.3. INITIALIZATION WITH RESET, INIT AND BIST

The Pentium OverDrive processor with MMX technology handling of RESET, INIT, and the Built In Self Test (BIST) is the same as the original Pentium processors. The register states after RESET, INIT, and BIST are same as the original Pentium processors. For further information refer to Section 8 in this datasheet.

3.4. Instruction Differences

The Pentium OverDrive processor with MMX technology is 100% compatible with the Pentium processor (75-200). Two additions have been made. The 57 instructions that comprise the MMX Technology Instruction set and the RDPMC (Read Performance Monitoring Counter) instruction. These new instructions are an added feature and will not impact the use of the upgraded system in anyway unless specifically used.

3.4.1. MMX™ TECHNOLOGY EXTENSIONS TO THE INTEL ARCHITECTURE

Intel's MMX technology is an extension to the Intel architecture which provides for additional performance for multimedia and communications applications. Intel processors that include this technology are still 100% compatible with all "scalar" Intel processors. This means that all existing software that runs on existing Intel processors will continue to run (without modification) on an Intel processor that incorporates MMX technology.

Intel's MMX technology uses a SIMD (Single Instruction, Multiple Data) tecnique to speedup multimedia and communications software by processing multiple data elements in parallel. The MMX instruction set all 57 new opcodes and a new 64-bit quadword type. The new 64-bit data type holds packed integer values. These packed integer values can be 8 bytes, 4 words, or 2 double-words.

The Pentium OverDrive processor with MMX technology includes the MMX instruction set as defined by the *Intel Architecture MMX™ Technology Programmers Reference Manual* (Order #243007) and the *Intel Architecture MMX™ Technology Developer's Manual* (Order #243006). Software can determine that the system has been upgraded to a Intel Architecture processor that supports MMX technology via the CPUID instruction.

3.4.2. RDPMC (READ PERFORMANCE MONITORING COUNTER)

RDPMC will enable the user to only READ the performance monitoring counters.

3.5. CPUID

The CPUID instruction allows software to determine the type and features of the microprocessor. When executing the CPUID instruction the Pentium OverDrive processor with MMX technology behaves like the original Pentium processors:

- If the value in EAX is '0' then the 12-byte ASCII string "GenuineIntel" (little endian) is returned in EBX, EDX, and ECX. Also, a '1' is returned in EAX.
- If the value in EAX is '1' then the processor version is returned in EAX and the processor capabilities are returned in EDX. The values of EAX and EDX for the Pentium® OverDrive® processor with MMX™ technology are given below.
- If the value in EAX is neither '0' nor '1', Pentium OverDrive processor with MMX technology writes '0' to all registers or is undefined.

The stepping field has the same format as the original Pentium processor and will be the same for the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology will have a unique CPUID from the original Pentium processor and the Pentium processor with MMX technology (154xH Vs. 052xH and 054xH). The type field is defined in Table 11.

Table 10. EAX Bit Values Definition for CPUID

CPU	31...14	13...12	11...8	7...4	3...0
Field Definition	(reserved)	type	family	model	stepping
Pentium® processor (75, 90, 100)	(reserved)	Table 11	5H	2H	varies
Pentium processor with MMX™ technology (166, 200, 233-MHz)	(reserved)	Table 11	5H	4H	varies
Pentium OverDrive® processor with MMX technology	(reserved)	Table 11	5H	4H	varies

Table 11. EAX Bit Values Definition for Processor Type

Bit 13	Bit 12	Processor Type
0	0	Primary Pentium® processor
0	0	Primary Pentium processor with MMX™ technology
0	1	Pentium OverDrive® processor with MMX technology
1	0	Dual Pentium processor *
1	1	Reserved

NOTE:

* The Pentium® OverDrive® processor with MMX™ technology does not support Dual Processing mode.

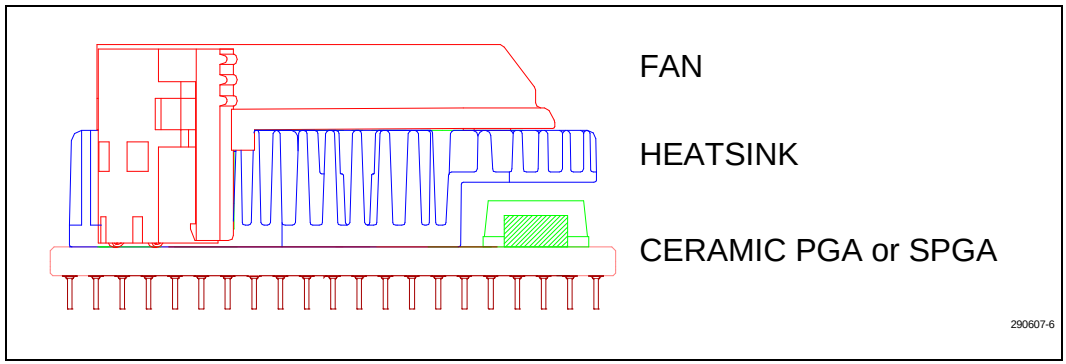


Figure 6. Pentium® OverDrive® Processor with MMX™ Technology with Fan/Heatsink

3.6. On-Package Fan/Heatsink

The on-package fan/heatsink included with the Pentium OverDrive processor with MMX technology requires different stress ratings than the original Pentium processor. The fan is a detachable unit, and the storage temperature is stated separately in Table 12. Operation of the Pentium OverDrive processor with MMX technology is defined at T_A = 10°C to 45°C. The fan/heatsink is shown in Figure 6.

3.7. On-Package Voltage Regulator

The Pentium OverDrive processor with MMX technology has an on-package voltage regulator to supply 2.8 volts to the processor core. This allows the Pentium OverDrive processor with MMX technology to function in a 3.3 volt only system.

3.8. Cache Support

The Pentium OverDrive processor with MMX technology has an enhanced internal cache (2x16KB Total, 4 way set-associative Code and Data caches, each with improved TLBs) and will support the L2 caches supported by the Pentium processor (75-200). The Pentium OverDrive processor with MMX technology supports the Intel 82430 chipsets. **Chipsets with 5V signal levels, 82497/82492 cache controller, and the 82498/82493 cache controller are not supported by the Pentium OverDrive processor with MMX technology.**

3.9. Code Prefetch Queue and Branch Target Buffers

Code should not be written to rely on the specific code prefetch queue or branch target buffer mechanism of a particular processor. With each new generation and family of processors, these mechanisms are subject to change.

3.10. I/O Buffers

The Pentium OverDrive processor with MMX technology buffer models comply with the specifications for the buffer model for the respective original Pentium processor. The circuit topology is the same and the ranges of values in the Pentium OverDrive processor with MMX technology model are within the original Pentium processor ranges. The buffer models used by the Pentium OverDrive processor with MMX technology accurately model flight time and signal quality.

3.11. Test Register Access

The Pentium OverDrive processor with MMX technology have test registers which allow testing of different areas of the processor. These test registers are called Model Specific Registers (MSR). These MSR's are accessed using the RDMSR and WRMSR instructions.

4.0. BIOS AND SOFTWARE

The Pentium OverDrive processor with MMX technology is a drop-in replacement for the respective original Pentium processor. BIOS changes are not normally necessary but might be required. Please call Intel Technical Support hotline if assistance is required. Pentium OverDrive processor with MMX technology is 100% backward software compatible with their respective original Pentium processors.

5.0. ELECTRICAL SPECIFICATIONS

This section describes the electrical differences between the Pentium processor (75-200) and the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology requires 3.3 volts to power the processor. The voltage to the socket is 3.3 volt and is converted by an on-package voltage regulator to the proper voltage for the processor's internal core voltage plane. The internal 3.3 volt I/O plane is powered from the socket to the processor. The Pentium OverDrive processor with MMX technology looks like a 3.3 volt device externally.

5.1. Power and Ground

For clean on-chip power distribution, the Pentium OverDrive processor with MMX technology in an SPGA package has 60 V_{CC} (power) and 68 V_{SS} (ground) inputs. The 28 V_{CC2} pins are connected internally to a power plane that provides power to the on-package voltage regulator for the core supply. The 32 V_{CC3} pins are connected internally to a separate power plane that provides power to the I/O buffers. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the Pentium OverDrive processor with MMX technology. On the circuit board all V_{CC} pins must be connected to a 3.3V V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

The Pentium OverDrive processor with MMX technology pinout contains two 5V V_{CC} pins (V_{CC5}) used to provide power to the fan/heatsink. These pins should be connected to +5 volts ±5% regardless of the system design.

5.2. Decoupling Recommendations

Decoupling recommendation for the original Pentium processor apply to the Pentium OverDrive processor with MMX technology upgradable systems and capacitors should be placed near the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology can cause transient power surges, particularly when driving large capacitive loads. The Pentium OverDrive processor with MMX technology are shipped with adequate decoupling capacitors on the package to limit transients in excess of Pentium processors tolerance. It is recommended to follow the original Pentium processor specification for decoupling recommendations.

5.3. Other Connection Recommendations

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to ground. All NC pins must remain unconnected.

5.4. Absolute Maximum Ratings

The tables in this section provide environmental stress ratings for the Pentium OverDrive processor with MMX technology. Functional operation at the absolute maximum and minimum is not implied or guaranteed. Extended exposure to maximum ratings may affect device reliability. Furthermore, precautions should be taken to avoid high static voltages and electric fields to prevent static electric discharge. Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. The tables contain stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.

Table 12. Absolute Maximum Ratings without Fan/Heatsink

Symbol	Parameter	Min	Max	Unit	Notes
	Storage Temperature	-40	+125	^{0}C	
	Case Temperature Under Bias	-40	+110	^{0}C	
V_{CC3}	3.3 V Supply Voltage with respect to V_{SS}	-0.5	+4.6	V	
V_{CC5}	5 V Supply Voltage with respect to V_{SS}	-0.5	6.5	V	
V_{IN}	3.3 V Only Buffer DC Input Voltage	-0.5	V_{CC3}+0.5V not to exceed 4.6V MAX	V	(2)
V_{INSB}	5.0V Safe Buffer DC Input Voltage	-0.5	+6.5	V	(1) (3)

NOTES:

1. Applies to the CLK and PICCLK.
2. Applies to all Pentium® OverDrive® processor with MMX™ technology inputs except CLK and PICCLK.
3. See overshoot/undershoot transient specification in the *Pentium® Family User's Manual, Volume 1.*

Table 13. Absolute Maximum Ratings for Fan/Heatsink Only

	Parameter	Min	Max	Unit	Notes
Fan:					
	Storage Temperature	-40	70	°C	
	Case Temperature Under Bias	-5	60	°C	
V_{CC5}	5V Fan Supply Voltage with Respect to V_{SS}	-0.5	6.5	V	

5.5. D.C. Specifications

The Pentium OverDrive processor with MMX technology will have compatible D.C. specifications to the original Pentium processor, except for I_{CC} (Power Supply Current) and I_{CC5} (Fan/Heatsink Current). The Pentium OverDrive processor with MMX technology voltage specification are V_{CC3} = 3.135V to 3.6V and V_{CC5} = 5V ±5%.

Table 14 lists the D.C. specifications which apply to the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology requires a 3.3V power supply and 3.3V input signals with the exception of CLK and signals which are 5V tolerant.

Table 14. 3.3V D.C. Specifications

V_{CC} = 3.135V to 3.6V (See Notes 6, 7), T_A = 10 to 45°C					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	Input Low Voltage	-0.3	0.8	V	TTL Level (3)
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	TTL Level (3)
V_{OL}	Output Low Voltage		0.4	V	TTL Level (1) (3)
V_{OH}	Output High Voltage	2.4		V	TTL Level (2) (3)
V_{IL5}	Input Low Voltage	-0.3	0.8	V	TTL Level (8)
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level (8)
I_{CC5}	Fan/Heatsink Current		200	mA	
I_{CC3}	Power Supply Current		4330	mA	@50/125 MHz (4)(5)
			4330	mA	@60/150 MHz (4)(5)
			4330	mA	@60/180 MHz (4)(5)
			4330	mA	@66/166 MHz (4)(5)
			5000	mA	@66/200 MHz (4)(5)
I_{CC5}	Fan/Heatsink Current		200	mA	
I_{CCSB}	Standby	450	770	mA	

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3 volt TTL levels apply to all signals except CLK and PICCLK.
4. For worst case conditions: V_{CC3}+5% and T_{CASE} = 10°C.
5. Power supply transient response and decoupling capacitors must be sufficient to handle the current transients required when transitioning from standby to full power mode.
6. Refer to Chapter 23 in the *Pentium® Family User's Manual, Volume 1,* for a listing of the remaining D.C. Specifications.
7. The worst case ambient temperature is T_A = 45° C.
8. Applies to 5V safe inputs: CLK and PICCLK.

5.6. A.C. Specifications

5.6.1. A. C. TABLES FOR A 50-MHZ BUS

The AC specifications of the 180/150-Pentium OverDrive processor with MMX technology consist of setup times, hold times, and valid delays at 0pF.

The A.C. specifications given in Table 15 consist of output delays, input setup requirements and input hold requirements for a 50-MHz external bus. All A.C. specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both “0” and “1” logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct 150-MHz Pentium OverDrive processor with MMX technology running 125-MHz operation.

Table 15. 50-MHz Bus A.C. Specifications

$3.135 < V_{CC} < 3.6V$, TA = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
	Frequency	25.0	50.0	MHz		Max core Freq = 125 MHz @ 2/5
t_{1a}	CLK Period	20.0	40.0	nS	7	
t_{1b}	CLK Period Stability		±250	pS	7	Adjacent Clocks, (1), (25)
t_2	CLK High Time	4.0		nS	7	@2V, (1)
t_3	CLK Low Time	4.0		nS	7	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	7	(2.0V-0.8V), (1)
t_5	CLK Rise Time	0.15	1.5	nS	7	(0.8V-2.0V), (1)
t_{6a}	ADS#, ADSC#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	8	
t_{6b}	AP Valid Delay	1.0	8.5	nS	8	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	8	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	8	(1)
t_8	PCHK#, APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	8	(4)
t_9	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	nS	8	(4)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	8	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	8	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	8	

Table 15. 50-MHz Bus A.C. Specifications (Continued)

3.135 < V_{CC} < 3.6V, T_A = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	8	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	8.5	nS	8	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	9	(1)
t_{14}	A5-A31 Setup Time	6.5		nS	10	
t_{15}	A5-A31 Hold Time	1.0		nS	10	
t_{16a}	INV, AP Setup Time	5.0		nS	10	
t_{16b}	EADS# Setup Time	6.0		nS	10	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	10	
t_{18a}	KEN# Setup Time	5.0		nS	10	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	10	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	10	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	10	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	10	
t_{22}	BOFF# Setup Time	5.5		nS	10	
t_{22a}	AHOLD Setup Time	6.0		nS	10	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	10	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	10	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	10	
t_{25b}	HOLD Hold Time	1.5		nS	10	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	10	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	10	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	10	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	10	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	11	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	10	(12)

Table 15. 50-MHz Bus A.C. Specifications

3.135 < V_{CC} < 3.6V, TA = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.8		nS	10	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2.0		nS	10	
t_{36}	RESET Setup Time	5.0		nS	11	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	11	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	11	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	11	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	11	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	11	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	11	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	11	To RESET falling edge (20)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	11	To RESET falling edge (20)
t_{42d}	Reset Configuration Signals (BRDYC#) Hold Time, RESET Driven Synchronously.	1.0		nS		To RESET falling edge (1), (27)
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	7	
t_{46}	TCK High Time	25.0		nS	7	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	7	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	7	(2.0V-0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	7	(0.8V-2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	13	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	12	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	12	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	12	(8)

Table 15. 50-MHz Bus A.C. Specifications

3.135 < V_{CC} < 3.6V, TA = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{54}	TDO Float Delay		25.0	nS	12	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	12	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	12	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	12	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	12	(3), (7), (10)

NOTES:

Notes 2, 6, and 13 are general and apply to all standard TTL signals used with the Pentium® OverDrive processor with MMX™ technology.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/nS rise and fall times.
3. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
6. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the max TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
11. Setup time is required to guarantee recognition on a specific clock. This is not applicable to the Pentium OverDrive processor with MMX technology.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5 V.
14. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously. However, when operating the Pentium® OverDrive® processor with MMX™ technology, FLUSH# and RESET must be asserted synchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF, BF1, and CPUTYP should be strapped to V_{CC} or V_{SS}.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency specturm should not have any power spectrum peaking between 500KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. BRDYC# and BUSCHK# are used as Reset configuration signals to select buffer size.
21. The value of this signal may have been changed, check the latest Pentium Processor Data Book for the updated values.

** Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

5.6.2. A. C. TABLES FOR A 60-MHZ BUS

The A.C. specifications given in Table 16 consist of output delays, input setup requirements and input hold requirements for a 60-MHz external bus. All A.C. specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct 180-MHz Pentium OverDrive processor with MMX technology operation.

Table 16. 60-MHz Bus A.C. Specifications

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
	Frequency	30	60.0	MHz		Max core Freq = 150 MHz @ 2/5
t_{1a}	CLK Period	16.67	33.33	nS	7	
t_{1b}	CLK Period Stability		±250	pS	7	Adjacent Clocks, (1), (25)
t_2	CLK High Time	4.0		nS	7	@2V, (1)
t_3	CLK Low Time	4.0		nS	7	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	7	(2.0V-0.8V), (1)
t_5	CLK Rise Time	0.15	1.5	nS	7	(0.8V-2.0V), (1)
t_{6a}	ADS#, ADSC#, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	nS	8	
t_{6b}	AP Valid Delay	1.0	8.5	nS	8	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	8	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	9	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	8	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.8	nS	8	(4)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	8	(4)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	8	(4)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	8	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	8	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	8	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	8	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	8	

Table 16. 60-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	9	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	10	
t_{15}	A5-A31 Hold Time	1.0		nS	8	
t_{16a}	INV, AP Setup Time	5.0		nS	8	
t_{16b}	EADS# Setup Time	5.5		nS	8	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	8	
t_{18a}	KEN# Setup Time	5.0		nS	8	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	8	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	8	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	8	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	8	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	8	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	8	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	8	
t_{25}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	8	
t_{25a}	HOLD Hold Time	1.5		nS	8	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	8	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	8	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	8	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	8	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	8	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	8	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.0		nS	8	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	8	

Table 16. 60-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{36}	RESET Setup Time	5.0		nS	9	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	9	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	9	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	9	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	9	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	9	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	9	(15)
t_{42b}	Reset Configuration Signals (FLUSH#, BRDYC#, INIT, BUSCHK#) Hold Time, Async.	2.0		CLKs	9	(20)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	9	(20)
t_{42d}	Reset Configuration Signals (BRDYC#) Hold Time, RESET Driven Synchronously.	1.0		nS		To RESET falling edge (1), (27)
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	7	
t_{46}	TCK High Time	25.0		nS	7	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	7	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	7	(2.0V-0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	7	(0.8V-2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	13	Asynchronous, (1)
t_{51}	TDI, TMS Setup Time	5.0		nS	12	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	12	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	12	(8)
t_{54}	TDO Float Delay		25.0	nS	12	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	12	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	12	(1), (3), (8), (10)

Table 16. 60-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	12	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	12	(3), (7), (10)

NOTES:

Notes 2, 6, and 13 are general and apply to all standard TTL signals used with the Pentium® OverDrive processor with MMX™ technology.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/nS rise and fall times.
3. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
6. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the max TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
11. Setup time is required to guarantee recognition on a specific clock. This is not applicable to the Pentium OverDrive processor with MMX technology.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5 V.
14. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously. However, when operating the Pentium® OverDrive® processor with MMX™ technology, FLUSH# and RESET must be asserted synchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF, BF1, and CPUTYP should be strapped to V_{CC} or V_{SS}.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency specturm should not have any power spectrum peaking between 500KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. BRDYC# and BUSCHK# are used as Reset configuration signals to select buffer size.
21. The value of this signal may have been changed, check the latest Pentium Processor Data Book for the updated values.

** Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

5.6.3. A. C. TABLES FOR A 66-MHZ BUS

The A.C. specifications given in Table 17 consist of output delays, input setup requirements and input hold requirements for a 66-MHz external bus. All A.C. specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct 200-MHz Pentium OverDrive processor with MMX technology operation.

Table 17. 66-MHz Bus A.C. Specifications

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
	Frequency	33.33	66.6	MHz		Max core Freq = 166 MHz @ 2/5
t_{1a}	CLK Period	15.0	30.0	nS	7	
t_{1b}	CLK Period Stability		±250	pS	7	Adjacent Clocks, (1), (25)
t_2	CLK High Time	4.0		nS	7	@2V, (1), (5)
t_3	CLK Low Time	4.0		nS	7	@0.8V, (1), (5)
t_4	CLK Fall Time	0.15	1.5	nS	7	(2.0V-0.8V),(1),(5)
t_5	CLK Rise Time	0.15	1.5	nS	7	(0.8V-.0V),(1),(5)
t_{6a}	ADSC#, PWT, PCD, BE0-7#, D/C#, W/R#, CACHE#, SCYC, Valid Delay	1.0	7.0	nS	8	
t_{6b}	AP Valid Delay	1.0	8.5	nS	8	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	8	
t_{6d}	ADS#, MIO# Valid Delay	1.0	6.0	nS	8	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	9	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	8	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	8	(4)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	8	(4), (21)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	8	(4), (21)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	8	(21)
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	8	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	8	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	8	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	8	(21)

Table 17. 66-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	9	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	10	
t_{15}	A5-A31 Hold Time	1.0		nS	10	
t_{16a}	INV, AP Setup Time	5.0		nS	10	
t_{16b}	EADS# Setup Time	5.5		nS	10	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	10	
t_{18a}	KEN# Setup Time	5.0		nS	10	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	10	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	10	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	10	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	10	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	10	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	10	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	10	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	10	
t_{25b}	HOLD Hold Time	1.5		nS	10	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	10	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	10	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	10	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	10	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	10	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	10	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.0		nS	10	(21)
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2.0		nS	10	(21)

Table 17. 66-MHz Bus A.C. Specifications (Continued)

3.135 < V_{CC} < 3.6V, T_A = 10 to 45°C, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{36}	RESET Setup Time	5.0		nS	11	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	11	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	11	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	11	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	11	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	11	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	11	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#,BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	11	To RESET falling edge (20)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	11	To RESET falling edge (20)
t_{42d}	Reset Configuration Signals (BRDYC#) Hold Time, RESET Driven Synchronously.	1.0		nS		To RESET falling edge (1), (27)
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	7	
t_{46}	TCK High Time	25.0		nS	7	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	7	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	7	(2.0V-0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	7	(0.8V-2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	13	Asynchronous, (1)
t_{51}	TDI, TMS Setup Time	5.0		nS	12	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	12	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	12	(8)
t_{54}	TDO Float Delay		25.0	nS	12	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	12	(3), (8), (10)

Table 17. 66-MHz Bus A.C. Specifications (Continued)

$3.135 < V_{CC} < 3.6V$, $T_A = 10$ to $45°C$, $C_L = 0$ pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	12	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	12	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	12	(3), (7), (10)

NOTES:

Notes 2, 6, and 13 are general and apply to all standard TTL signals used with the Pentium® OverDrive processor with MMX™ technology.

1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3 Volt transitions with 1Volt/nS rise and fall times.
3. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8 V/ns <= CLK input rise/fall time <= 8 V/ns.
6. 0.3 V/ns <= Input rise/fall time <= 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1ns can be added to the max TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
11. Setup time is required to guarantee recognition on a specific clock. This is not applicable to the Pentium OverDrive processor with MMX technology.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5 V.
14. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously. However, when operating the Pentium® OverDrive® processor with MMX™ technology, FLUSH# and RESET must be asserted synchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF, BF1, and CPUTYP should be strapped to V_{CC} or V_{SS}.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency specturm should not have any power spectrum peaking between 500KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. BRDYC# and BUSCHK# are used as Reset configuration signals to select buffer size.
21. The value of this signal may have been changed, check the latest Pentium Processor Data Book for the updated values.

** Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

5.6.4. TIMING AND WAVEFORMS

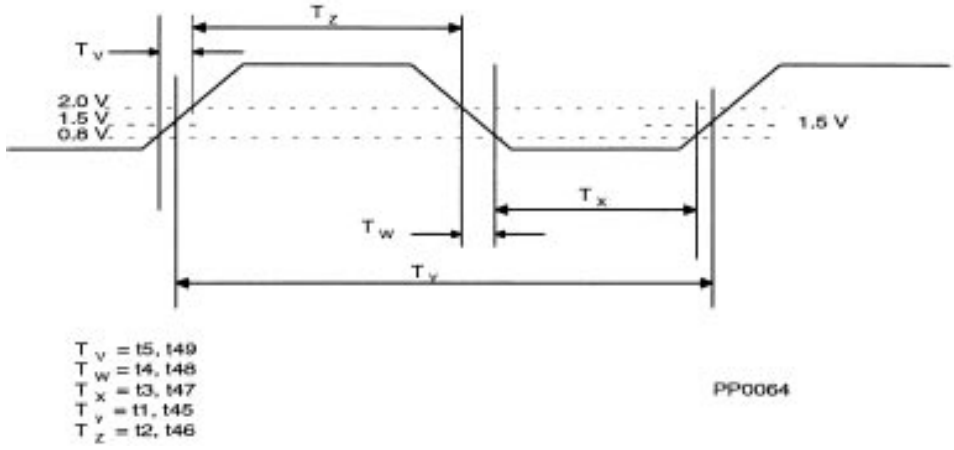


Figure 7. Clock Waveform

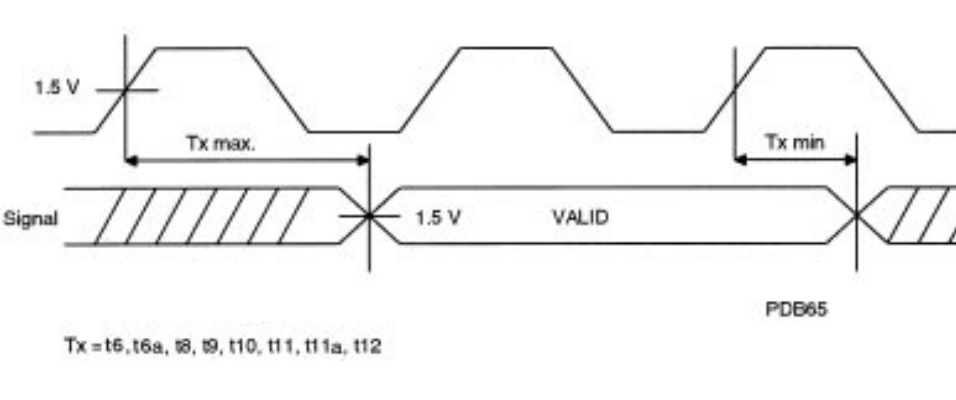


Figure 8. Valid Delay Timing

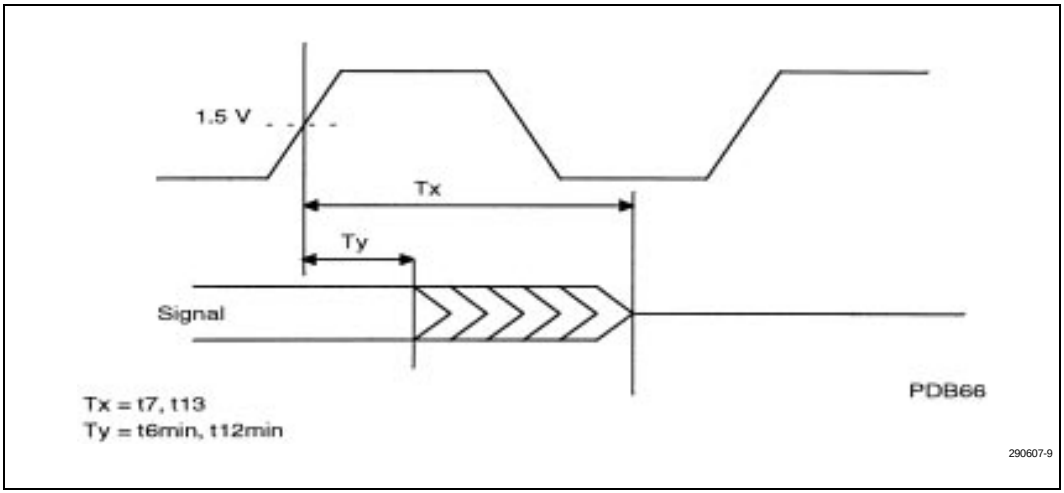


Figure 9. Float Delay Timing

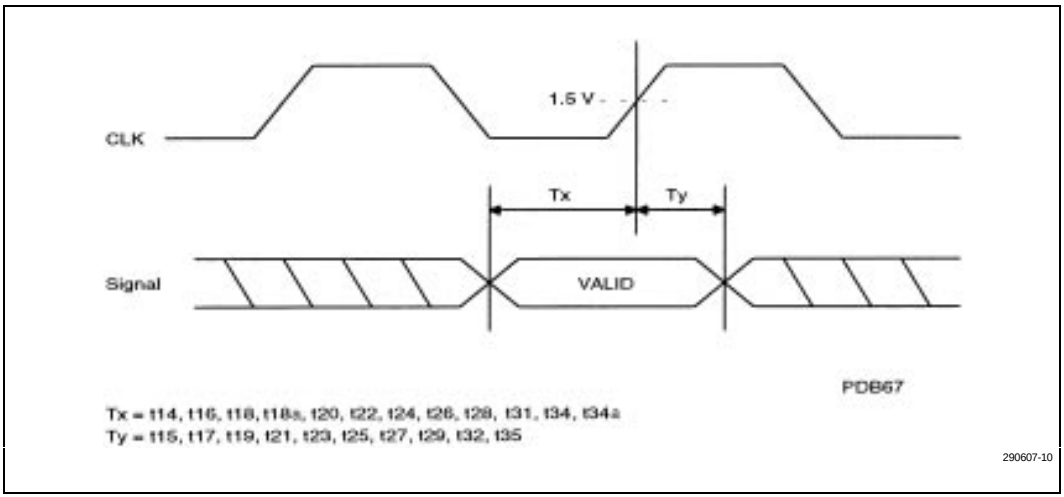


Figure 10. Setup and Hold Timing

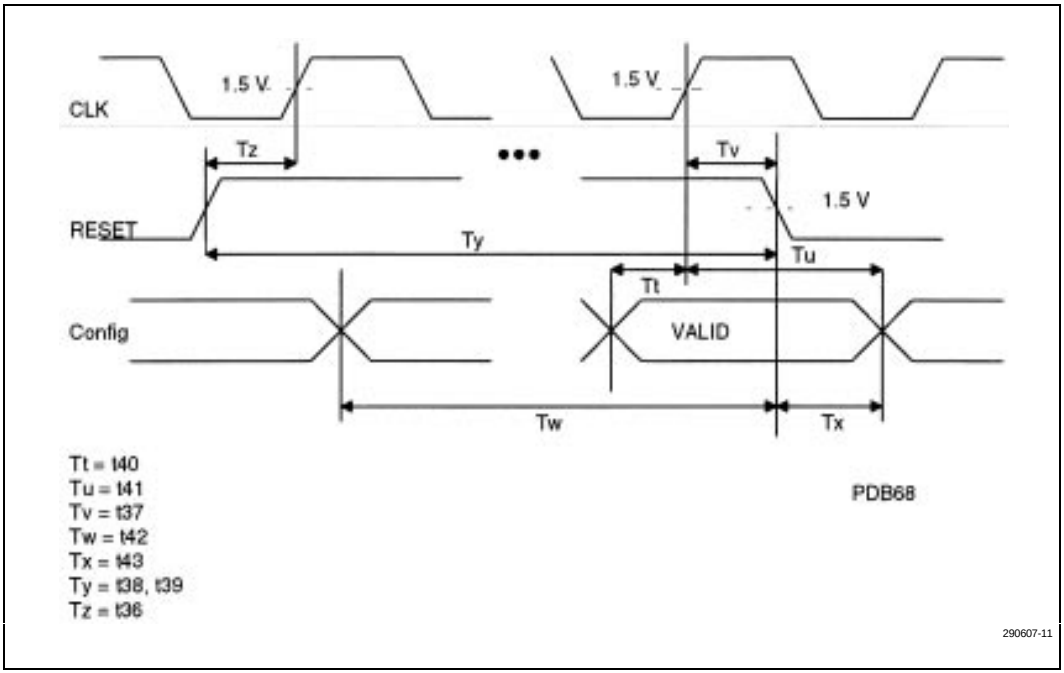


Figure 11. Reset and Configuration Timing

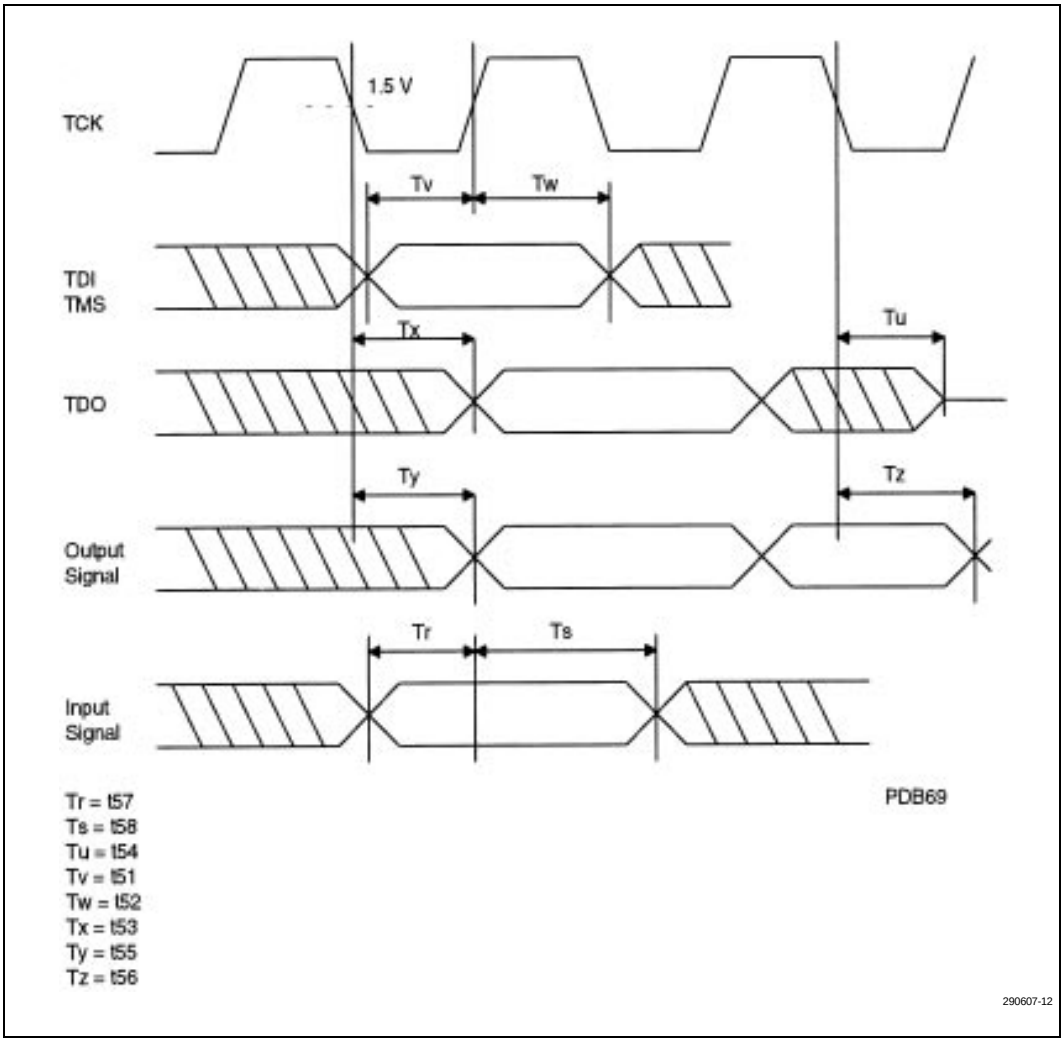


Figure 12. Test Timing

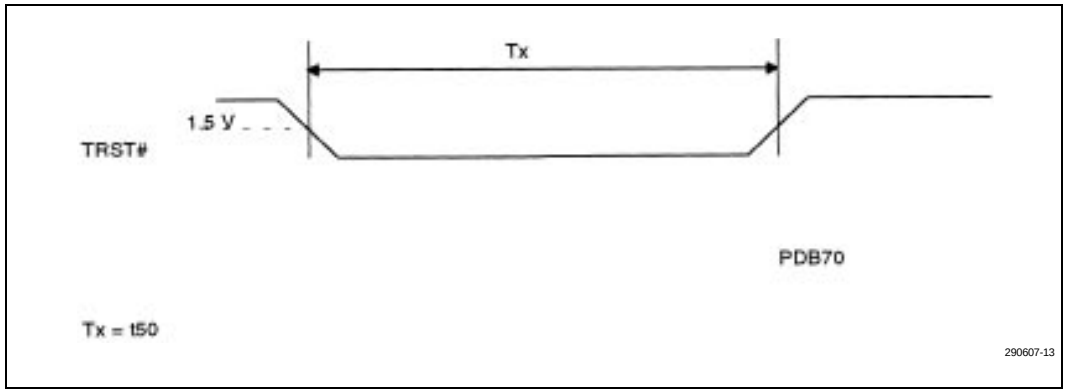


Figure 13. Reset and Configuration Timing

6.0. MECHANICAL SPECIFICATIONS

6.1. Package Dimensions

The Pentium OverDrive processor with MMX technology, an upgrade for the 75, 90, 100-MHz Pentium processor-based systems, uses a 320-pin ceramic staggered pin grid array (SPGA) package. The pins will be arranged in a 37 x 37 matrix and the package dimensions will be 1.95″ x 1.95″ (4.95cm x 4.95cm). See Table 18.

Table 18. Pentium® OverDrive® Processor with MMX™ Technology Package Summary

	Package Type	Total Pins	Pin Array	Package Size
Pentium® OverDrive® Processor with MMX™ Technology	SPGA	320	37 x 37	1.95” x 1.95” 4.95cm x 4.95cm

NOTE:

The mechanical specifications are provided in Table 19. Figure 14 shows the package dimensions for the Pentium® OverDrive® processor with MMX™ technology.

Table 19. Package Dimensions

Family: Ceramic Staggered Pin Grid Array Package						
Symbol	**Millimeters**			**Inches**		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
A*		33.88	Solid Lid		1.334	Solid Lid
A1	0.33	0.43	Solid Lid	0.013	0.017	Solid Lid
A2	2.62	2.97		0.103	0.117	
A4		20.32			0.800	
A5	10.16		Air Space	0.400		Air Space
B	0.43	0.51		0.017	0.020	
D	49.28	49.91		1.940	1.965	
D1	45.47	45.97		1.790	1.810	
E1	2.41	2.67		0.095	0.105	
E2	1.14	1.40		0.045	0.055	
L	3.05	3.30		0.120	0.130	
N	320		SPGA pins	320		SPGA pins
S1	1.52	2.54		0.060	0.100	

NOTES:

* Assumes the minimum air space above the fan/heatsink.

A 0.2″ clearance around three of four sides of the package is also required to allow free airflow through the fan/heatsink.

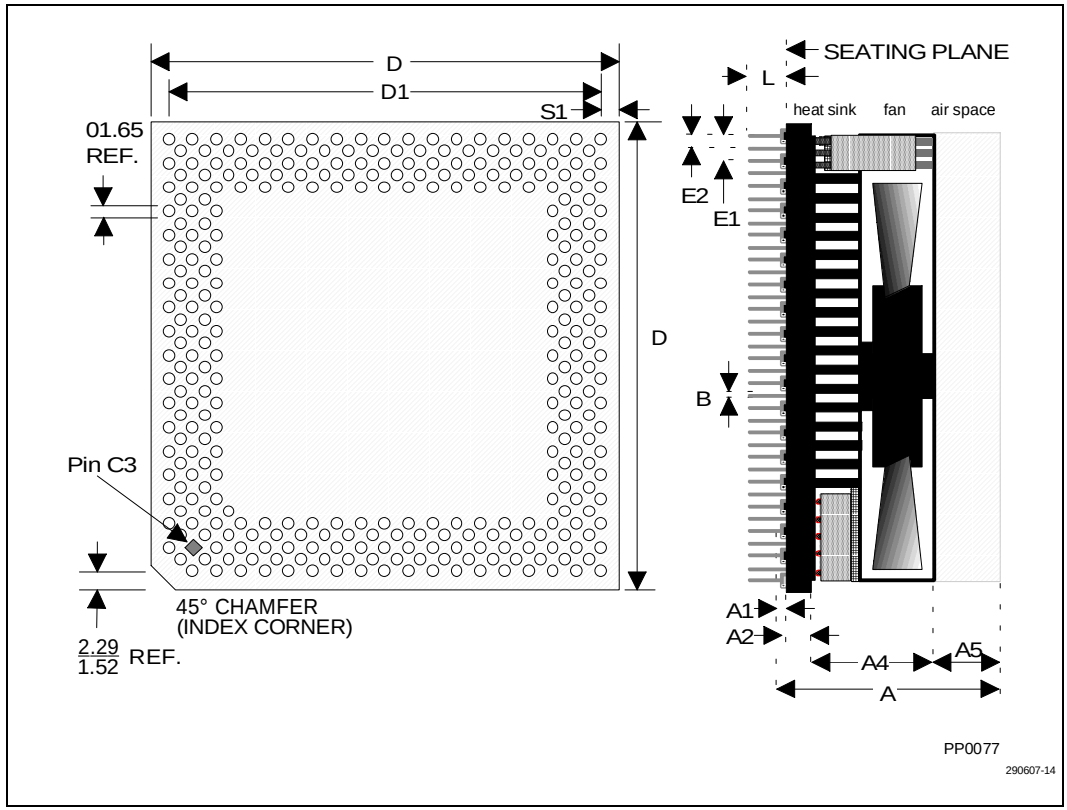


Figure 14. Pentium® OverDrive® Processor with MMX™ Technology Package Dimensions

6.2. Spatial Requirements

The Pentium OverDrive processor with MMX technology employs a fan/heatsink thermal management device. Clearance requirements must be met around the fan/heatsink to ensure unimpeded air flow for proper cooling. Figure 15 shows the Pentium OverDrive processor with MMX technology's fan/heatsink space requirements.

The Pentium OverDrive processor with MMX technology has spatial requirements defined in the respective socket specification that must be met. As shown in Figure 16, it is acceptable to allow any device (i.e., add-in cards, surface mount device, chassis, etc.) to enter within the free space distance of 0.2" from the Pentium OverDrive processor with MMX technology package if it is not taller than the level of the heatsink base. In other words, if a component is taller than height "B," it cannot be closer to the Pentium OverDrive processor with MMX technology package than distance "A". This applies to three of the four sides of the Pentium OverDrive processor with MMX technology package, although the back and handle sides of a ZIF socket will generally automatically meet this specification since they have widths larger than distance "A." Compliance to this requirement will ensure systems can be upgraded to the Pentium OverDrive processor with MMX technology.

NOTE:
Z = 1.4 for Pentium® OverDrive® processor with MMX™ technology.

Figure 15. Illustrates Physical Space Requirements for the Pentium® OverDrive® Processor with MMX™ Technology

Figure 16. Required Free Space from Sides of SPGA Package

6.3. Socket

6.3.1. SOCKET COMPATIBILITY

Socket 5 (320 pins) and Socket 7 (321 pins) are defined specifically for the requirements of the Pentium OverDrive processor with MMX technology. Socket 5 and Socket 7 define a fifth row of pins in the inside of the 296-pin SPGA socket. The rows "E" and "AJ" are the new rows of pins defined by Socket 5 and Socket 7. Socket 5 and Socket 7 are a superset of the original 75, 90, and 100-MHz Pentium processor (296 pins) pinout.

The Pentium OverDrive processor with MMX technology sockets are compatible with their respective original Pentium processors. To insure proper operation of Pentium OverDrive processor with MMX technology, all power and ground pins should be connected as defined by the respective socket definitions.

6.3.2. SOCKET 5 PINOUT

Socket 5 is the 320-pin ZIF (Zero Insertion Force) socket recommended for the 150/166-Pentium OverDrive processor with MMX technology. The Socket 5 pinout is defined with additional power and ground pins to ensure proper functionality of the Pentium OverDrive processor with MMX technology. The pinout is also specifically defined to ensure proper orientation for the Pentium OverDrive processor with MMX technology.

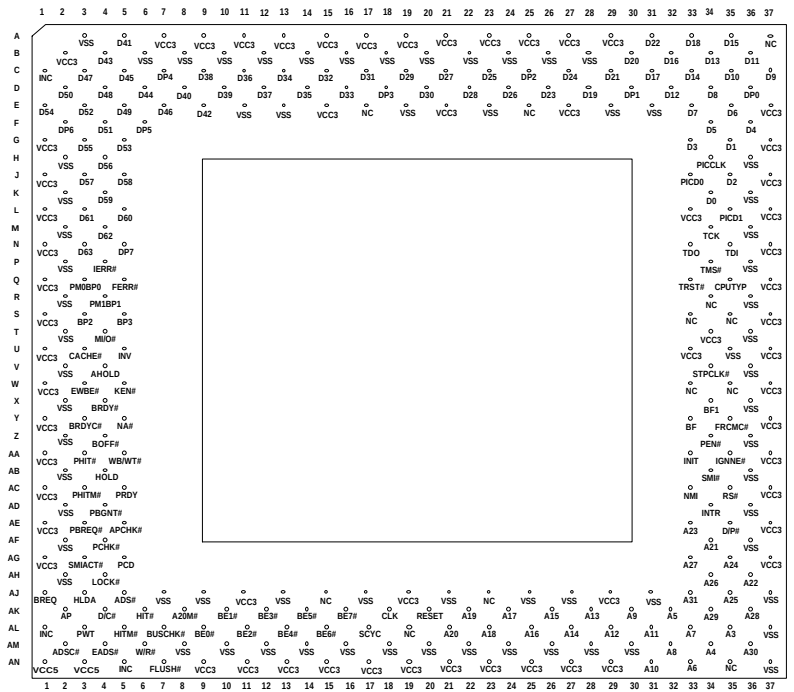
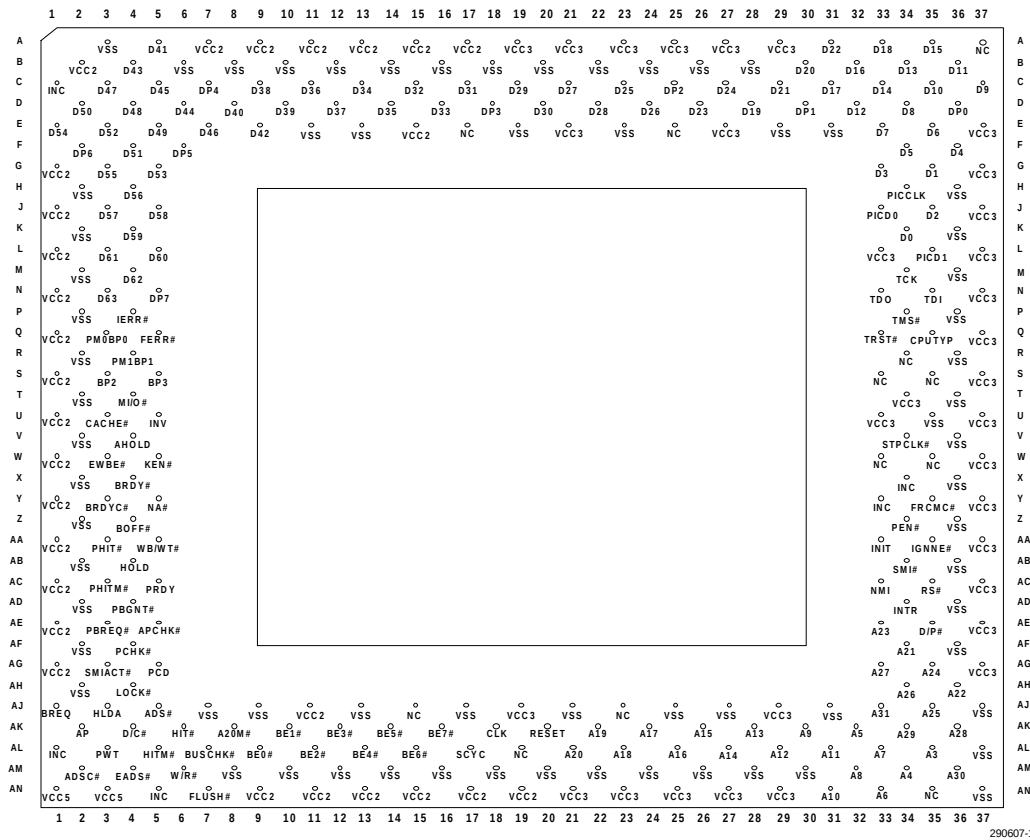


Figure 17. 320-Pin Socket 5

6.3.3. SOCKET 7 PINOUT

Socket 7 is a 321-pin ZIF (Zero Insertion Force) socket recommended for future Pentium and Pentium OverDrive processors and should be used for all new designs. Socket 7 is pin compatible with the 320-pin Socket 5 with the addition of a key pin. Contact Intel for further information.



NOTE:
Shaded pins are internal no connects on the Pentium® OverDrive® processor with MMX™ technology.

Figure 18. Pentium® OverDrive® Processor with MMX™ Technology Pinout—Top Side View

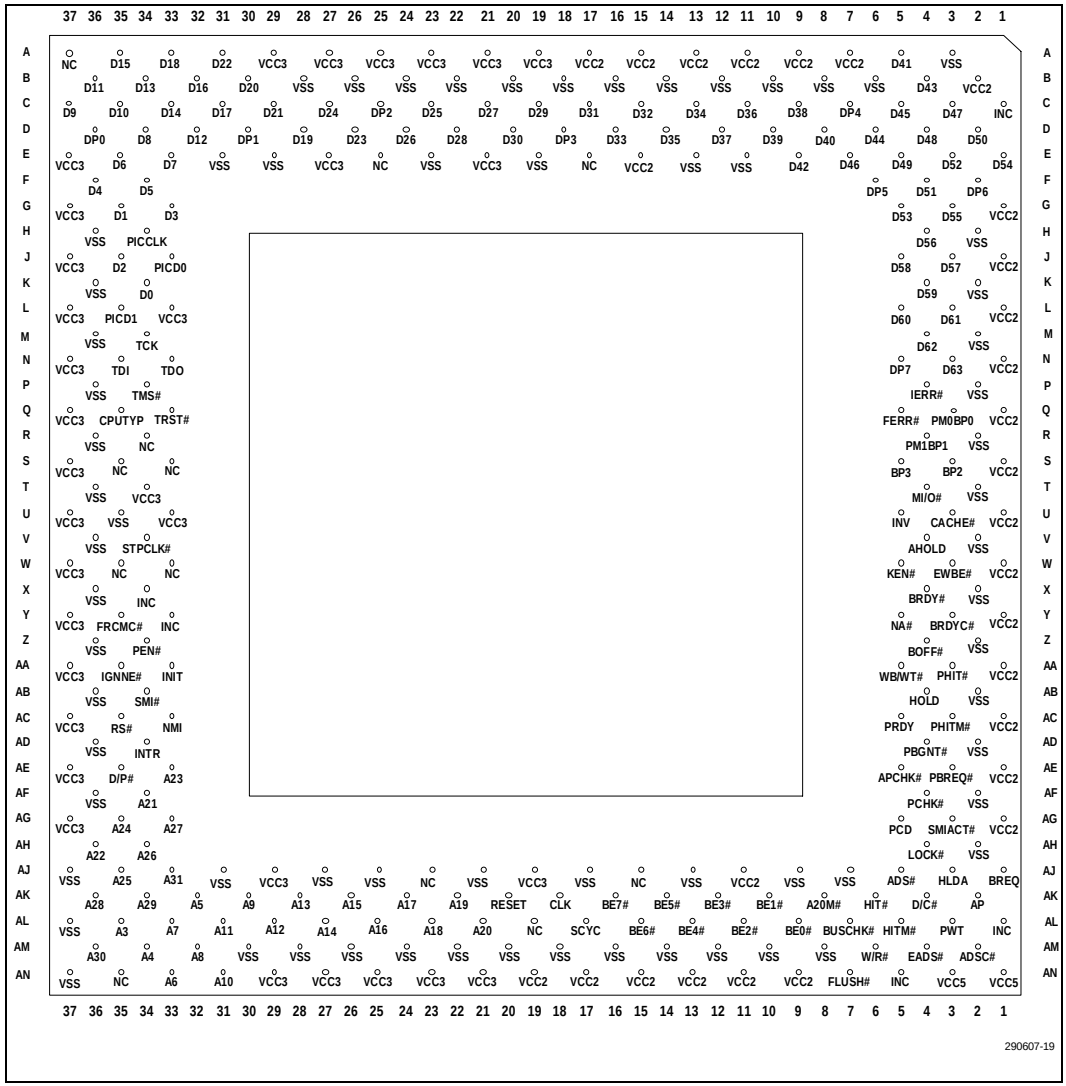


Figure 19. Pentium® OverDrive® Processor with MMX™ Technology Pinout—Pin Side View

7.0. THERMAL SPECIFICATIONS

The Pentium OverDrive processor with MMX technology is shipped with an attached fan/heatsink for a complete thermal solution for the processor upgrade. The fan/heatsink cooling solution will properly cool the Pentium OverDrive processor with MMX technology provided the space requirements of Section 6.2 are met and the maximum air temperature entering the fan/heatsink (T_A) does not exceed 45°C. The fan/heatsink inlet temperature (T_A) is measured 0.3" above the centerline of the fan hub at the system maximum ambient operating temperature (see Figure 15).

8.0. TESTABILITY

8.1. Introduction

This section describes the features which are included in the Pentium OverDrive processor with MMX technology for purposes of testability of the part. The testability features provided for the original Pentium processor are also available on the Pentium OverDrive processor with MMX technology. The Pentium OverDrive processor with MMX technology however, does not support the IEEE Standard 1149.1 boundary scan using the Test Access Port (TAP) and TAP Controller as described in Chapters 11 and 27 of the *Pentium® Family User's Manual, Volume 1*. Contact your Intel representative for further details. Some features of testability are described below.

8.2. Built in Self Test (BIST)

Self test is initiated by driving the INIT pin high when RESET transitions from high to low. No bus cycles are run by the Pentium OverDrive processor with MMX technology during self test. The duration of self test is approximately 2^{19} clocks. BIST is used to test approximately 70% of the devices in the Pentium OverDrive processor with MMX technology.

The Pentium OverDrive processor with MMX technology BIST consists of two parts: hardware self test and microcode self test. During the hardware portion of BIST, the microcode and the large PLAs are tested. All possible input combinations of the microcode ROM and PLAs are tested. The microcode self test is done by comparing the stored value of ROM check sums with the result of the self test.

If a mismatch occurs or errors are detected during BIST, the Pentium OverDrive processor with MMX technology will assert the IERR# pin and attempt to shutdown.

8.3. Tri-State Test Mode

When the FLUSH# pin is sampled low in the clock prior to the RESET pin going from high to low, the Pentium OverDrive processor with MMX technology enters tristate test mode. The Pentium OverDrive processor with MMX technology floats all of its output pins and bi-directional pins including pins which are never floated during normal operation (except TD0). Tristate test mode can be initiated in order to facilitate testing of board connections. The Pentium OverDrive processor with MMX technology remains in tristate test mode until the RESET pin is toggled again.

APPENDIX A

Pentium® OverDrive® Processor with MMX™ Technology UPGRADABILITY DESIGN CONSIDERATIONS

Intel has designed the family of Pentium OverDrive processors so that they can be easily installed by the end-user. PC manufactures can support this by implementing the design considerations listed in Table 20.

Table 20. Design Considerations

Design Consideration	Implementation
Visible Pentium® OverDrive® Processor with MMX™ Technology Socket	The Pentium OverDrive processor socket should be easily visible when the PC's cover is removed. Label the Pentium OverDrive processor socket and the location of pin 1 by silk screening this information on the PC board.
Accessible Pentium OverDrive Processor Socket	Make the Pentium processor easily accessible to the end user (i.e., do not place the Intel Pentium OverDrive processor socket under the hard disk). If the low insertion force (LIF) is used, position the Pentium OverDrive processor socket on the PC board such that there is ample clearance around the socket.
Foolproof Chip Orientation	Intel packages all Pentium OverDrive processors with a "keyed pin configuration" that insures that the Pentium OverDrive processors fits into the respective sockets in the correct orientation.
Zero Insertion Force Upgrade Socket	The high pin count of the Pentium OverDrive processors often require more than 60 lbs of insertion force for Low Insertion Force (LIF) sockets. A Zero Insertion Force (ZIF) socket insures that the chip insertion force does not damage the PC Board. If the ZIF socket has a handle, be sure to allow enough clearance for the socket handle. If a LIF socket is used, additional PC board support is recommended.
"Plug and Play"	Jumper or switch changes should not be needed to electrically configure the system for the Pentium OverDrive processor.
Thorough Documentation	Describe the Pentium OverDrive processor's installation procedure in the PC's User's Manual.

APPENDIX B

Pentium® OverDrive® Processor with MMX™ Technology ZIF SOCKET VENDORS

The following list provides examples of sockets which can be used for Pentium processor-based systems.

NOTE

This is not a comprehensive list, Intel has not tested all of the Vendor's sockets listed below and cannot guarantee that these will meet every PC manufacturer's specific requirement.

	Socket No.	Style	Drawing No.	Part No.
AMP	Socket 5	SLAZ, OC, T	C-916513	916513
(800) 522-6752	Socket 5	SLAZ, OC, T	C-916560	916560
	Socket 5	SLAZ, OC, T	C-916655	916655
	Socket 5	SLAZ, OC, T	C-916656	916656
	Socket 5	SLAZ, OC, T	C-916671	916671
	Socket 5	SLAZ, OC, T	C-916672	916672
	Socket 7	SLAZ, OC, T	C-916637	916637
	Socket 7	SLAZ, OC, T	C-916657	916657
	Socket 7	SLAZ, OC, T	C-916658	916658
Appros	Socket 5	SLAZ, OC, T	KEA391129	SLR-S19-320-LN2
(408) 567-1234	Socket 7	SLAZ, OC, T	KEA391130	SLR-S19-321-LN2
	Average plating thickness used for qualification testing: 11.2 micro inches gold.			
Augat	Socket 5	SLAZ, OC, T	MP-AX159BCD20	MP-AX159BCD203
(800) 999-7646	Socket 5	SLAZ, OC, T	MP-AX159BCD20A	MP-AX159BCD203A
	Socket 5	SLAZ, OC, T	MP-AX159BCD20B	MP-AX159BCD203B
	Socket 7	SLAZ, OC, T	MP-AX164BCD21X	MP-AX164BCD213
	Socket 7	SLAZ, OC, T	MP-AX164BCD21XA	MP-AX164BCD213A
	Socket 7	SLAZ, OC, T	MP-AX164BCD21XB	MP-AX164BCD213B
	Average plating thickness used for qualification testing sockets: 19 micro inches gold.			

	Socket No.	Style	Drawing No.	Part No.
Berg/Mckenzie	Socket 5	SLAZ, OC, T	SAL B 270086-000	ZIF 97050-4020
(510) 654-2700	Socket 5	SLAZ, OC, T	SAL B 270086-000	ZIF 97050-4120
	Socket 7	SLAZ, OC, T	SAL B 270088-000	ZIF 97054-4020
	Socket 7	SLAZ, OC, T	SAL B 270088-000	ZIF 97054-4120
	Average plating thickness used for qualification testing sockets: 35 micro inches gold			
Foxconn	Socket 5	SLAZ, OC, NT	309-0000-049	PZ32023-0120
(408) 749-1228	Socket 5	SLAZ, OC, T	309-0000-049	PZ32033-0120
	Socket 5	SLAZ, OC, T	309-0000-049	PZ32043-0120
	Socket 5	SLAZ, OC, T	309-0000-049	PZ32053-0120
	Socket 7	SLAZ, OC, T	309-0000-062	PZ32143-0120
	Socket 7	SLAZ, OC, T	309-0000-062	PZ32153-0120
	Average plating thickness used for qualification testing: 10.0 micro inches gold			
JAE	Socket 5	SLAZ, OC, T	SJ029842-E	PCPS-ZL320-A9
(714) 753-2628	Socket 7	SLAZ, OC, T	SJ029842-E	PCPS-ZL321-A9
	Average plating thickness used for qualification testing: Socket 5/7 3.7 micro inched gold Flash/31.4 microinches Palladium Nickel, Socket 8 4.5 micro inched gold Flash/34 micro inches Palladium Nickel.			
Producer	Socket 5	SLAZ, OC, T	PD104-3202	PD104-32025
886-2-202-3578	*Average plating thickness used for qualification testing: 5.7 micro inches gold.*			
Yamaichi	Socket 5	SLAZ, OC, T	KL-13790	NP210-320-0100-CC0
(800) 769-0797	Socket 5	SLAZ, OC, T	KL-13425	NP210-320-0100-CC1
	Socket 5	SLAZ, OC, T	KL-13518	NP210-320-0100-CC2
	Socket 5	SLAZ, OC, T	KL-13930	NP210-320-0100-CC3
	Socket 5	SLAZ, OC, T	KL-13625	NP210-320K13625(D)
	Socket 7	SLAZ, OC, T	KL-13823	NP210-321-0100-CC1
	Socket 7	SLAZ, OC, T	KL-13620	NP210-321-0100-CC2
	Socket 7	SLAZ, OC, T	KL-13938	NP210-321-0100-CC3
	Average plating thickness used for qualification testing: 6.1 micro inches gold.			