

MITSUBISHI MICROCOMPUTERS M35061-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

M35061-XXXSP/FP is CATV screen display control IC which can display 40 (horizontal) X 17 (vertical). It has built-in SYRAM which can be used with character ROM.

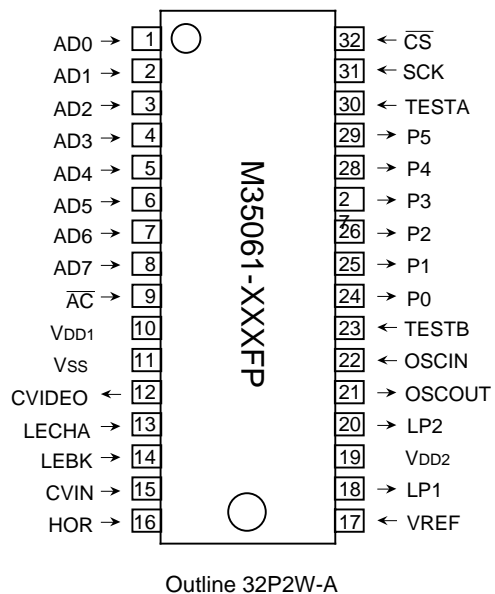
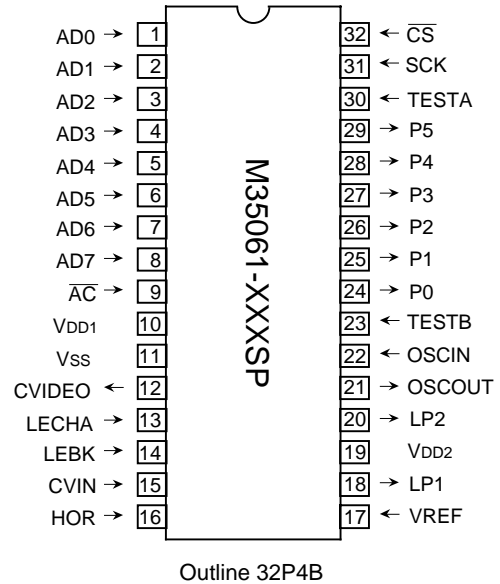
It uses a silicon gate CMOS process and M35061-XXXSP housed in a small 32-pin shrink DIP package, and M35061-XXXFP housed in a small 32-pin shrink SOP package. For M35061-002SP/FP that is a standard ROM version of M35061-XXXSP/FP, the character pattern is also mentioned.

FEATURES

- Screen composition 40 characters X 17 lines
(at scrolling 40 characters X 16 lines)
- Number of characters displayed 680 (Max.)
- Character composition 12 X 13 dot matrix
- Characters available character ROM 128 characters
SYRAM 7 characters
- Character sizes available horizontal 2 (once, twice)
vertical 2 (once, twice)
setting by every line
- Display locations available
Horizontal direction 486 locations
Vertical direction 235 locations
- Blinking character units
Cycle approximately 1 second, or approximately 0.5 seconds
(per screen)
Duty 25%, 50% or 75%
(per screen)
- Data input 8-bit parallel X 3
- Coloring Character coloring 8 colors choices per character
(Note)
Background coloring 8 colors choices per character
(Note)
Raster coloring 8 colors choices per screen
- Blanking Character size blanking
Border size blanking
Matrix-outline
Halftone blanking
Can be set by every line
- General-purpose output ports Combined port output 6
(switching to RGB output)
- RAM erase Display RAM erasing by every line
SYRAM erasing separately
- Scrolling Bit by bit smooth scroll implemented by software
- Composite synchronizing signal generation Built-in
(PAL, NTSC, M-PAL)
- Display oscillation circuit Built-in
- Synchronous separation circuit Built-in
- Synchronous correction circuit Built-in

Note: Superimpose coloring is available. (NTSC, PAL, M-PAL)

PIN CONFIGURATION (TOP VIEW)

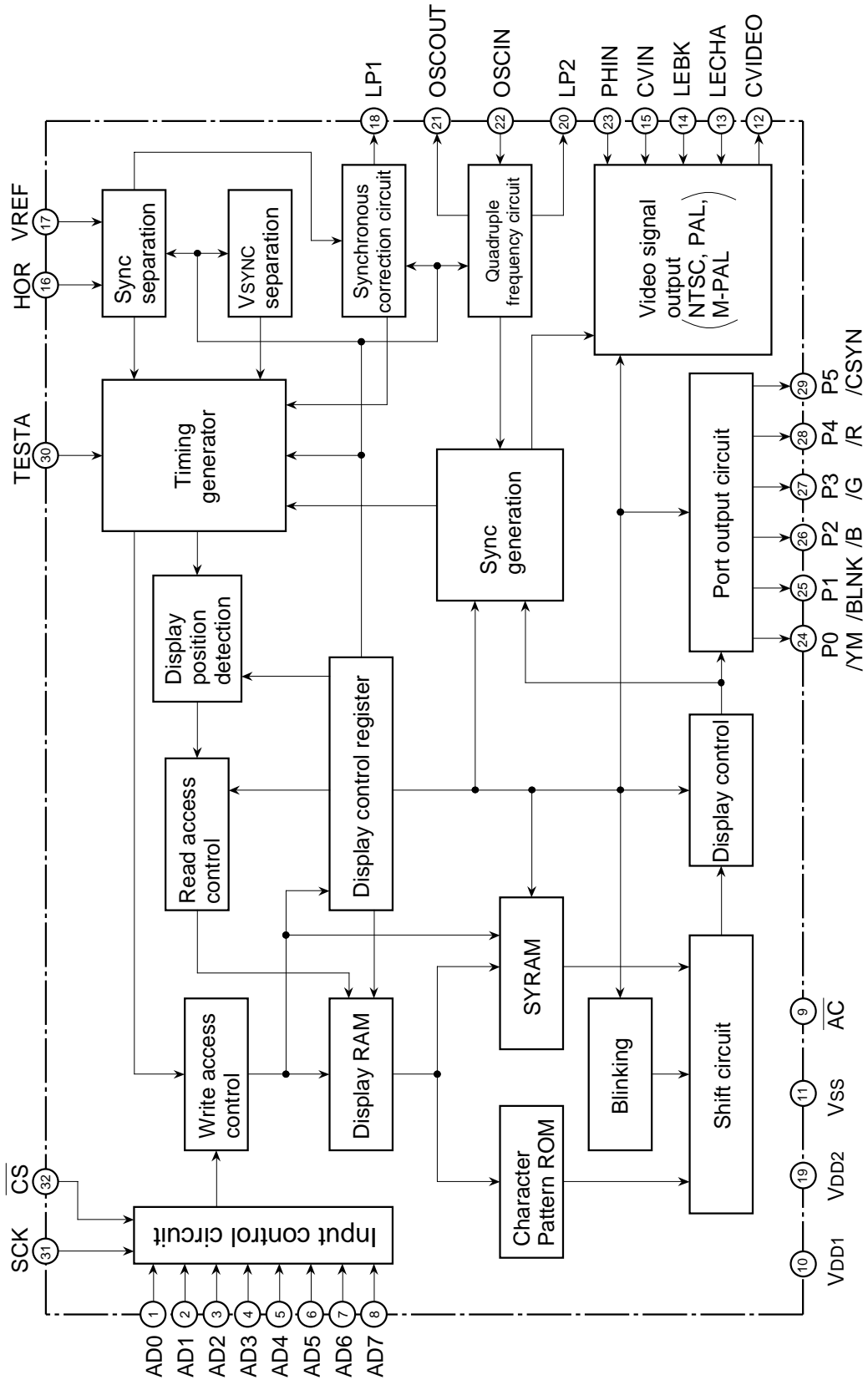


PIN DESCRIPTION

Symbol	Pin name	Input/Output	Function
AD0-AD7	Parallel data input	Input	These input pins determine address and data of display control register and display data memory by 8-bit parallel. Hysteresis input is required.
AC	Auto-clear input	Input	When this input pin transitions from "H" to "L", the device is reset. Built-in a pull-up resistor. Hysteresis input is required.
VDD1	Power pin	—	Digital power supply pin. This pin must be connected to +5 V.
VSS	Earthing pin	—	Ground pin. This pin must be connected to 0 V.
CVIDEO	Composite video signal output	Output	This pin outputs the composite video signal. The output signal is 2 V _{P-P} . In superimpose mode, this pin's signal consists of the OSD signal combined with the input composite signal CVIN.
LECHA	Character level input	Input	This input pin is used for controlling the "white" character color level of the OSD signal.
LEBK	Black level input	Input	This input pin is used for controlling the "black" character color level of the OSD signal.
CVIN	Composite video signal input	Input	This pin inputs the external composite video signal. In superimpose mode, this pin's signal consists of the OSD signal combined with the external composite video signal.
HOR	Synchronous signal input	Input	This pin inputs the external composite video signal. This pin inputs the clamped external video signal, sync-sep internal.
VREF	Slice level input	Input	This input pin is used to determine the slice voltage for extracting the sync signals from the video composite signal.
LP1	Filter output 1	Output	This is filter output pin 1.
VDD2	Power pin	—	Analog power supply pin. This pin must be connected to +5 V.
LP2	Filter output 2	Output	This is filter output pin 2.
OSCOU	fsc I/O pin for synchronous signal generating	Output	These are the sub-carrier oscillation (fsc) input pins for synchronous signal generating. NTSC (3.580 MHz), PAL (4.434 MHz), M-PAL (3.576 MHz) (Note).
OSCIN		Input	
PHIN	PHASE control input	Input	Control the phase changing by scanning line by PAL, M-PAL method.
P0	Port output	Output	This output pin can be configured to port P0 or YM output.
P1	Port output	Output	This output pin can be configured to port P1 or BLNK output.
P2	Port output	Output	This output pin can be configured to port P2 or B output.
P3	Port output	Output	This output pin can be configured to port P3 or G output.
P4	Port output	Output	This output pin can be configured to port P4 or R output.
P5	Port output	Output	This output pin can be configured to port P5 or CSYN output.
TESTA	Test input	Input	Factory test pin. The pin must be connected to GND.
SCK	Clock input for data input	Input	This pin is enabled when the CS pin is "L". Data input to pins AD0 to AD7 is latched at the rising edge of this signal. This pin is hysteresis input.
CS	Chip select input	Input	This is chip selection input pin. When this pin is "L", transmission is enabled. This pin is hysteresis input.

Note: fsc signal inputrefer to "note on when fsc signal input".

BLOCK DIAGRAM



SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MEMORY CONSTRUCTION

Address 000₁₆ to 2A7₁₆ are assigned to the display RAM, 2A8₁₆ to 2B0₁₆ are assigned to the display control registers and 300₁₆ to 36C₁₆ are assigned to SYRAM.

The internal circuit is reset and all display control registers (address 2A8₁₆ to 2B0₁₆) are set to "0". The memory constitution of display RAM and register is shown in Figure 1 and the memory constitution of SYRAM is shown in Figure 2.

Table 1 The memory constitution of display RAM and register

add-ress	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	
000 ₁₆	SB	SG	SR	0	0	0	SYC2	SYC1	SYC0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0	
?	SY color setting			0	0	0	SYRAM setting			Raster color setting			BLINK	Character color setting			0	Character setting							
2A7 ₁₆	SB	SG	SR	0	0	0	SYC2	SYC1	SYC0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0	
2A8 ₁₆	—	TEST 3	TEST 2	TEST 1	TEST 0	TEST 11	TEST 10	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	
2A9 ₁₆	—	—	—	BLINK 3	BLINK 2	BLINK 1	BLINK 0	HSZ 16	HSZ 15	HSZ 14	HSZ 13	HSZ 12	HSZ 11	HSZ 10	HSZ 9	HSZ 8	HSZ 7	HSZ 6	HSZ 5	HSZ 4	HSZ 3	HSZ 2	HSZ 1	HSZ 0	
2AA ₁₆	—	—	—	TEST 12	EQP	TEST 20	HIDE	VSZ 16	VSZ 15	VSZ 14	VSZ 13	VSZ 12	VSZ 11	VSZ 10	VSZ 9	VSZ 8	VSZ 7	VSZ 6	VSZ 5	VSZ 4	VSZ 3	VSZ 2	VSZ 1	VSZ 0	
2AB ₁₆	—	—	TEST 26	TEST 25	PHASE 2	PHASE 1	PHASE 0	DSP0 16	DSP0 15	DSP0 14	DSP0 13	DSP0 12	DSP0 11	DSP0 10	DSP0 09	DSP0 08	DSP0 07	DSP0 06	DSP0 05	DSP0 04	DSP0 03	DSP0 02	DSP0 01	DSP0 00	
2AC ₁₆	—	—	—	TEST 21	LINE B	LINE G	LINE R	DSP1 16	DSP1 15	DSP1 14	DSP1 13	DSP1 12	DSP1 11	DSP1 10	DSP1 09	DSP1 08	DSP1 07	DSP1 06	DSP1 05	DSP1 04	DSP1 03	DSP1 02	DSP1 01	DSP1 00	
2AD ₁₆	—	TEST 23	TEST 22	SERS 0	—	—	—	ERS 16	ERS 15	ERS 14	ERS 13	ERS 12	ERS 11	ERS 10	ERS 9	ERS 8	ERS 7	ERS 6	ERS 5	ERS 4	ERS 3	ERS 2	ERS 1	ERS 0	
2AE ₁₆	—	—	—	—	—	SEND 4	SEND 3	SEND 2	SEND 1	SEND 0	SST 4	SST 3	SST 2	SST 1	SST 0	SLIN 4	SLIN 3	SLIN 2	SLIN 1	SLIN 0	SBIT 3	SBIT 2	SBIT 1	SBIT 0	
2AF ₁₆	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ALL24	SRAND 2	SRAND 1	SRAND 0	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0	
2B0 ₁₆	—	TEST 19	TEST 18	TEST 17	TEST 24	LEVEL 2	LEVEL 1	LEVEL 0	INT NON	PAL NTSC	MPAL	PALH	TEST 16	TEST 15	SEPV1	SEPV0	BLK	—	DSP ONV	DSP ON	—	SEL COR	SCOR	EX	

TEST_n (n = number) is MITSUBISHI test memory. Set 0 to all bits.

Table 2 The memory constitution of SYRAM

add-ress	DA17 ~ DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	SYRAM code
300 ₁₆	0	SYEX	S00B	S00A	S009	S008	S007	S006	S005	S004	S003	S002	S001	S000	00 ₁₆
30C ₁₆		SYEX	S00B	S00A	S009	S008	S007	S006	S005	S004	S003	S002	S001	S000	
310 ₁₆	0	SYEX	S01B	S01A	S019	S018	S017	S016	S015	S014	S013	S012	S011	S010	01 ₁₆
31C ₁₆		SYEX	S01B	S01A	S019	S018	S017	S016	S015	S014	S013	S012	S011	S010	
?	:	:	?											?	
350 ₁₆	0	SYEX	S05B	S05A	S059	S058	S057	S056	S055	S054	S053	S052	S051	S050	05 ₁₆
35C ₁₆		SYEX	S05B	S05A	S059	S058	S057	S056	S055	S054	S053	S052	S051	S050	
360 ₁₆	0	SYEX	S06B	S06A	S069	S068	S067	S066	S065	S064	S063	S062	S061	S060	06 ₁₆
36C ₁₆		SYEX	S06B	S06A	S069	S068	S067	S066	S065	S064	S063	S062	S061	S060	

? : Name or value changes by definite ratio.
 : : The same name or value continues.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM.
The screen constitution is shown in Figure 1.

Line 0	000001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	011	012	013	014	015	016	017	018	019	01A	01B	01C	01D	01E	01F	020	021	022	023	024	025	026	027	
Line 1	028	029	02A	02B	02C	02D	02E	02F	030	031	032	033	034	035	036	037	038	039	03A	03B	03C	03D	03E	03F	040	041	042	043	044	045	046	047	048	049	04A	04B	04C	04D	04E	04F
	050	051	052	053	054	055	056	057	058	059	05A	05B	05C	05D	05E	05F	060	061	062	063	064	065	066	067	068	069	06A	06B	06C	06D	06E	06F	070	071	072	073	074	075	076	077
	078	079	07A	07B	07C	07D	07E	07F	080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F	090	091	092	093	094	095	096	097	098	099	09A	09B	09C	09D	09E	09F
	0A0	0A1	0A2	0A3	0A4	0A5	0A6	0A7	0A8	0A9	0AA	0AB	0AC	0AD	0AE	0AF	0B0	0B1	0B2	0B3	0B4	0B5	0B6	0B7	0B8	0B9	0BA	0BB	0BC	0BD	0BE	0BF	0C0	0C1	0C2	0C3	0C4	0C5	0C6	0C7
	0C8	0C9	0CA	0CB	0CC	0CD	0CE	0CF	0D0	0D1	0D2	0D3	0D4	0D5	0D6	0D7	0D8	0D9	0DA	0DB	0DC	0DD	0DE	0DF	0E0	0E1	0E2	0E3	0E4	0E5	0E6	0E7	0E8	0E9	0EA	0EB	0EC	0ED	0EE	0EF
	0F0	0F1	0F2	0F3	0F4	0F5	0F6	0F7	0F8	0F9	0FA	0FB	0FC	0FD	0FE	0FF	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117
	118	119	11A	11B	11C	11D	11E	11F	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F	160	161	162	163	164	165	166	167
	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F
	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7
	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF	200	201	202	203	204	205	206	207
	208	209	20A	20B	20C	20D	20E	20F	210	211	212	213	214	215	216	217	218	219	21A	21B	21C	21D	21E	21F	220	221	222	223	224	225	226	227	228	229	22A	22B	22C	22D	22E	22F
	230	231	232	233	234	235	236	237	238	239	23A	23B	23C	23D	23E	23F	240	241	242	243	244	245	246	247	248	249	24A	24B	24C	24D	24E	24F	250	251	252	253	254	255	256	257
	258	259	25A	25B	25C	25D	25E	25F	260	261	262	263	264	265	266	267	268	269	26A	26B	26C	26D	26E	26F	270	271	272	273	274	275	276	277	278	279	27A	27B	27C	27D	27E	27F
Line 16	280	281	282	283	284	285	286	287	288	289	28A	28B	28C	28D	28E	28F	290	291	292	293	294	295	296	297	298	299	29A	29B	29C	29D	29E	29F	2A0	2A1	2A2	2A3	2A4	2A5	2A6	2A7

The hexadecimal numbers in the boxes show the display RAM address

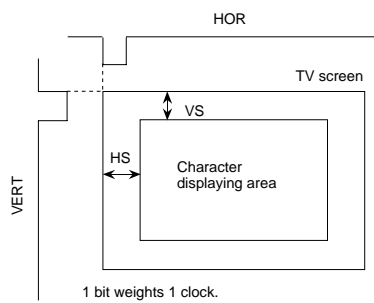
Fig. 1 Screen constitution

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

REGISTERS DESCRIPTION

(1) Address 2A8₁₆

DA	Register	Contents		Remarks
		Status	Function	
0	VP0	0	If VS is the vertical display start location, $VS = H \times \left(\sum_{n=0}^7 2^n VP_n \right)$ H: Cycle with the horizontal synchronizing pulse	The vertical start location is specified using the 8 bits from VP7 to VP0. VP7 to VP0 < 14 ₁₆ are not available.
		1		
1	VP1	0		
		1		
2	VP2	0		
		1		
3	VP3	0		
		1		
4	VP4	0		
		1		
5	VP5	0		
		1		
6	VP6	0		
		1		
7	VP7	0		
		1		
8	HP0	0	If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 19 ₁₆ are not available.
		1		
9	HP1	0		
		1		
A	HP2	0		
		1		
B	HP3	0		
		1		
C	HP4	0		
		1		
D	HP5	0		
		1		
E	HP6	0		
		1		
F	HP7	0		
		1		
10	HP8	0		
		1		
11	TEST10	0	Test mode (Must be cleared to 0.)	
		1		
12	TEST11	0		
		1		
13	TEST0	0		
		1		
14	TEST1	0		
		1		
15	TEST2	0		
		1		
16	TEST3	0		
		1		
17	—	0	Must be cleared to 0.	
		1		



Note: The mark ○ around the status value means the reset status by the "L" level is input to AC pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Address 2A916

DA	Register	Contents		Remarks									
		Status	Function										
0	HSZ0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>HSZx</td> <td>Horizontal direction character size</td> </tr> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	HSZx	Horizontal direction character size	0	1T/dot	1	2T/dot	Set to line 0 of display RAM			
		HSZx		Horizontal direction character size									
0	1T/dot												
1	2T/dot												
1													
1	HSZ1	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 1 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
2	HSZ2	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 2 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
3	HSZ3	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 3 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
4	HSZ4	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 4 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
5	HSZ5	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 5 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
6	HSZ6	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 6 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
7	HSZ7	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 7 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
8	HSZ8	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 8 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
9	HSZ9	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 9 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
A	HSZ10	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 10 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
B	HSZ11	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 11 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
C	HSZ12	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 12 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
D	HSZ13	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 13 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
E	HSZ14	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 14 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
F	HSZ15	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 15 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
10	HSZ16	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table>	0	1T/dot	1	2T/dot	Set to line 16 of display RAM					
		0		1T/dot									
1	2T/dot												
1													
11	BLINK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>BLINK1 \ BLINK0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Blinking OFF</td> <td>Duty 25%</td> </tr> <tr> <td>1</td> <td>Duty 50%</td> <td>Duty 75%</td> </tr> </table>	BLINK1 \ BLINK0	0	1	0	Blinking OFF	Duty 25%	1	Duty 50%	Duty 75%	Blinking duty ratio can be altered.
		BLINK1 \ BLINK0		0	1								
0	Blinking OFF	Duty 25%											
1	Duty 50%	Duty 75%											
1													
12	BLINK1	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>BLINK1 \ BLINK0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Blinking OFF</td> <td>Duty 25%</td> </tr> <tr> <td>1</td> <td>Duty 50%</td> <td>Duty 75%</td> </tr> </table>	BLINK1 \ BLINK0	0	1	0	Blinking OFF	Duty 25%	1	Duty 50%	Duty 75%	Blinking duty ratio can be altered.
		BLINK1 \ BLINK0		0	1								
0	Blinking OFF	Duty 25%											
1	Duty 50%	Duty 75%											
1													
13	BLINK2	0	Cycle approximately 1 second.	Blinking cycle can be altered.									
		1	Cycle approximately 0.5 second.										
14	BLINK3	0	Normal blinking	Character is in flashing state.									
		1	Normal character, reversed character alternation display.	Character is always displayed (normal character, reversed character).									
15	—	0	Must be cleared to 0.										
		1											
16	—	0	Must be cleared to 0.										
		1											
17	—	0	Must be cleared to 0.										
		1											

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Address 2AA16

DA	Register	Contents		Remarks						
		Status	Function							
0	VSZ0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">VSZx</td> <td style="text-align: center;">Vertical direction character size</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1H/dot</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">2H/dot</td> </tr> </table>	VSZx	Vertical direction character size	0	1H/dot	1	2H/dot	Set to line 0 of display RAM
		VSZx		Vertical direction character size						
0	1H/dot									
1	2H/dot									
1	Set to line 1 of display RAM									
1	VSZ1	0		<p style="text-align: center;">H: Horizontal synchronous pulse</p>	Set to line 2 of display RAM					
		1	Set to line 3 of display RAM							
2	VSZ2	0	<p style="text-align: center;">H: Horizontal synchronous pulse</p>		Set to line 4 of display RAM					
		1			Set to line 5 of display RAM					
3	VSZ3	0			<p style="text-align: center;">H: Horizontal synchronous pulse</p>	Set to line 6 of display RAM				
		1				Set to line 7 of display RAM				
4	VSZ4	0		<p style="text-align: center;">H: Horizontal synchronous pulse</p>		Set to line 8 of display RAM				
		1				Set to line 9 of display RAM				
5	VSZ5	0	<p style="text-align: center;">H: Horizontal synchronous pulse</p>			Set to line 10 of display RAM				
		1				Set to line 11 of display RAM				
6	VSZ6	0			<p style="text-align: center;">H: Horizontal synchronous pulse</p>	Set to line 12 of display RAM				
		1				Set to line 13 of display RAM				
7	VSZ7	0		<p style="text-align: center;">H: Horizontal synchronous pulse</p>		Set to line 14 of display RAM				
		1				Set to line 15 of display RAM				
8	VSZ8	0	<p style="text-align: center;">H: Horizontal synchronous pulse</p>			Set to line 16 of display RAM				
		1								
9	VSZ9	0			<p style="text-align: center;">H: Horizontal synchronous pulse</p>					
		1								
A	VSZ10	0		<p style="text-align: center;">H: Horizontal synchronous pulse</p>						
		1								
B	VSZ11	0	<p style="text-align: center;">H: Horizontal synchronous pulse</p>							
		1								
C	VSZ12	0			<p style="text-align: center;">H: Horizontal synchronous pulse</p>					
		1								
D	VSZ13	0		<p style="text-align: center;">H: Horizontal synchronous pulse</p>						
		1								
E	VSZ14	0	<p style="text-align: center;">H: Horizontal synchronous pulse</p>							
		1								
F	VSZ15	0			<p style="text-align: center;">H: Horizontal synchronous pulse</p>					
		1								
10	VSZ16	0		<p style="text-align: center;">H: Horizontal synchronous pulse</p>						
		1								
11	HIDE	0	SYRAM writing over			Decided by register LINER, G and B or DAC bit (SYEX) of SYRAM.				
		1	SYRAM writing over or character erasing							
12	TEST20	0	Test mode (Must be cleared to 0.)							
		1								
13	EQP	0	It does not include equivalent pulse.							
		1	It includes equivalent pulse.							
14	TEST12	0	Test mode (Must be cleared to 0.)							
		1								
15	—	0	Must be cleared to 0.							
		1								
16	—	0	Must be cleared to 0.							
		1								
17	—	0	Must be cleared to 0.							
		1								

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address 2AB16

DA	Register	Status	Contents			Remarks																																																		
			Function																																																					
0	DSP0 00	0	DSP0XX	0	1	Set to line 0 of display RAM																																																		
		1																																																						
1	DSP0 01	0	DSP1XX	Character	Border	Set to line 1 of display RAM																																																		
		1																																																						
2	DSP0 02	0	1	Matrix-outline	Halftone (Note)	Set to line 2 of display RAM																																																		
		1																																																						
3	DSP0 03	0	Set by combination of DSP0xx (address 2AB16) and DSP1xx (address 2AC16). At internal synchronous mode (EX = 1), display monitor signal area is all blanking signal (BLNK output) area. Note: For half-tone display, it is necessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200 resistor in series. However, the half-tone display is possible only with superimposed displays.			Set to line 3 of display RAM																																																		
1	1	Set to line 4 of display RAM																																																						
4	DSP0 04	0				Set to line 5 of display RAM																																																		
1	1	Set to line 6 of display RAM																																																						
5	DSP0 05	0				Set to line 7 of display RAM																																																		
1	1	Set to line 8 of display RAM																																																						
6	DSP0 06	0				Set to line 9 of display RAM																																																		
1	1	Set to line 10 of display RAM																																																						
7	DSP0 07	0				Set to line 11 of display RAM																																																		
1	1	Set to line 12 of display RAM																																																						
8	DSP0 08	0				Set to line 13 of display RAM																																																		
1	1	Set to line 14 of display RAM																																																						
9	DSP0 09	0				Set to line 15 of display RAM																																																		
1	1	Set to line 16 of display RAM																																																						
A	DSP0 10	0				<table border="1"> <thead> <tr> <th rowspan="2">PHASE 2</th> <th rowspan="2">PHASE 1</th> <th rowspan="2">PHASE 0</th> <th colspan="2">Color</th> </tr> <tr> <th>SELCOR=0</th> <th>SELCOR=1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Black</td> <td>Black</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Red</td> <td>Red-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Green</td> <td>Green-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Yellow</td> <td>Yellow</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Blue</td> <td>Gray</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Magenta</td> <td>Yellow-2</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Cyan</td> <td>Cyan</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>White</td> <td>White</td> </tr> </tbody> </table>			PHASE 2	PHASE 1	PHASE 0	Color		SELCOR=0	SELCOR=1	0	0	0	Black	Black	0	0	1	Red	Red-2	0	1	0	Green	Green-2	0	1	1	Yellow	Yellow	1	0	0	Blue	Gray	1	0	1	Magenta	Yellow-2	1	1	0	Cyan	Cyan	1	1	1	White	White	Refer Fig 3, 4 about phase angle.
PHASE 2	PHASE 1	PHASE 0										Color																																												
			SELCOR=0	SELCOR=1																																																				
0	0	0	Black	Black																																																				
0	0	1	Red	Red-2																																																				
0	1	0	Green	Green-2																																																				
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1	0	0	Blue	Gray																																																				
1	0	1	Magenta	Yellow-2																																																				
1	1	0	Cyan	Cyan																																																				
1	1	1	White	White																																																				
B	DSP0 11	0	Test mode (Must be cleared to 0.)																																																					
1	1																																																							
C	DSP0 12	0																																																						
1	1																																																							
D	DSP0 13	0																																																						
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10	DSP0 16	0				Must be cleared to 0.																																																		
1	1																																																							
11	PHASE 0	0																																																						
1	1																																																							
12	PHASE 1	0																																																						
1	1																																																							
13	PHASE 2	0																																																						
1	1																																																							
14	TEST25	0																																																						
1	1																																																							
15	TEST26	0																																																						
1	1																																																							
16	—	0																																																						
1	1																																																							
17	—	0																																																						
1	1																																																							

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address 2AC16

DA	Register	Status	Contents			Remarks																																																		
			Function																																																					
0	DSP1 00	0	DSP0XX	0	1	Set to line 0 of display RAM																																																		
		1																																																						
1	DSP1 01	0	DSP1XX	Character	Border	Set to line 1 of display RAM																																																		
		1																																																						
2	DSP1 02	0	1	Matrix-outline	Halftone (Note)	Set to line 2 of display RAM																																																		
		1																																																						
3	DSP1 03	0	Set by combination of DSP0XX (address 2AB16) and DSP1XX (address 2AC16). At internal synchronous mode (EX = 1), display monitor signal area is all blanking signal (BLNK output) area. Note: For half-tone display, it is necessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200 resistor in series. However, the half-tone display is possible only with superimposed displays.			Set to line 3 of display RAM																																																		
1	1	Set to line 4 of display RAM																																																						
4	DSP1 04	0				Set to line 5 of display RAM																																																		
1	1	Set to line 6 of display RAM																																																						
5	DSP1 05	0				Set to line 7 of display RAM																																																		
1	1	Set to line 8 of display RAM																																																						
6	DSP1 06	0				Set to line 9 of display RAM																																																		
1	1	Set to line 10 of display RAM																																																						
7	DSP1 07	0				Set to line 11 of display RAM																																																		
1	1	Set to line 12 of display RAM																																																						
8	DSP1 08	0				Set to line 13 of display RAM																																																		
1	1	Set to line 14 of display RAM																																																						
9	DSP1 09	0				Set to line 15 of display RAM																																																		
1	1	Set to line 16 of display RAM																																																						
A	DSP1 10	0				<table border="1"> <thead> <tr> <th rowspan="2">LINE B</th> <th rowspan="2">LINE G</th> <th rowspan="2">LINE R</th> <th colspan="2">Color</th> </tr> <tr> <th>SELCOR=0</th> <th>SELCOR=1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Black</td> <td>Black</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Red</td> <td>Red-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Green</td> <td>Green-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Yellow</td> <td>Yellow</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Blue</td> <td>Gray</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Magenta</td> <td>Yellow-2</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Cyan</td> <td>Cyan</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>White</td> <td>White</td> </tr> </tbody> </table>			LINE B	LINE G	LINE R	Color		SELCOR=0	SELCOR=1	0	0	0	Black	Black	0	0	1	Red	Red-2	0	1	0	Green	Green-2	0	1	1	Yellow	Yellow	1	0	0	Blue	Gray	1	0	1	Magenta	Yellow-2	1	1	0	Cyan	Cyan	1	1	1	White	White	Set to line 10 of display RAM
LINE B	LINE G	LINE R										Color																																												
			SELCOR=0	SELCOR=1																																																				
0	0	0	Black	Black																																																				
0	0	1	Red	Red-2																																																				
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1	1	1	White	White																																																				
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B	DSP1 11	0	Set to line 12 of display RAM																																																					
1	1	Set to line 13 of display RAM																																																						
C	DSP1 12	0	Set to line 14 of display RAM																																																					
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10	DSP1 16	0																																																						
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11	LINER	0	<table border="1"> <thead> <tr> <th rowspan="2">LINE B</th> <th rowspan="2">LINE G</th> <th rowspan="2">LINE R</th> <th colspan="2">Color</th> </tr> <tr> <th>SELCOR=0</th> <th>SELCOR=1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Black</td> <td>Black</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Red</td> <td>Red-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Green</td> <td>Green-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Yellow</td> <td>Yellow</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Blue</td> <td>Gray</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Magenta</td> <td>Yellow-2</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Cyan</td> <td>Cyan</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>White</td> <td>White</td> </tr> </tbody> </table>			LINE B	LINE G	LINE R	Color		SELCOR=0	SELCOR=1	0	0	0	Black	Black	0	0	1	Red	Red-2	0	1	0	Green	Green-2	0	1	1	Yellow	Yellow	1	0	0	Blue	Gray	1	0	1	Magenta	Yellow-2	1	1	0	Cyan	Cyan	1	1	1	White	White	SYRAM color setting. Color is decided by DAC bit (SYEX) of SYRAM or HIDE register.			
		LINE B							LINE G	LINE R	Color																																													
SELCOR=0	SELCOR=1																																																							
0	0	0				Black	Black																																																	
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14	TEST21	0	Test mode (Must be cleared to 0.)																																																					
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		1																																																						

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address 2AD₁₆

DA	Register	Contents		Remarks							
		Status	Function								
0	ERS0	0	Erase display RAM	Set to line 0 of display RAM							
		1									
1	ERS1	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>ERSx</td> <td>RAM erase</td> </tr> <tr> <td>0</td> <td>do not erase</td> </tr> <tr> <td>1</td> <td>do erase</td> </tr> </table>	ERSx	RAM erase	0	do not erase	1	do erase	Set to line 1 of display RAM	
		ERSx		RAM erase							
0	do not erase										
1	do erase										
1											
2	ERS2	0	Do not set "1" more than 2 bits at the same time. The setting is not retained even if the bit is set to "1". Therefore, it is not necessary to cancel it.	Set to line 2 of display RAM							
		1									
3	ERS3	0			Set to line 3 of display RAM						
		1									
4	ERS4	0				Set to line 4 of display RAM					
		1									
5	ERS5	0					Set to line 5 of display RAM				
		1									
6	ERS6	0						Set to line 6 of display RAM			
		1									
7	ERS7	0							Set to line 7 of display RAM		
		1									
8	ERS8	0								Set to line 8 of display RAM	
		1									
9	ERS9	0									Set to line 9 of display RAM
		1									
A	ERS10	0									
		1									
B	ERS11	0									
		1									
C	ERS12	0									
		1									
D	ERS13	0									
		1									
E	ERS14	0									
		1									
F	ERS15	0									
		1									
10	ERS16	0									
		1									
11	-	0							Must be cleared to 0.		
		1									
12	-	0								Must be cleared to 0.	
		1									
13	-	0									Must be cleared to 0.
		1									
14	SERS0	0	do not erase SYRAM						Set to SYRAM code 00 ₁₆ ~ 06 ₁₆ (Note)		
		1	erase SYRAM								
15	TEST22	0	Test mode (Must be cleared to 0.)								
		1									
16	TEST23	0									
		1									
17	—	0	Must be cleared to 0.								
		1									

Note: The setting is not retained even if the bit is set to "1". Therefore, it is not necessary to cancel it.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address 2AE16

DA	Register	Contents		Remarks		
		Status	Function			
0	SBIT0	0	Set display start bit of scroll block: $SA = \sum_{n=0}^3 2^n (SBIT_n)$	Setting valid SA = 0 ~ 12 invalid SA = 13 ~ 15		
		1				
1	SBIT1	0				
		1				
2	SBIT2	0				
		1				
3	SBIT3	0				
		1				
4	SLIN0	0			Set display start line of scroll block: $SB = \sum_{n=0}^4 2^n (SLIN_n)$	Setting valid SB = 0 ~ 16 invalid SB = 17 ~ 31
		1				
5	SLIN1	0				
		1				
6	SLIN2	0				
		1				
7	SLIN3	0				
		1				
8	SLIN4	0				
		1				
9	SST0	0	Set start line of scroll block (last line number of the fixed block 1): $SC = \sum_{n=0}^4 2^n (SST_n)$	Setting valid SC = 0 ~ 15 invalid SC = 16 ~ 31		
		1				
A	SST1	0				
		1				
B	SST2	0				
		1				
C	SST3	0				
		1				
D	SST4	0				
		1				
E	SEND0	0			Set start line of fixed block 2 (last line number of the scroll block): $SD = \sum_{n=0}^4 2^n (SEND_n)$	When the scrolling on setting valid SD = 2 ~ 17 invalid SD = 18 ~ 31 When the scrolling off set SD = 0 SD > SC + 2
		1				
F	SEND1	0				
		1				
10	SEND2	0				
		1				
11	SEND3	0				
		1				
12	SEND4	0				
		1				
13	—	0	Must be cleared to 0.			
		1				
14	—	0				
		1				
15	—	0				
		1				
16	—	0				
		1				
17	—	0				
		1				

Note: When the scrolling on, set the ratio which will be $SC < SB < SD$.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

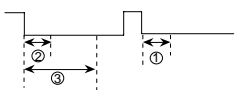
(8) Address 2AF16

DA	Register	Contents				Remarks		
		Status	Function					
0	PTC0	0	Port P0 output			Select P0 pin		
		1	YM output					
1	PTC1	0	Port P1 output			Select P1 pin		
		1	BLNK output					
2	PTC2	0	Port P2 output			Select P2 pin		
		1	B output					
3	PTC3	0	Port P3 output			Select P3 pin		
		1	G output					
4	PTC4	0	Port P4 output			Select P4 pin		
		1	R output					
5	PTC5	0	Port P5 output			Select P5 pin		
		1	CSYN output					
6	PTD0	0	When port output: 0 output, when YM output: negative polarity.			Select data of P0 pin		
		1	When port output: 1 output, when YM output: polarity.					
7	PTD1	0	When port output: 0 output, when BLNK output: negative polarity.			Select data of P1 pin		
		1	When port output: 1 output, when BLNK output: polarity.					
8	PTD2	0	When port output: 0 output, when B output: negative polarity.			Select data of P2 pin		
		1	When port output: 1 output, when B output: polarity.					
9	PTD3	0	When port output: 0 output, when G output: negative polarity.			Select data of P3 pin		
		1	When port output: 1 output, when G output: polarity.					
A	PTD4	0	When port output: 0 output, when R output: negative polarity.			Select data of P4 pin		
		1	When port output: 1 output, when R output: polarity.					
B	PTD5	0	When port output: 0 output, when CSYN output: negative polarity.			Select data of P5 pin		
		1	When port output: 1 output, when CSYN output: polarity.					
C	SRAND0	0	SRAND SRAND SRAND2				Condition of border display is changeable.	
		1	1	0	0	1		
D	SRAND1	0	0	0	Complete border = 1 dot	Right and dot border = 1 dot		
		1	0	1	Complete border = 2 dot	Right and dot border = 2 dot		
E	SRAND2	0	1	0	Complete border = 3 dot	Right and dot border = 3 dot		
		1	1	1	Complete border = 4 dot	Right and dot border = 4 dot		
F	ALL24	0	Blanking with all 40 characters in matrix-outline mode					
		1	Horizontal display period fully blanked with all characters in matrix-outline size.					
10	PC0	0	Display frequency f_T control $f_T = f_H \times \left\{ \sum_{n=0}^7 (2^n PC_n) + 512 \right\}$					PC7 ~ PC0 < 3616, PC7 ~ PC0 > C616 is not available.
		1						
11	PC1	0						
		1						
12	PC2	0						
		1						
13	PC3	0						
		1						
14	PC4	0						
		1						
15	PC5	0						
		1						
16	PC6	0						
		1						
17	PC7	0						
		1						

Note: At EX (address 2B016) = "0" (external synchronous), setting "1" of ALL24 register is not available.
Refer Fig. 2 about PTC0 ~ 5, PTD0 ~ 5.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 2B016

DA	Register	Contents		Remarks															
		Status	Function																
0	EX	0	External synchronization	(Note 1)															
		1	Internal synchronization																
1	SCOR	0	Superimpose black and white display	Valid at only register "EX"=0 (at external synchronous) (Note 2, 3 and 4)															
		1	Superimpose coloring display																
2	SELCOR	0	Normal	Refer to Table 3, 4, 7 and 8.															
		1	Mode of expansion																
3	—	0	Must be cleared to 0.																
		1																	
4	DSPON	0	Digital output display OFF																
		1	Digital output display ON																
5	DSPONV	0	Composite video output display OFF																
		1	Composite video output display ON																
6	—	0	Must be cleared to 0.																
		1																	
7	BLK	0	Matrix outline	Only at register "DSP1xx" = 1 (xx = 00 ~ 16) is valid.															
		1	Matrix outline + border (border color is black)																
8	SEPV0	0	<table border="1"> <thead> <tr> <th>SEPV1</th> <th>SEPV0</th> <th>Composite Sync Separation Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Separation is performed during 1 in vertical blanking period</td> </tr> <tr> <td>0</td> <td>1</td> <td>Separation is performed during 2 in vertical blanking period</td> </tr> <tr> <td>1</td> <td>0</td> <td>Separation is performed during 3 in vertical blanking period</td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting disabled</td> </tr> </tbody> </table>	SEPV1	SEPV0	Composite Sync Separation Function	0	0	Separation is performed during 1 in vertical blanking period	0	1	Separation is performed during 2 in vertical blanking period	1	0	Separation is performed during 3 in vertical blanking period	1	1	Setting disabled	Method of sync separation from composite video. 
		SEPV1		SEPV0	Composite Sync Separation Function														
0	0	Separation is performed during 1 in vertical blanking period																	
0	1	Separation is performed during 2 in vertical blanking period																	
1	0	Separation is performed during 3 in vertical blanking period																	
1	1	Setting disabled																	
1																			
9	SEPV1	0		Case 1 condition: vertical sync must repeat 2X within 2 or 3; indicates this area.															
		1																	
A	TEST15	0	Test mode (Must be cleared to 0.)																
		1																	
B	TEST16	0																	
		1																	
C	PALH	0	Interlace/noninterlace normal mode	Valid at only PAL and MPAL mode.															
		1	Interlace/noninterlace expansion mode																
D	MPAL	0	<table border="1"> <thead> <tr> <th>PAL/NTSC</th> <th>MPAL</th> <th>Format</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>NTSC</td> </tr> <tr> <td>0</td> <td>1</td> <td>M-PAL</td> </tr> <tr> <td>1</td> <td>0</td> <td>PAL</td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting disabled</td> </tr> </tbody> </table>	PAL/NTSC	MPAL	Format	0	0	NTSC	0	1	M-PAL	1	0	PAL	1	1	Setting disabled	
		PAL/NTSC		MPAL	Format														
0	0	NTSC																	
0	1	M-PAL																	
1	0	PAL																	
1	1	Setting disabled																	
1																			
E	PAL/NTSC	0																	
		1																	
F	INT/NON	0	Interlace																
		1	Noninterlace																

- Notes** 1: For internal synchronization, shut out (mute) the external video signal input, outside the IC. This avoids external video signal leaks inside the IC.
 2: For superimposed color displays, input an fsc signal which is synchronized with the color burst of the composite video signal (input to the CVIN pin) to the OSCIN pin.
 3: When EX (address 2B016) = "1" (internal synchronization), set the SCOR register to "0".
 4: When using a crystal oscillator (for the fsc input) between the OSCIN and OSCOUT pin, set the SCOR register to "0".

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 2B016 (cont.)

DA	Register	Contents		Remarks								
		Status	Function									
10	LEVEL0	0	Composite video generation is off.	Refer to Table 5 and 6.								
		1	Composite video generation is on.									
11	LEVEL1	0	Display clock is on (oscillating).									
		1	Display clock is off (not oscillating).									
12	LEVEL2	0	Sync separation is disabled.									
		1	Sync separation is enabled.									
13	TEST24	0	Test mode (Must be cleared to 0.)									
		1										
14	TEST17	0			Test mode (Must be cleared to 0.)							
		1										
15	TEST18	0					Test mode (Must be cleared to 0.)					
		1										
16	TEST19	0							Test mode (Must be cleared to 0.)			
		1										
17	—	0									Must be cleared to 0.	
		1										

REGISTER CONSTRUCTION COMPOSITION

Table 3 Color and phase of NTSC, PAL (SELCOR = 0)

PHASE2 LINEB	PHASE1 LINEG	PHASE0 LINER	Phase (rad)		Color
			NTSC	PAL	
0	0	0	—	—	Black
0	0	1	7 /16	± 7 /16	Red
0	1	0	27 /16	∓ 5 /16	Green
0	1	1	/16	± /16	Yellow
1	0	0	17 /16	∓ 15 /16	Blue
1	0	1	11 /16	± 11 /16	Magenta
1	1	0	23 /16	∓ 9 /16	Cyan
1	1	1	—	—	White

Table 4 Color and phase of NTSC, PAL (SELCOR = 1)

PHASE2 LINEB	PHASE1 LINEG	PHASE0 LINER	Phase (rad)		Color
			NTSC	PAL	
0	0	0	—	—	Black
0	0	1	7 /16	± 7 /16	Red-2
0	1	0	27 /16	∓ 5 /16	Green-2
0	1	1	/16	± /16	Yellow
1	0	0	—	—	Gray
1	0	1	/16	± /16	Yellow-2
1	1	0	23 /16	∓ 9 /16	Cyan
1	1	1	—	—	White

Table 7 Video signal level (SELCOR = 0)

Color name	Phase (rad)		Luminance level (V)			Chroma amplitude (vs. color burst)		
	NTSC	PAL	Min.	Typ.	Max.	Min.	Typ.	Max.
Sync	—	—	1.3	1.5	1.7	—	—	—
Pedestal	—	—	1.9	2.1	2.3	—	—	—
Color Burst	0	±4 /16	1.9	2.1	2.3	—	1.0	—
Black	—	—	2.1	2.3	2.5	—	—	—
Red	7 /16 ± 2 /16	± 7 /16 ± 2 /16	2.3	2.5	2.7	1.5	3.0	4.5
Green	27 /16 ± 2 /16	∓ 5 /16 ± 2 /16	2.7	2.9	3.1	1.4	2.8	4.2
Yellow	/16 ± 2 /16	± /16 ± 2 /16	3.1	3.3	3.5	1.0	2.0	3.0
Blue	17 /16 ± 2 /16	∓ 15 /16 ± 2 /16	2.0	2.2	2.4	1.0	2.0	3.0
Mazenta	11 /16 ± 2 /16	± 11 /16 ± 2 /16	2.5	2.7	2.9	1.4	2.8	4.2
Cyan	23 /16 ± 2 /16	∓ 9 /16 ± 2 /16	2.9	3.1	3.3	1.5	3.0	4.5
White	—	—	3.1	3.3	3.5	—	—	—

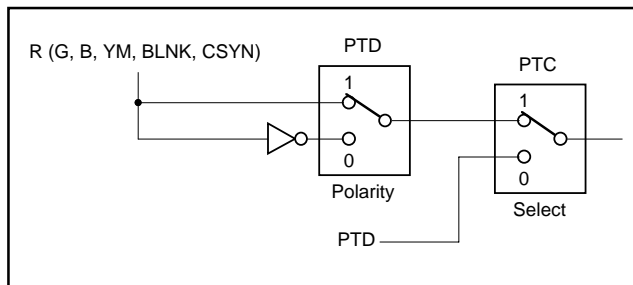


Fig. 2 Switching port output with R, G and B output

Table 5 Setting condition at LEVEL 0, 1 and 2

	At display clock operates	At display clock stops
LEVEL1	0	1
DSPON	1	0
DSPONV	1	0
CS pin	L	H

No character display at display clock

Table 6 Setting condition at LEVEL 0, 1 and 2 (at operation)

	Operation state	Stop state
LEVEL0	1	0
LEVEL1	0	1
LEVEL2	1	0

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Table 8 Video signal level (SELCOR = 1)

Color name	Phase (rad)		Luminance level (V)			Chroma amplitude (vs. color burst)		
	NTSC	PAL	Min.	Typ.	Max.	Min.	Typ.	Max.
Sync	—	—	1.3	1.5	1.7	—	—	—
Pedestal	—	—	1.9	2.1	2.3	—	—	—
Color Burst	0	$\pm 4 / 16$	1.9	2.1	2.3	—	1.0	—
Black	—	—	2.1	2.3	2.5	—	—	—
Red-2	$7 / 16 \pm 2 / 16$	$\pm 7 / 16 \pm 2 / 16$	2.6	2.8	3.0	1.5	2.0	3.0
Green-2	$27 / 16 \pm 2 / 16$	$\mp 5 / 16 \pm 2 / 16$	3.1	3.3	3.5	0.5	1.0	1.5
Yellow	$/ 16 \pm 2 / 16$	$\pm / 16 \pm 2 / 16$	3.1	3.3	3.5	1.0	2.0	3.0
Gray	—	—	2.8	3.0	3.2	—	—	—
Yellow-2	$/ 16 \pm 2 / 16$	$\pm / 16 \pm 2 / 16$	3.2	3.4	3.6	0.4	0.8	1.2
Cyan	$23 / 16 \pm 2 / 16$	$\mp 9 / 16 \pm 2 / 16$	2.9	3.1	3.3	1.5	3.0	4.5
White	—	—	3.1	3.3	3.5	—	—	—

DISPLAY FORMS
1. Blanking mode

Display forms are shown in Table 9, display forms at each display mode are shown in Fig. 3.

Table 9 Display forms

Display mode	DSP1 xx (Address 2AC16)	DSP0 xx (Address 2AB16)	BLNK output
Character	0	0	Character size
Border	0	1	Border size
Matrix-outline	1	0	All blanking
Halftone	1	1	Blanking OFF

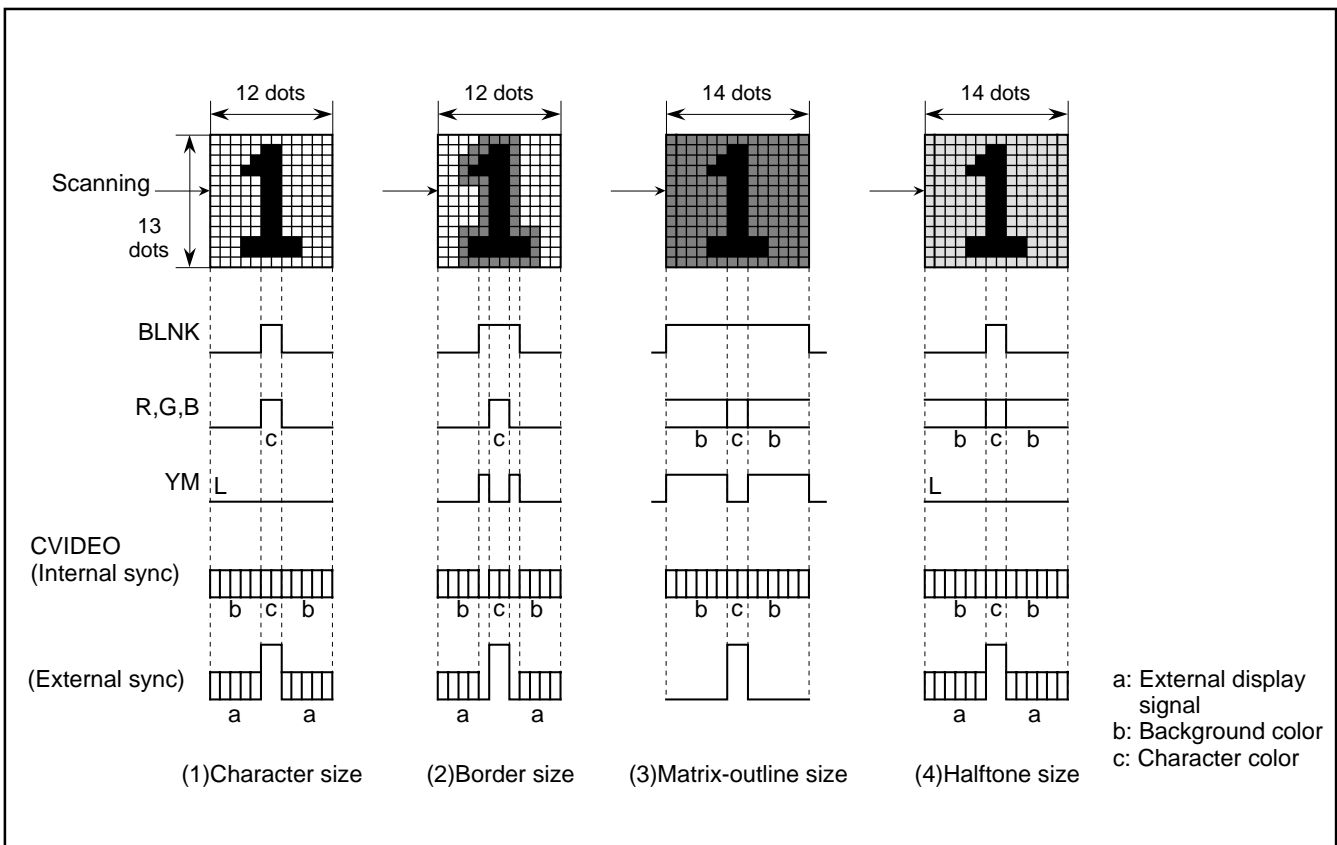


Fig. 3 Display forms at each display mode

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

For matrix and halftone, a character's number of dots in the horizontal direction increases to 14.

Figure 4 shows a display example for a case where adjacent characters have different background colors and for character code FF₁₆.

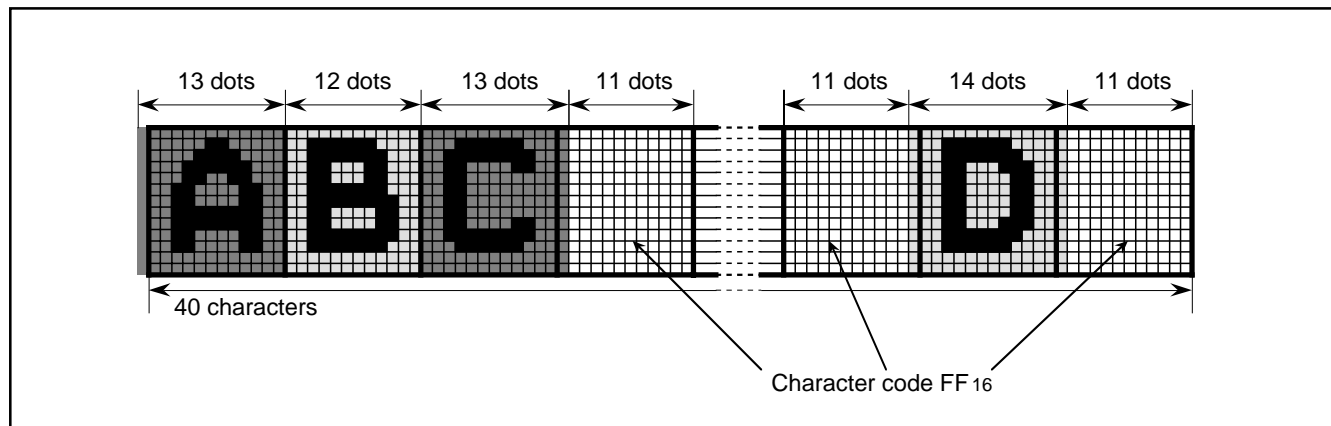


Fig. 4 Number of dots in the horizontal direction at matrix-outline or halftone

2. Border mode

In border mode, characters are displayed with borders. (Refer to Table 9.) In matrix and halftone modes also, characters are displayed with borders if the BLK register (address 2B0₁₆) is set to 1.

Table 10 lists the types of borders.

Table 10 Bordering

SRAND2 (Address 2AF ₁₆)	SRAND1, 0	00	01	10	11
0	The zero dot →	 1 dot in horizontal direction	 2 dots in horizontal direction	 3 dots in horizontal direction	 4 dots in horizontal direction
1		 1 dot in horizontal direction	 2 dots in horizontal direction	 3 dots in horizontal direction	 4 dots in horizontal direction

Horizontal direction bordering is only 1 dot. When the character extends to the top line of the matrix, no border is left at the top, and when the character extends to the bottom (12th) line of the matrix, no border is left at the bottom.

3. Setting matrix outline

The ALL24 register (address 2AF16) allows you to set a matrix outline. A matrix outline can be set for each line by using the DSP1xx register (address 2AC16).

However, this setting is inhibited if the EX register (address 2B016) is 0 (external sync). An example of how you set a matrix outline is shown in Figure 5.

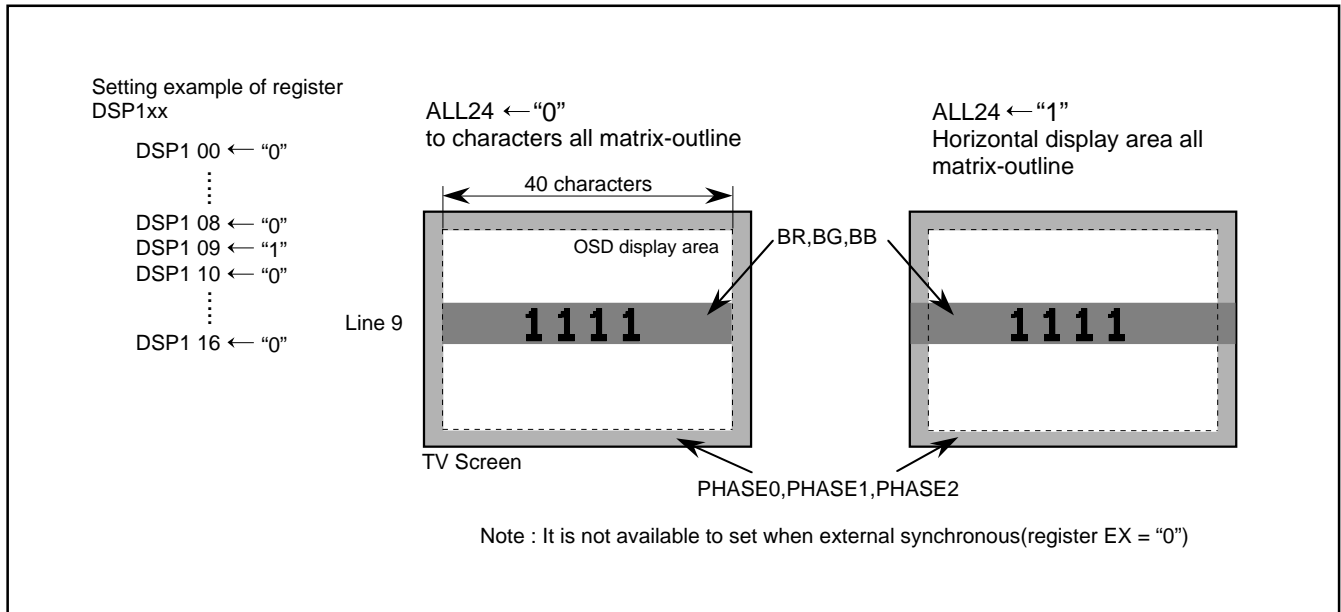


Fig. 5 Setting example all matrix-outline area

4. Blinking mode

Two patterns blinking by register BLINK3 (address 2A916) or BLINK bit of display RAM.

Blinking mode is shown in Table 11 (SYRAM do not blink).

Use registers BLINK0, 1, and 2 (address 2A916) to set the duty ratio and period that determines the blinking time. Tables 12 and 13 list the relationship between the register settings and the duty ratio and period.

Table 11 Blinking mode

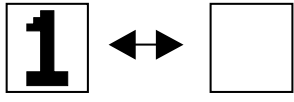
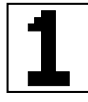
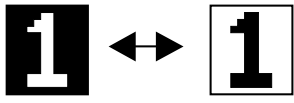

BLINK3	Blinking mode	at blinking OFF
0	Blinking 	Normal 
1	Normal character, reversed character alternation display 	Reverse 

Table 12 Setting of duty ratio

BLINK1	BLINK0	0	1
	0	Blink OFF	Duty 25%
1	Duty 50%	Duty 75%	

Table 13 Setting of cycle

BLINK2	Cycle
0	Approximately 1 second (Vertical sync divided into 1/64)
1	Approximately 0.5 second (Vertical sync divided into 1/32)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

5. Scroll display mode

The scroll display mode is entered by setting registers SBIT0 to 3 (SA), SLIN0 to 4 (SB), SST0 to 4 (SC), and SEND0 to 4 (SD) (all at address 2AE16). (Scroll is turned off when SD = 0.)

The screen is scrolled in the range from the (SC)'th line to the (SD-1)'th line, and sections above and below this range are fixed. The beginning line and beginning dot of scroll are the (SA)'th dot on

the (SB)'th line.

The screen can be scrolled up or down by successively incrementing or decrementing SA and SB.

Figure 6 shows examples of how the display is scrolled. The scroll range in these examples contains 12 lines (second to the 13th lines). However, the screen can display only 11 lines at a time, and the remaining one line is handled as a dummy line and not displayed.

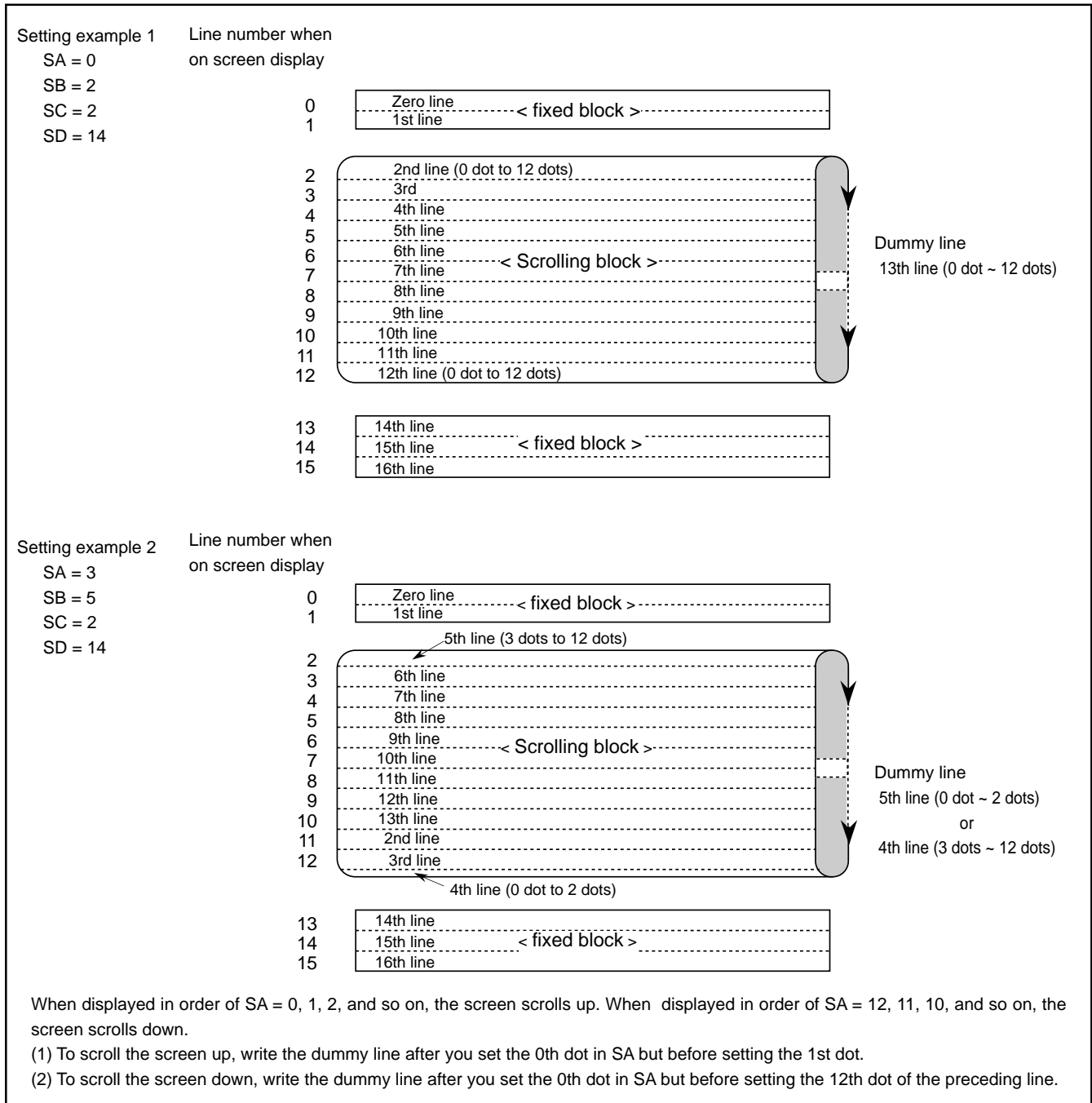


Fig. 6 Scrolling example

6. Character font

(1) Character ROM

Images are composed on a 12 X 13 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code FF16 is fixed as blank, without a background.

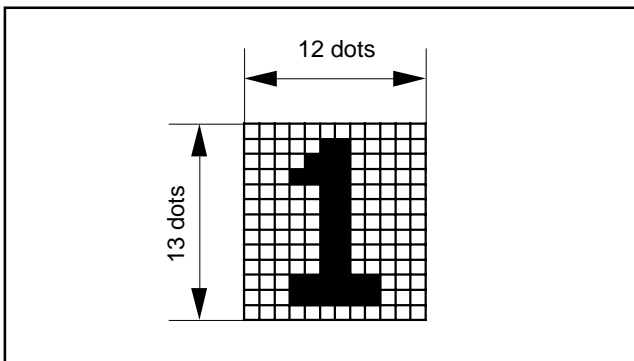


Fig. 7 Character construction

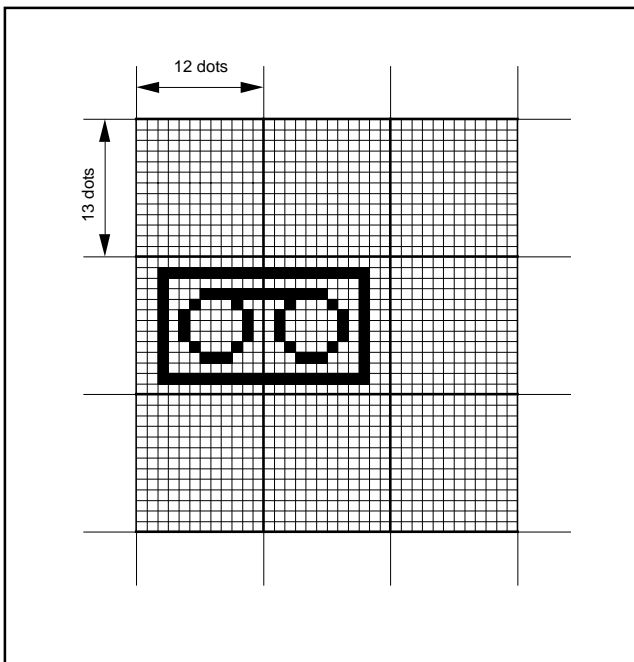


Fig. 8 Example for displaying a continuous pattern

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) SYRAM

You can set characters for 7 letters per screen (SYRAM code 00₁₆ to 06₁₆). Figure 9 shows an example of how to set.

Use display RAM's SYC2 to 0 (00₁₆ to 06₁₆) to specify SYRAM.

Note that SYRAM code 07₁₆ is fixed to a blank, so you cannot set a character font to this code.

If you do not put SYRAM and a character together, use code 07₁₆.

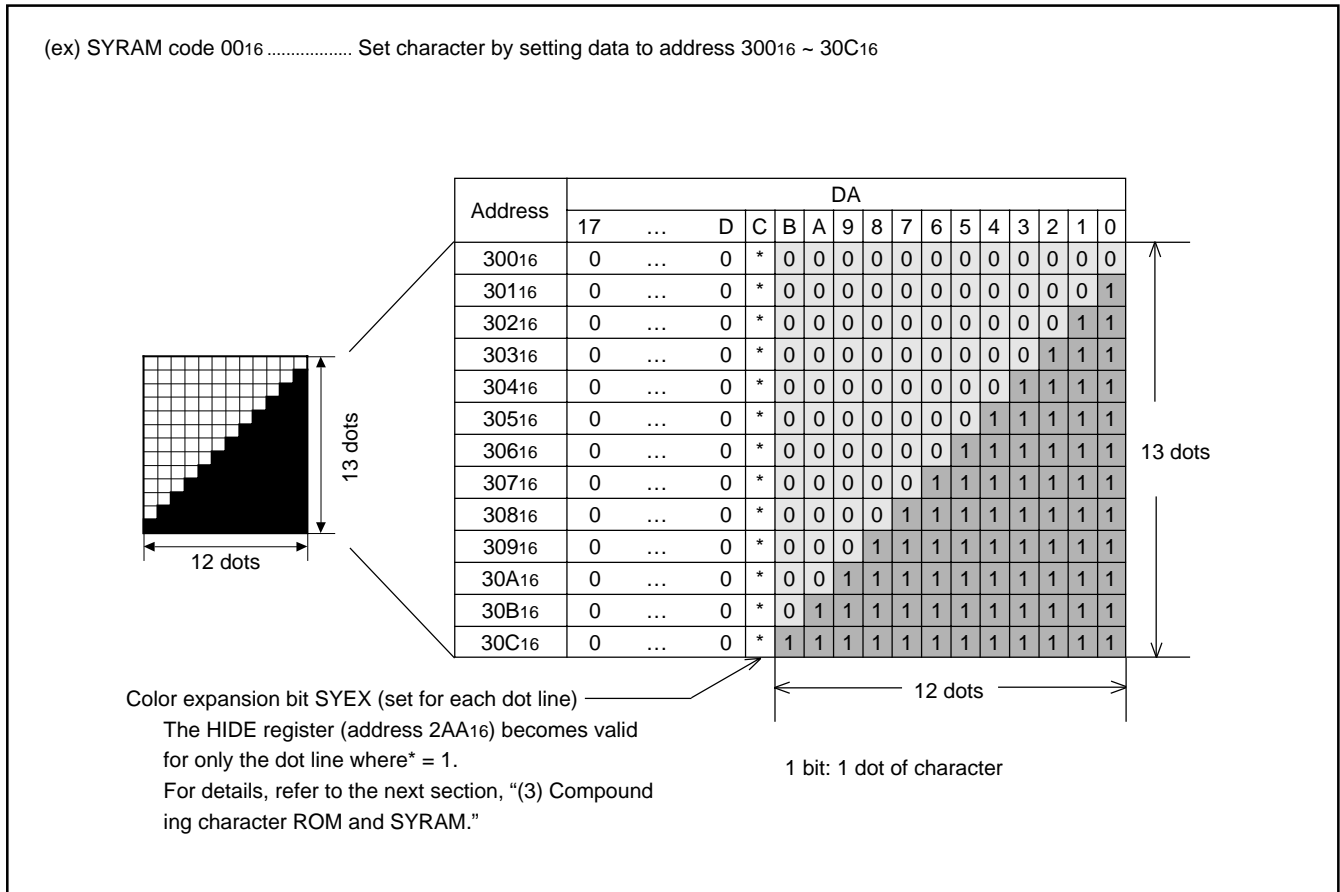


Fig. 9 Setting example of SYRAM

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Compounding character ROM and SYRAM

You can compound characters in character ROM with SYRAM.
The compounding method is determined by the SYEX color expansion bit and the HIDE register (address 2AA16).
For dot lines where SYEX = 0, the SYRAM color is set by the display RAM's SR, SG, and SB irrespective of the HIDE register's content.
If the HIDE register's content is 0, the SYRAM color for dot lines where SYEX = 1 is set by the LINER, LINEG, and LINEB registers (address 2AC16).

If the HIDE register's content is 1, the character ROM part of the dot lines where SYEX = 1 is overwritten in HIDE mode with colors set by the LINER, LINEG, and LINEB registers irrespective of the ROM's content and color. The color of the SYRAM part is set by the display RAM's SR, SG, and SB as in the case of dot lines where SYEX = 0.

Figure 10 shows an example for each instance of compounding.

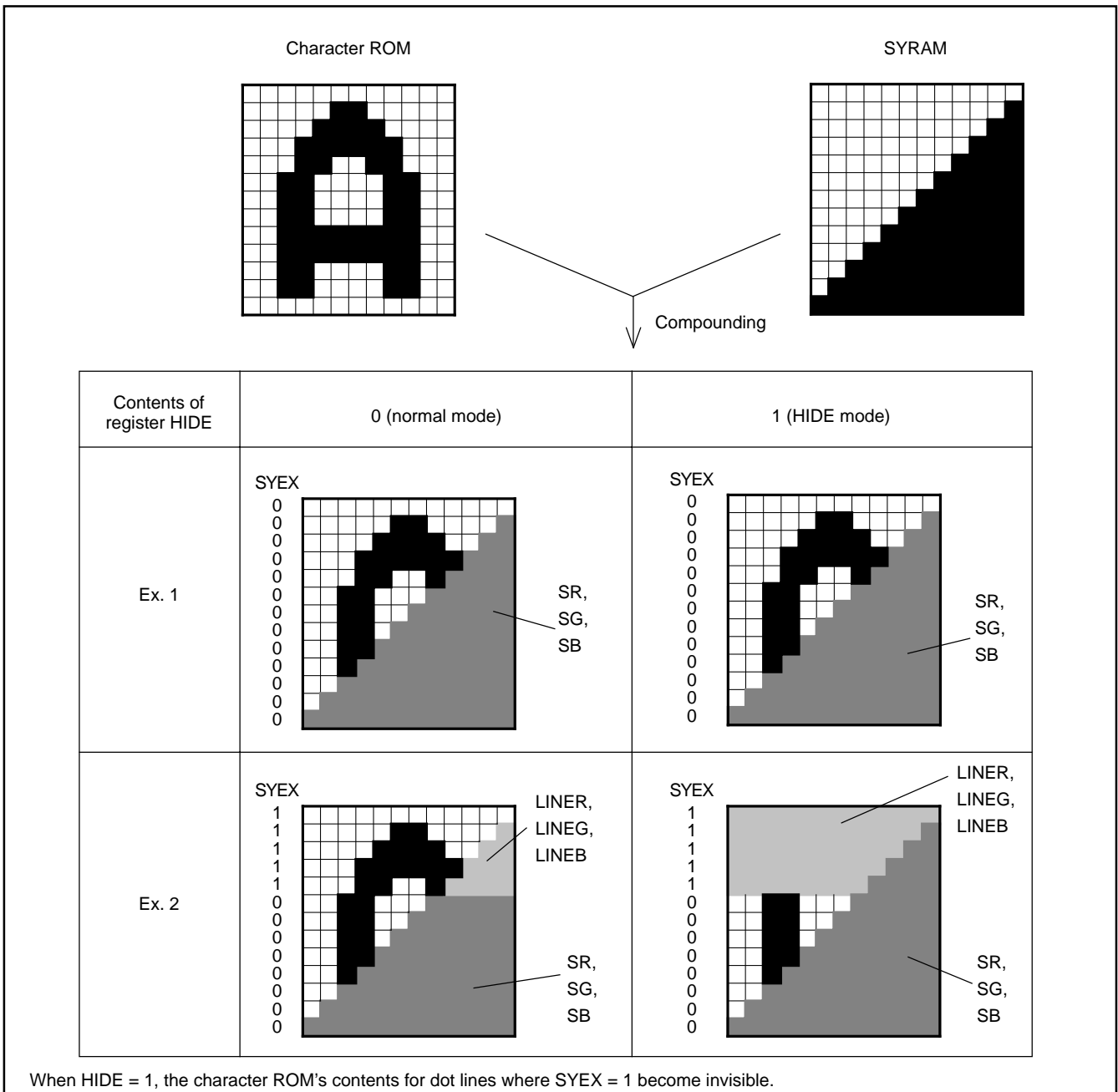


Fig. 10 Compounding example

EXAMPLE FOR DATA INPUT

Use an 8-bit parallel X 3 serial input to set data in the display RAM, display control register, and SYRAM. Table 14 lists an example of how data is set.

Table 14 Data setting

No.	Contents		DA																																					
	Address/data	Remarks	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
1	Address (2B016)	Address setting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
2	Data (2B016)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
3	Data (30016)	Set addresses SYRAM 30016 ~ 36C16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
4	Data (30116)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
93	Data (36C16)	Set address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
94	Address (00016)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
95	Data (00016)	Set registers address display RAM 00016 ~ 2A716	SB	SG	SR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
96	Data (00116)		SB	SG	SR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
773	Data (2A716)	Set registers address 2A816 ~ 2AF16	SB	SG	SR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
774	Data (2A816)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
775	Data (2A916)	Set registers address 2AA16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
776	Data (2AA16)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
777	Data (2AB16)	Set registers address 2AC16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
778	Data (2AC16)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
779	Data (2AD16)	Set registers address 2AE16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
780	Data (2AE16)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
781	Data (2AF16)	Set registers address 2B016	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ALL24	SRAND	SRAND	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	PTD	
782	Data (2B016)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



SERIAL DATA INPUT TIMING

- (1) The address consists of 8 bits X 3.
- (2) The data consists of 8 bits X 3.
- (3) The 8 bits X 3 in the SCK after the CS signal has fallen are the address, and for succeeding input data, the address is incremented every 24 bits (8 bits X 3). Refer to Fig.12 about detail for address increment.

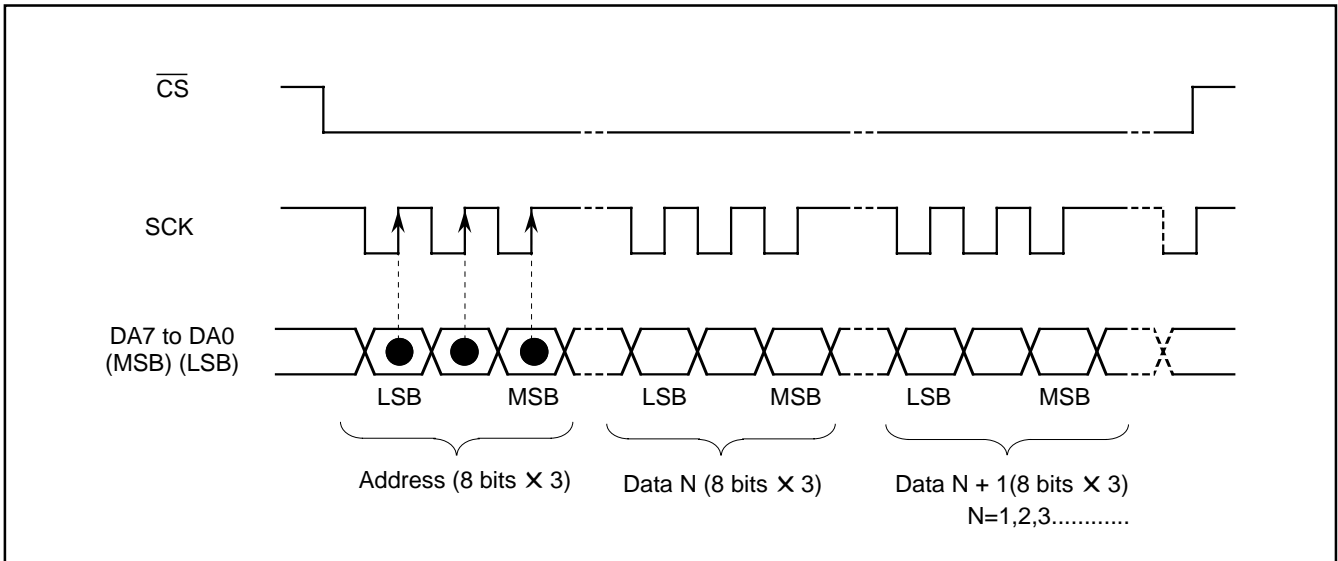


Fig. 11 Serial input timing

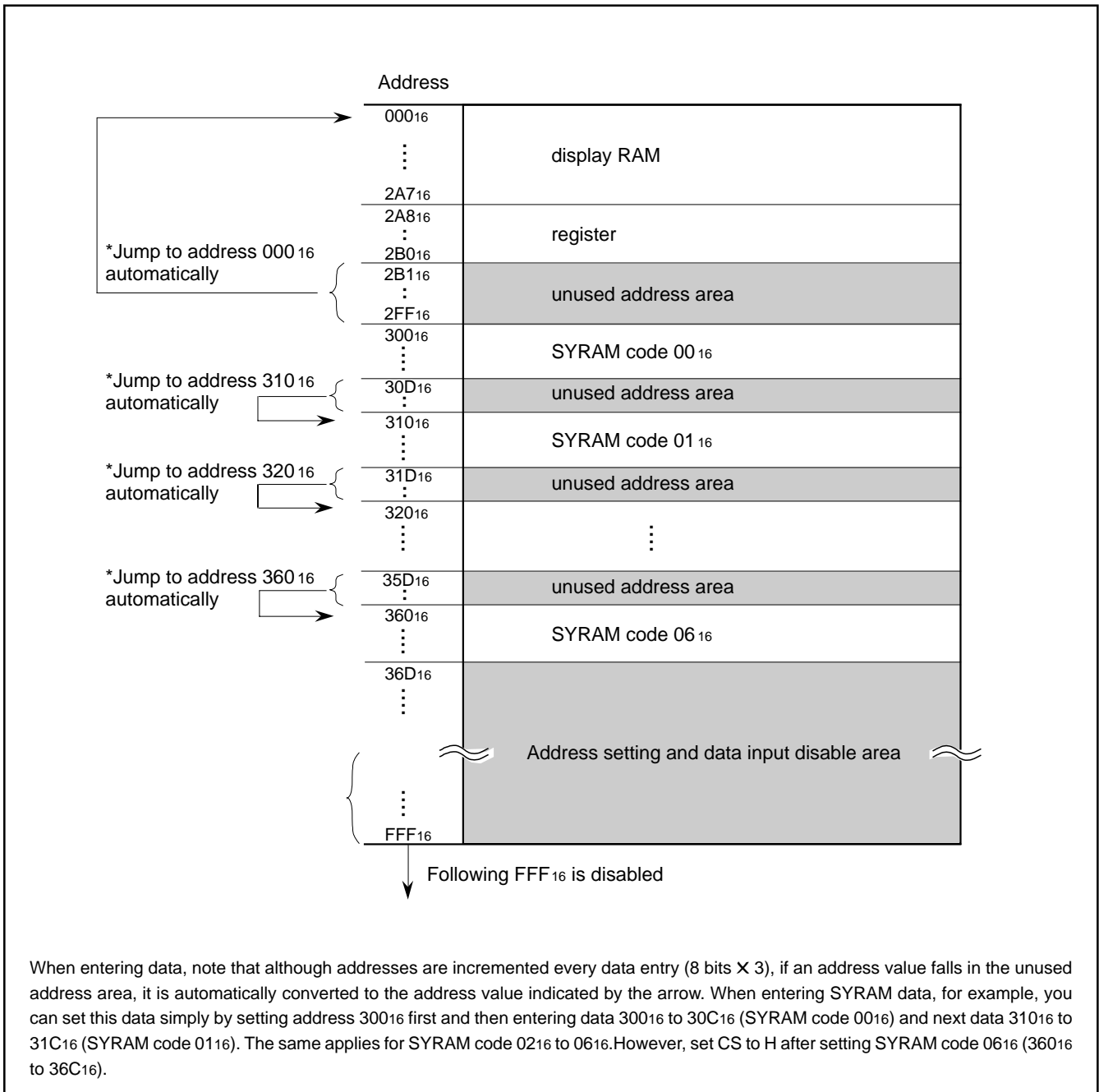


Fig. 12 Address construction

Notes on others

1. At system start-up

At system start-up, always set the AC pin to low level before setting registers.

2. Power supply noise

When power supply noise is generated, the internal oscillator circuit does not stabilize, whereby causing horizontal jitters across the picture display. Therefore, connect a bypass capacitor between the power supply and GND.

3. At power on

When power to the M35061-XXXSP/FP is activated, characters are sometimes output without defining the internal display RAM, composite RAM and register. Also, immediately after power is turned on, up until the oscillator circuit stabilizes, data is sometimes not set correctly in the register. Therefore, use the following start-up procedure.

- (a) Activate power. (AC pin = "L")
- (b) Engage auto clear. (AC pin = "H")
- (c) Disable data input for a 200 m sec (time enough to allow the internal oscillator circuit to stabilize).
- (d) Set register LEVEL n.
- (e) Set register PAL/NTSC.
- (f) Set register PC n.
- (g) Disable data input for a 20 m sec (time enough to allow the internal oscillator circuit to stabilize).
- (h) Set other registers.
- (i) Set the SYRAM.
- (j) Set the internal display RAM.
- (k) Turn registers DSPON and DSPONV on.

4. When resuming internal oscillation from the off state

The internal oscillator circuit stops oscillating when register LEVEL 1 = 1, DSPON = 0, DSPONV = 0 and CS pin = "H".

When resuming internal oscillation from the off state, up until the oscillator circuit stabilizes, data is sometimes not set correctly in the register. Therefore, start oscillation as follows.

- (a) CS pin = "H" (Oscillation off)
- (b) CS pin = "L" (Oscillation start)
- (c) Wait for a 20 m sec (time enough to allow the internal oscillator circuit to stabilize).
- (d) Set register LEVEL 1 = 0.
- (e) Set other registers, SYRAM and internal display RAM.
- (f) Turn registers DSPON and DSPONV on.

5. Other notes on oscillation

Make note of the fact that the internal oscillator circuit cannot stabilize in the below situations.

- (a) When the external composite video signal is discontinuous (when changing channels, etc.)
- (b) When register PC n setting is changed
- (c) When register LEVEL n setting is changed

Before changing settings, turn registers DSPON and DSPONV off.

Also, disable data input for 20 m sec after making settings.

6. When no external composite video signal is input

Without a signal, characters cannot be displayed by external synchronization. Therefore, switch to internal synchronization.

7. When signal level of the external composite video signal is extremely poor

With a weak electric field, character display is uncontrollable by external synchronization. Therefore, switch to internal synchronization.

8. When a crystal oscillator is used as the IC's fsc input

It is possible to connect a crystal oscillator between OSCIN and OSCOUT to input the subcarrier frequency (fsc) signal to the OSCIN pin. Talk with the manufacturer of the crystal oscillator you want to use about matching it to this IC.

However, when using a crystal oscillator, it is not possible to superimpose colors. Therefore, set the SCOR register (address 2B016 in DA1 register) to "0".

Crystal oscillator frequency	{	NTSC system: 3.580 MHz PAL system: 4.434 MHz M-PAL system: 3.576 MHz
------------------------------	---	--

9. Notes on superimposed colors

(1) Register setting

The below table gives register settings for superimposed colors.

Broad-casting method \ Register	PAL/NTSC	MPAL	EX	SCOR	PHIN pin
NTSC	0	0	0	1	Connect to GND
PAL	1	0	0	1	Input control signal. Refer to (2)
M-PAL	0	1	0	1	Input control signal. Refer to (2)

(2) Signal input to PHIN (23-pin) pin

It is necessary to input a control signal for alternating color burst phase (CB1/CB2) every other scanning line. The signal is input into the PHIN (23-pin) pin.

The below figure shows timing for the signal input to the PHIN (23-pin) pin.

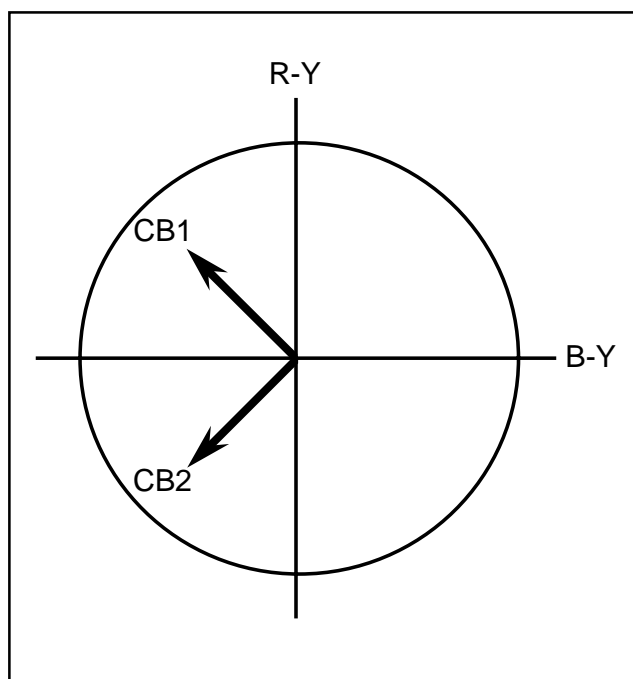


Fig. 13 Bector phase of PAL, M-PAL method

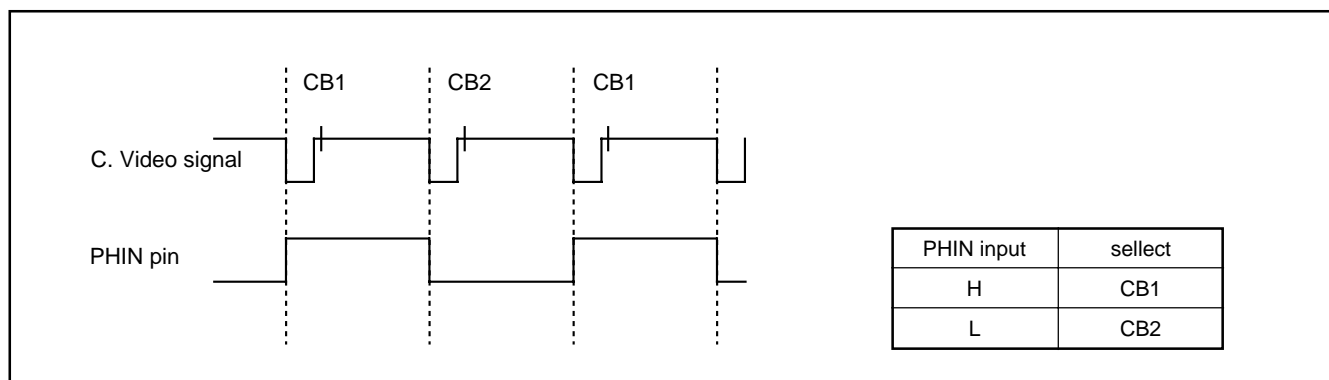


Fig. 14 Signal input timing for PHIN (23-pin) pin

10. Notes on fsc signal input

(1) This IC amplifies the subcarrier frequency (fsc) signal (NTSC system: 3.580 MHz, PAL system: 4.434 MHz, M-PAL system: 3.576 MHz) input to the OSCIN pin and generates the composite video signal internally.

The amplified fsc signal can be destabilized in the following cases.

(a) When the fsc signal is outside of recommended operating conditions

(b) When the waveform of the fsc signal is distorted

(c) When DC level in the fsc waveform fluctuates

When the amplified signal is unstable, the composite video signal generated inside the IC is also unstable in terms of synchronization with the subcarrier and phase.

Consequently, this results in color flicker and lost synchronization when the composite video signal is generated. Make note of the fact that this may prevent a stable blue background from being formed.

(2) When switching to internal synchronization from external synchronization (fsc signal is OFF), start fsc signal input 20 m sec or more before the internal oscillator circuit stabilizes.

M35061-XXXSP/FP PERIPHERAL CIRCUIT (For external fsc input)

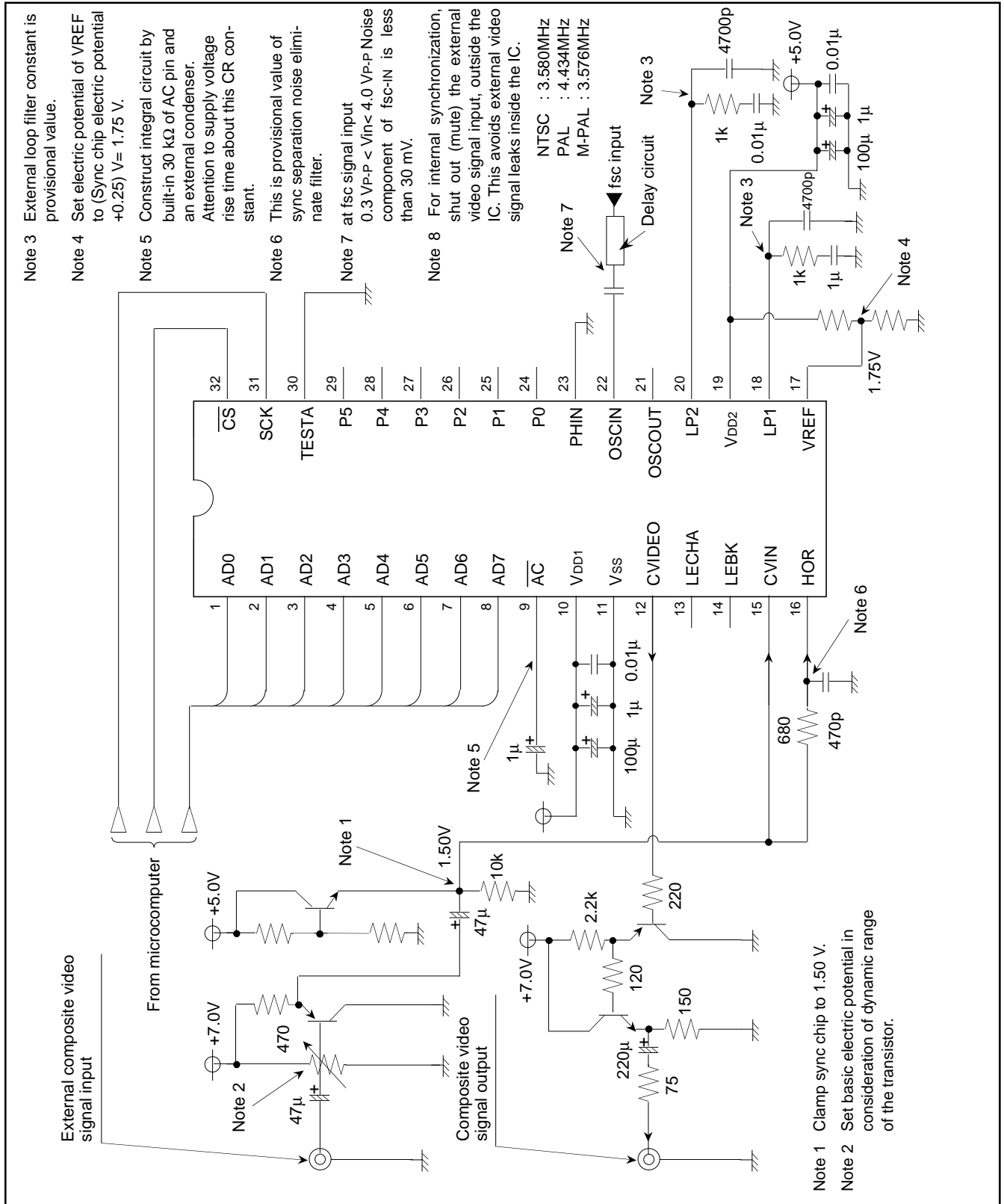


Fig.15 M35061-XXXSP/FP example of peripheral circuit

M35061-XXXSP/FP PERIPHERAL CIRCUIT (When using a crystal oscillator)

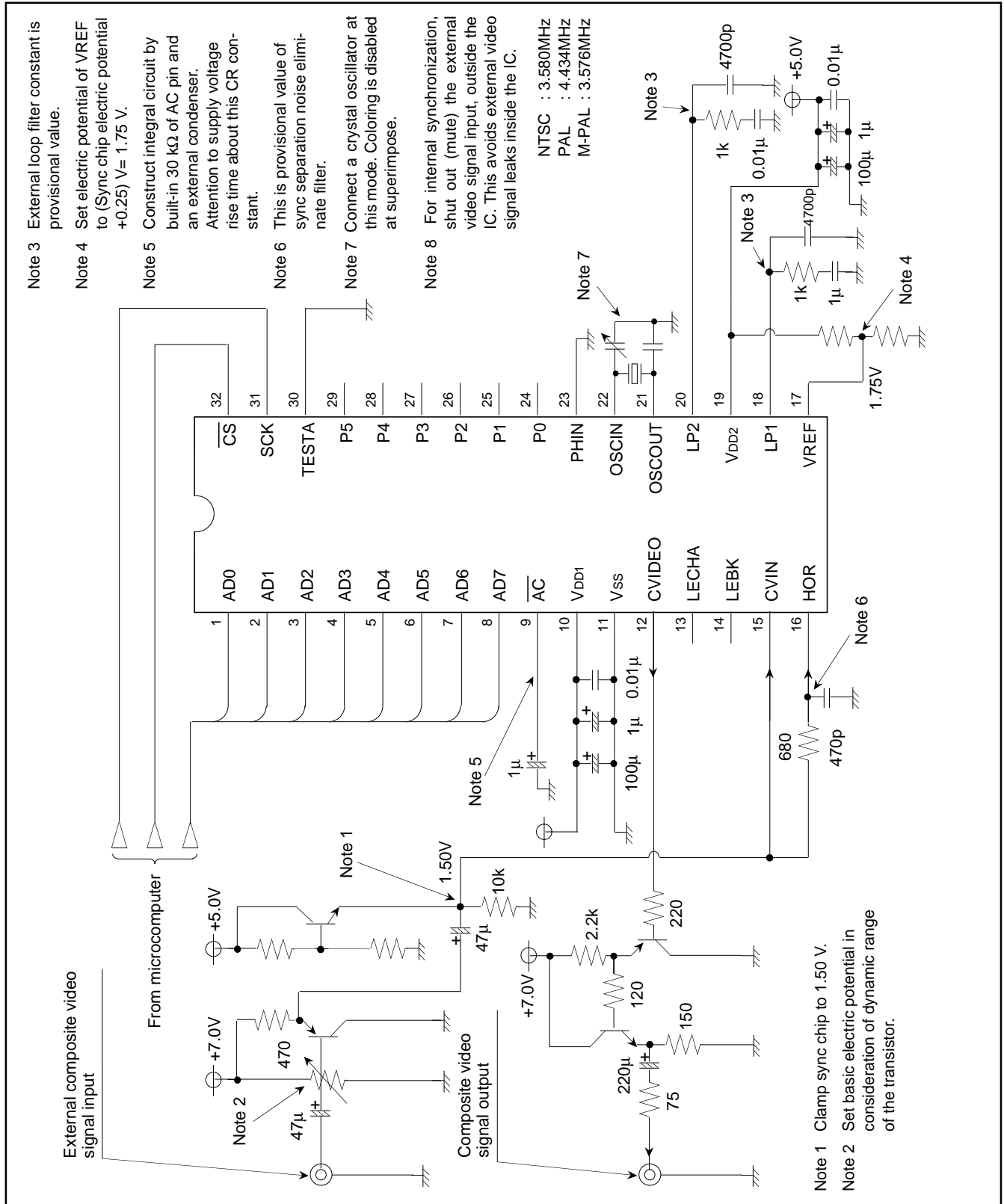


Fig.16 M35061-XXXSP/FP example of peripheral circuit

TIMING REQUIREMENTS ($T_a = -20^{\circ}\text{C} \sim +70^{\circ}\text{C}$, $V_{DD} = 5.00 \pm 0.25\text{V}$ unless otherwise noted)

DATA INPUT

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{SCK})$	SCK width	200	—	—	ns
$t_{su}(\overline{\text{CS}})$	$\overline{\text{CS}}$ setup time	200	—	—	ns
$t_h(\overline{\text{CS}})$	$\overline{\text{CS}}$ hold time	2	—	—	ms
$t_{su}(\text{AD})$	AD setup time	200	—	—	ns
$t_h(\text{AD})$	AD hold time	200	—	—	ns
$t_h(\text{SCK})$	1 word hold time	2	—	—	ms

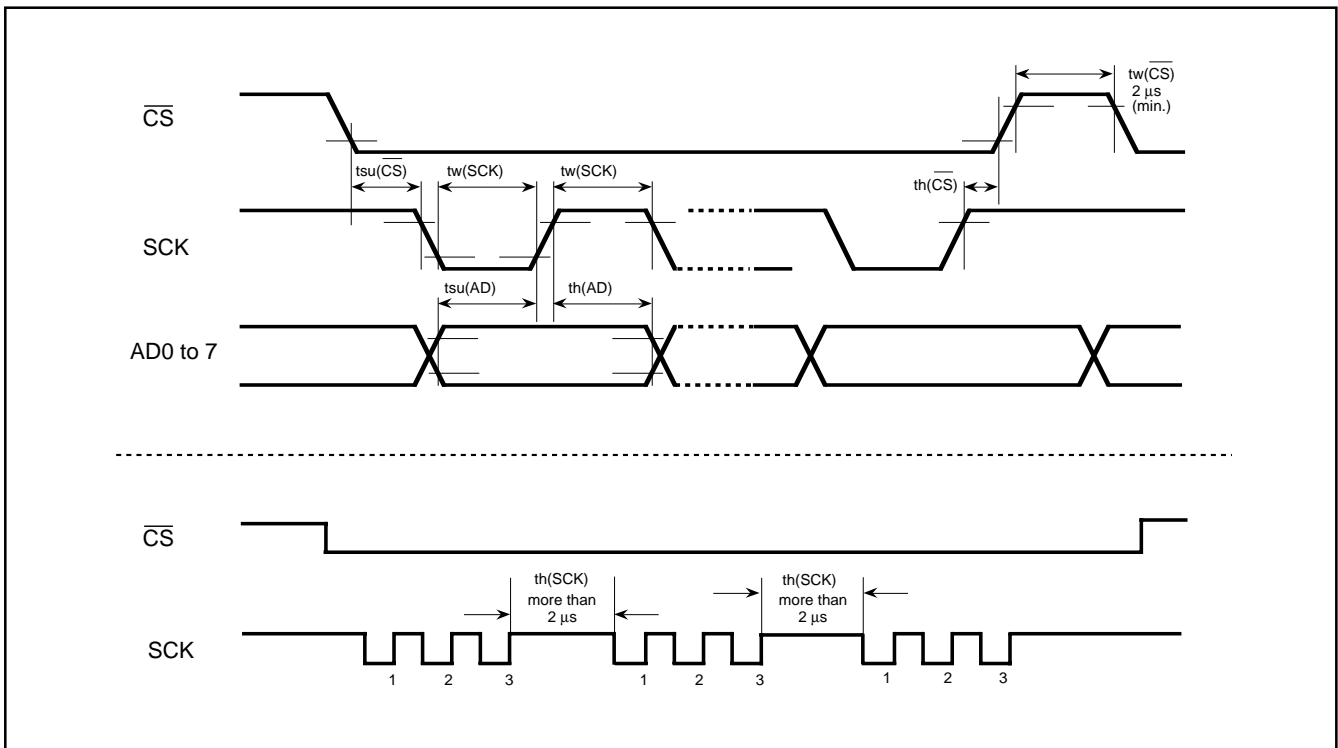


Fig. 17 Serial input timing requirements

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

ABSOLUTE MAXIMUM RATINGS ($V_{DD} = 5.00V$, $T_a = -20^{\circ}C \sim +70^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
VDD	Supply voltage	With respect to Vss.	- 0.3 ~ 6.0	V
VI	Input voltage		$V_{SS} - 0.3 < V_I < V_{DD} + 0.3$	V
VO	Output voltage		$V_{SS} < V_O < V_{DD}$	V
Pd	Power dissipation	$T_a = 25^{\circ}C$	300	mW
Topr	Operating temperature		- 20 ~ 70	$^{\circ}C$
Tstg	Storage temperature		- 40 ~ 125	$^{\circ}C$

RECOMMENDED OPERATIONAL CONDITIONS ($V_{DD} = 5.00 V$, $T_a = -20^{\circ}C \sim +70^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VDD	Supply voltage	4.75	5.00	5.25	V
VIH	"H" level input voltage \overline{AC} , \overline{CS} , SCK, AD0 ~ AD7	$0.8 \times V_{DD}$	V_{DD}	V_{DD}	V
VIL	"L" level input voltage \overline{AC} , \overline{CS} , SCK, AD0 ~ AD7	0	0	$0.2 \times V_{DD}$	V
VCVIN	Composite video input voltage CVIN	—	2 VP-P	—	V
VOSCIN	Input voltage OSCIN	0.3 VP-P	—	4.0 VP-P	V
fOSCIN	Oscillation frequency for synchronous signal (Duty 40~60%)	—	3.580 4.434 3.576	—	MHz

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VDD	Supply voltage	$T_a = -20^{\circ}C \sim +70^{\circ}C$	4.75	5.00	5.25	V
IDD	Supply current	$V_{DD} = 5.00 V$	—	25	50	mV
VOH	"H" level output voltage P0 ~ P5	$V_{DD} = 4.75$, $I_{OH} = -0.2 mA$	3.75	—	—	V
VOL	"L" level output voltage P0 ~ P5	$V_{DD} = 4.75$, $I_{OL} = 0.2 mA$	—	—	0.4	V
RI	Pull-up resistance \overline{AC}	$V_{DD} = 5.00 V$	10	30	100	k Ω

VIDEO SIGNAL INPUT CONDITIONS ($V_{DD} = 5.00 V$, $T_a = -20^{\circ}C \sim +70^{\circ}C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VIN-CU	Composite video signal input clamp voltage	Sync-chip voltage	—	1.5	—	V

NOTE FOR SUPPLYING POWER

(1) Timing of power supplying to AC pin

The internal circuit of M35061-XXXSP/FP is reset when the level of the auto clear input pin AC is "L".

This pin is hysteresis input with the pull-up resistor. The timing about power supplying of AC pin is shown in Figure 18.

After supplying the power (VDD and VSS) to M35061-XXXSP/FP, the t_w time must be reserved for 1 ms or more.

Before starting input from the microcomputer, the waiting time (ts) must be reserved for 200 ms after the supply voltage to the AC pin becomes $0.8 \times V_{DD}$ or more.

(2) Timing of power supplying to VDD1 pin and VDD2 pin

The power need to supply to VDD1 and VDD2 at a time, though it is separated perfectly between the VDD1 as the digital line and the VDD2 as the analog line.

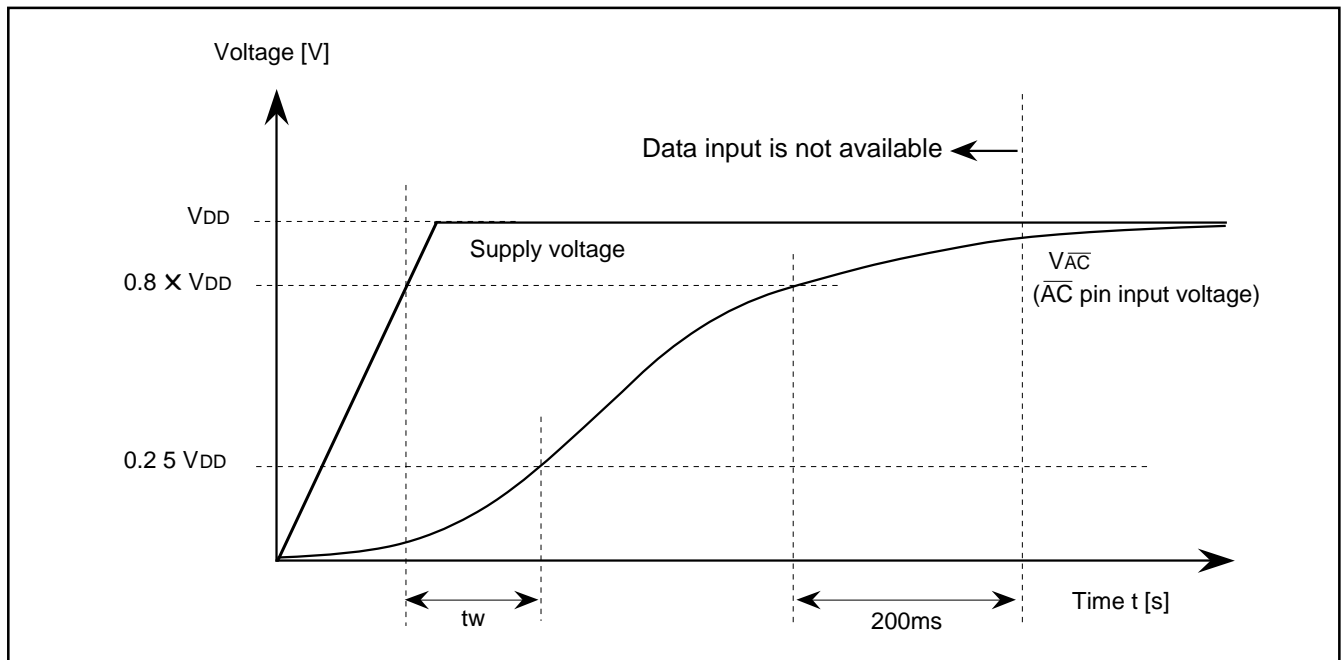


Fig. 18 Timing of power supplying to AC pin

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor (0.1μF) directly between the V_{DD1} pin and V_{SS} pin, and the V_{DD2} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M35061-XXXSP/FP mask ROM order confirmation form
- (2) 32P2W-A, 32P4B mask specification form
- (3) ROM data (EPROM 3 sets)
- (4) Floppy disks containing the character font generating program +character data

STANDARD ROM TYPE: M35061-002SP/FP

M35061-002SP/FP is a standard ROM type of M35061-XXXSP/FP.

Character patterns are fixed to the contents of Figure 19 to 20.

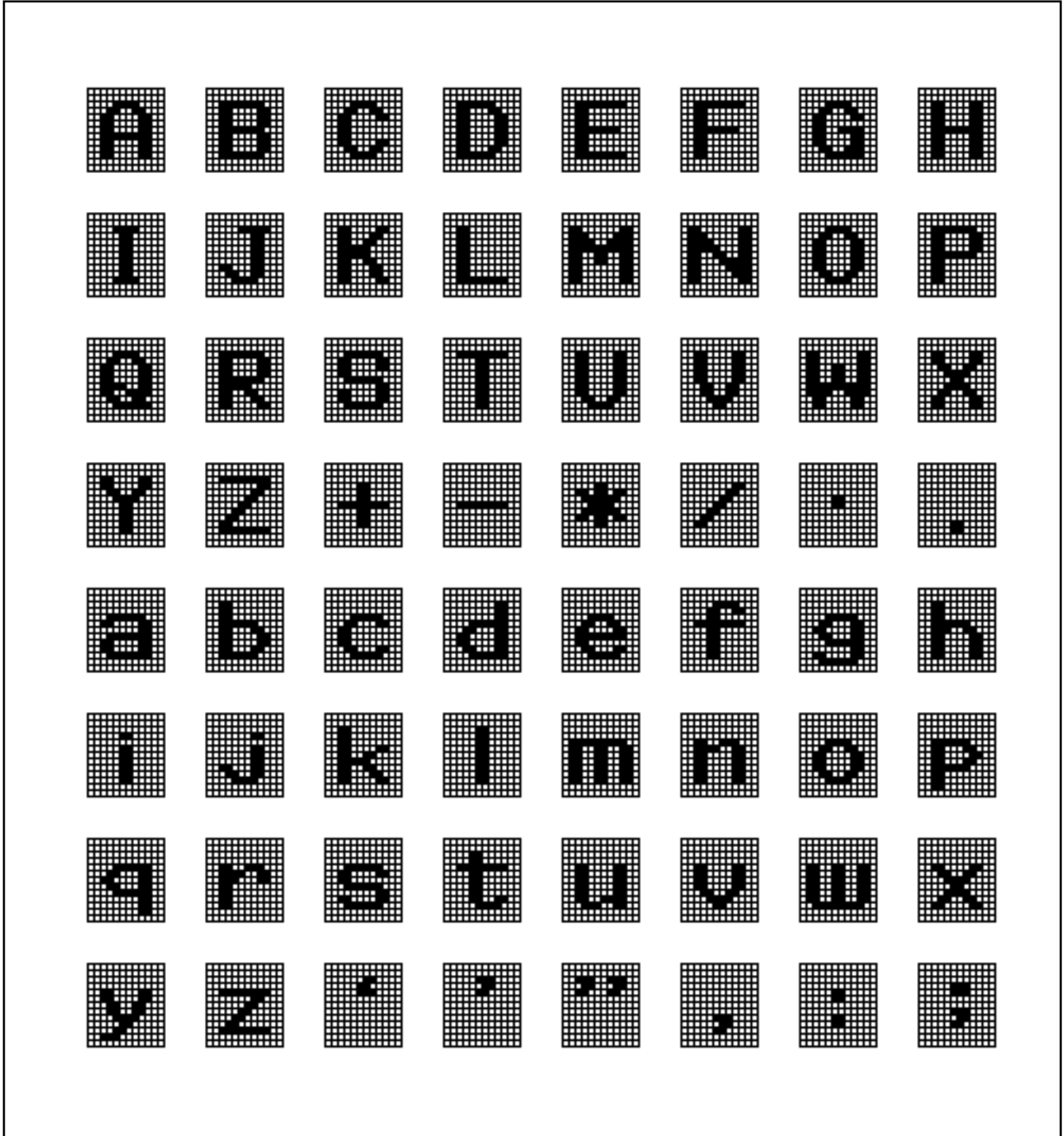


Fig. 19 M35061-002SP/FP Character patterns (1)

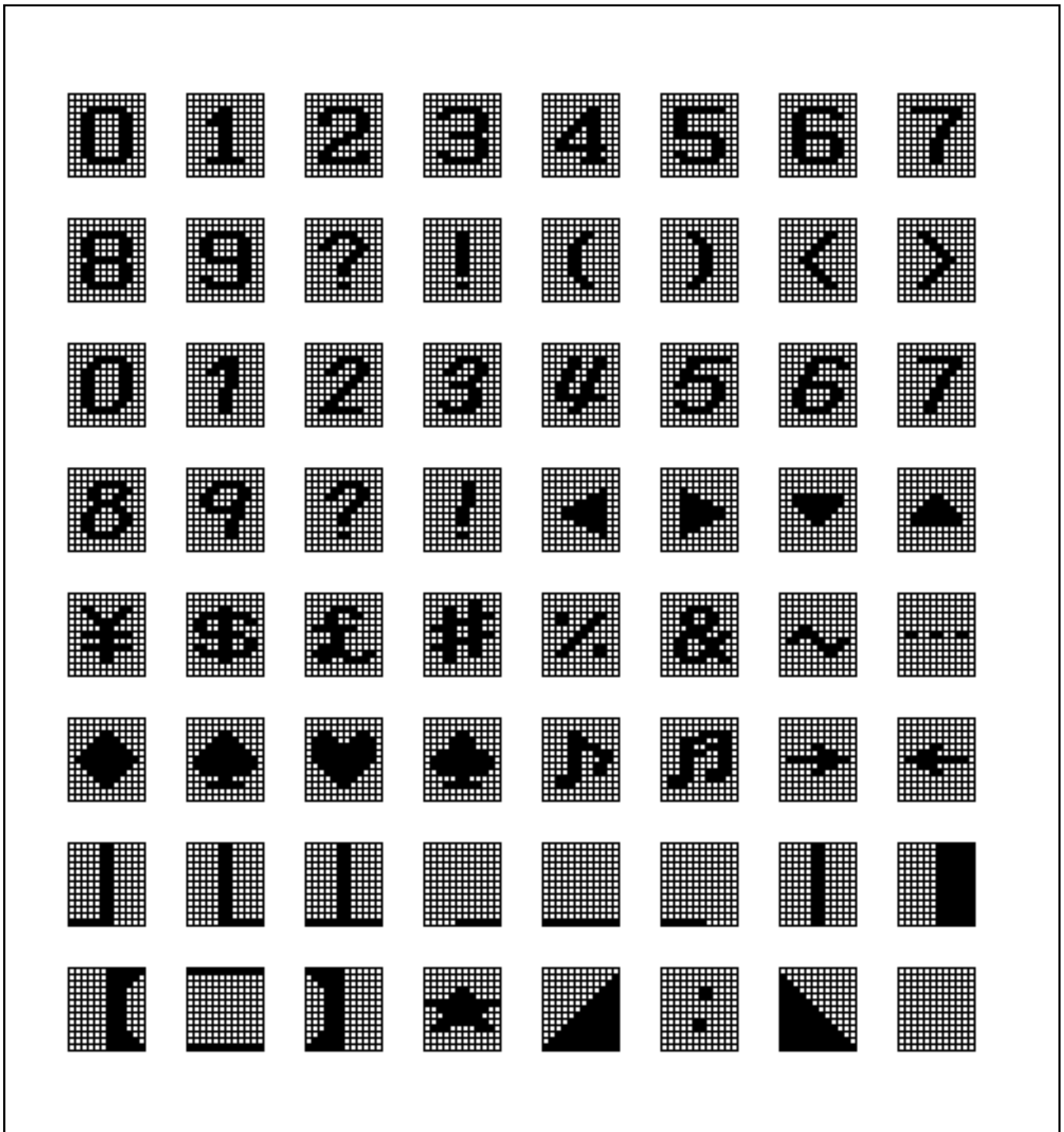


Fig. 20 M35061-002SP/FP Character patterns (2)



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