

Low power dual operational amplifiers

Features

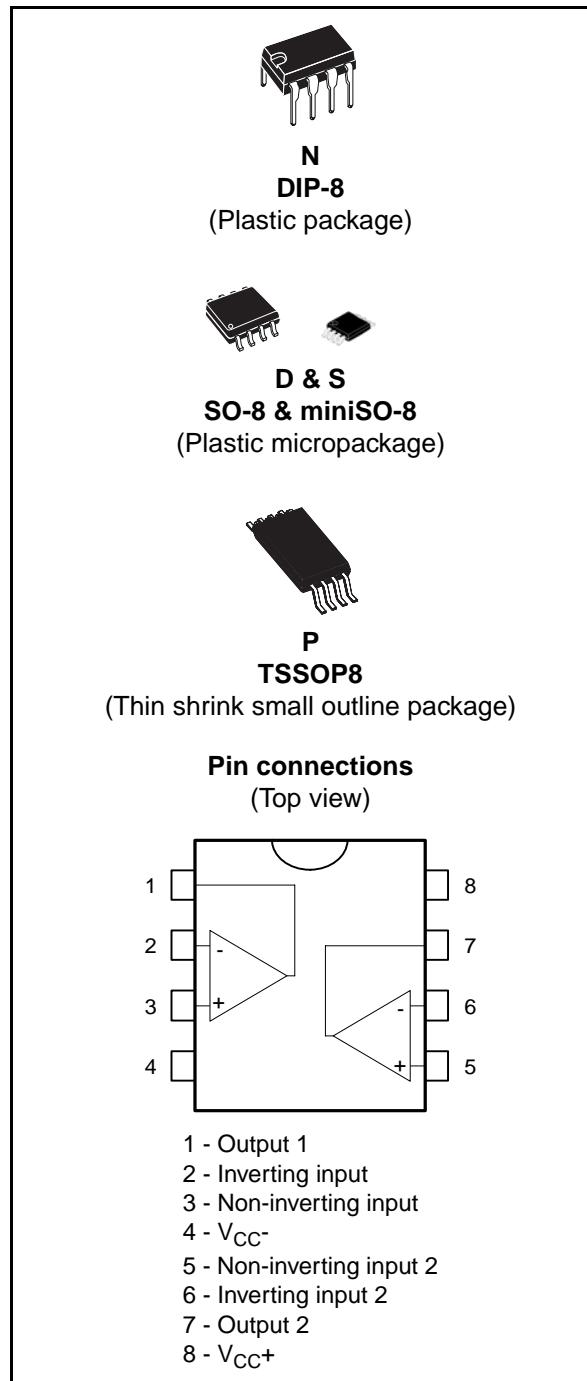
- Internally frequency compensated
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 mHz (temperature compensated)
- Very low supply current per operator essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to (V_{CC} - 1.5 V)

Description

These circuits consist of two independent, high-gain, internally frequency-compensated op-amps which are designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard +5 V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

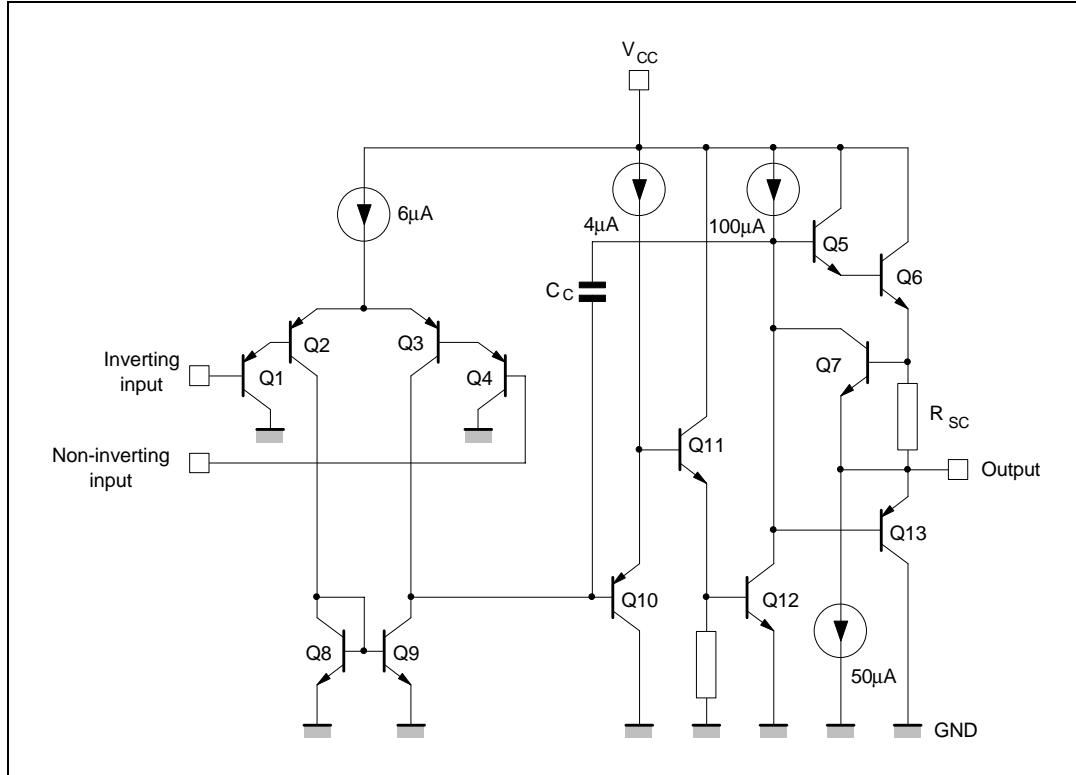


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1 Schematic diagram

Figure 1. Schematic diagram (1/2 LM158)



2 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	LM158,A	LM258,A	LM358,A	Unit
V_{CC}	Supply voltage	± 16 or 32			V
V_i	Input voltage	32			V
V_{id}	Differential input voltage	32			V
P_{tot}	Power dissipation ⁽¹⁾	500			mW
	Output short-circuit duration ⁽²⁾	Infinite			
I_{in}	Input current ⁽³⁾	50			mA
T_{oper}	Operating free-air temperature range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150			°C
T_j	Maximum junction temperature	150			°C
R_{thja}	Thermal resistance junction to ambient ^{(4) (5)}	125 190 120 85			°C/W
R_{thjc}	Thermal resistance junction to case	40 39 37 41			°C/W
ESD	HBM: human body model ⁽⁶⁾	300			V
	MM: machine model ⁽⁷⁾	200			V
	CDM: charged device model ⁽⁸⁾	1.5			kV

1. Power dissipation must be considered to ensure that the maximum junction temperature (T_j) is not exceeded.
2. Short-circuits from the output to V_{CC} can cause excessive heating if $V_{CC} > 15$ V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC} . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
7. Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
8. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

3 Operating conditions

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 32	V
V_{icm}	Common mode input voltage range $T_{amb} = +25^\circ C$	$V_{DD} -0.3$ to $V_{CC} -1.5$	V
T_{oper}	Operating free air temperature range LM158 LM258 LM358 LM258Y-LM358Y	-55 - +125 -40 - +105 0 - +70 -40 - +125	°C

4 Electrical characteristics

Table 3. Electrical characteristics for $V_{CC^+} = +5V$, V_{CC^-} = Ground, $V_o = 1.4V$, $T_{amb} = +25^\circ C$ (unless otherwise specified)

Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input offset voltage ⁽¹⁾ $T_{amb} = +25^\circ C$ LM158, LM258 LM158A		1	3		2	7	mV
	$T_{min} \leq T_{amb} \leq T_{max}$ LM158, LM258			2			5	
I_{io}	Input offset current $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		2	10 30		2	30 40	nA
I_{ib}	Input bias current ⁽²⁾ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		20	50 100		20	150 200	nA
A_{vd}	Large signal voltage gain $V_{CC} = +15 V$, $R_L = 2 k\Omega$, $V_o = 1.4 V$ to $11.4 V$ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		50 25	100		V/mV
SVR	Supply voltage rejection ratio ($R_s \leq 10 k\Omega$) $V_{CC^+} = 5 V$ to $30 V$ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	65 65	100		65 65	100		dB
I_{CC}	Supply current, all amp, no load $T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC} = +5 V$ $T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC} = +30 V$		0.7	1.2 2		0.7	1.2 2	mA
V_{icm}	Input common mode voltage range $V_{CC} = +30 V$ ⁽³⁾ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$V_{CC^+} - 1.5$ $V_{CC^+} - 2$	0 0		$V_{CC^+} - 1.5$ $V_{CC^+} - 2$	V
CMR	Common mode rejection ratio ($R_s \leq 10 k\Omega$) $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	70 60	85		70 60	85		dB
I_{source}	Output current source $V_{CC} = +15 V$, $V_o = +2 V$, $V_{id} = +1 V$	20	40	60	20	40	60	mA
I_{sink}	Output sink current ($V_{id} = -1 V$) $V_{CC} = +15 V$, $V_o = +2 V$ $V_{CC} = +15 V$, $V_o = +0.2 V$	10 12	20 50		10 12	20 50		mA μA

Table 3. Electrical characteristics for $V_{CC^+} = +5V$, V_{CC^-} = Ground, $V_o = 1.4V$, $T_{amb} = +25^\circ C$ (unless otherwise specified)

Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OPP}	Output voltage swing ($R_L = 2 k\Omega$) $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$V_{CC^+} - 1.5$ $V_{CC^+} - 2$	0 0		$V_{CC^+} - 1.5$ $V_{CC^+} - 2$	
V_{OH}	High level output voltage ($V_{CC^+} = 30 V$) $T_{amb} = +25^\circ C$, $R_L = 2 k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $T_{amb} = +25^\circ C$, $R_L = 10 k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	26 26 27 27	27 28		26 26 27 27	27 28		V
V_{OL}	Low level output voltage ($R_L = 10 k\Omega$) $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20		5	20 20	mV
SR	Slew rate $V_{CC} = 15V$, $V_i = 0.5$ to $3V$, $R_L = 2k\Omega$ $C_L = 100pF$, unity Gain	0.3	0.6		0.3	0.6		V/ μ s
GBP	Gain bandwidth product $V_{CC} = 30 V$, $f = 100$ kHz, $V_{in} = 10$ mV, $R_L = 2 k\Omega$, $C_L = 100$ pF	0.7	1.1		0.7	1.1		MHz
THD	Total harmonic distortion $f = 1$ kHz, $A_v = 20$ dB, $R_L = 2 k\Omega$, $V_o = 2 V_{pp}$, $C_L = 100$ pF, $V_O = 2 V_{pp}$		0.02			0.02		%
e_n	Equivalent input noise voltage $f = 1$ kHz, $R_s = 100 \Omega$, $V_{CC} = 30 V$		55			55		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input offset voltage drift		7	15		7	30	$\mu V/^\circ C$
DI_{io}	Input offset current drift		10	200		10	300	pA/ $^\circ C$
V_{o1}/V_{o2}	Channel separation ⁽⁴⁾ 1kHz $\leq f \leq 20$ kHz		120			120		dB

1. $V_o = 1.4 V$, $R_s = 0 \Omega$, $5 V < V_{CC^+} < 30 V$, $0 < V_{ic} < V_{CC^+} - 1.5 V$
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC^+} - 1.5 V$, but either or both inputs can go to +32 V without damage.
4. Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

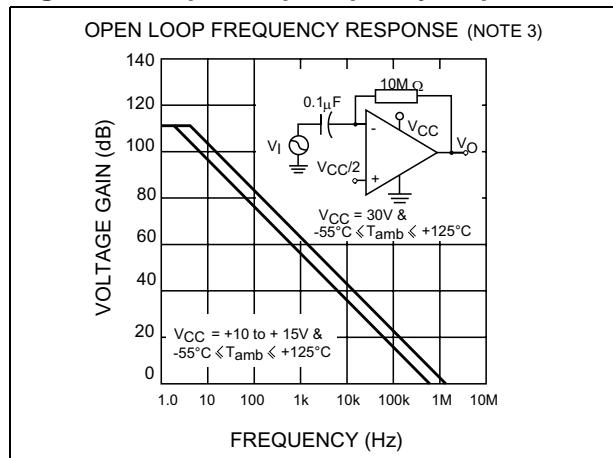
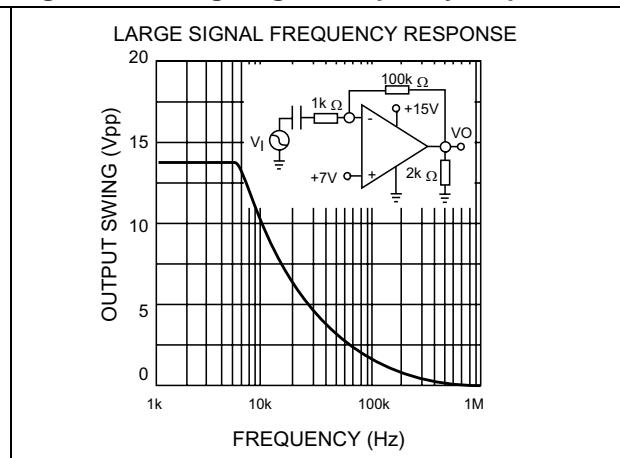
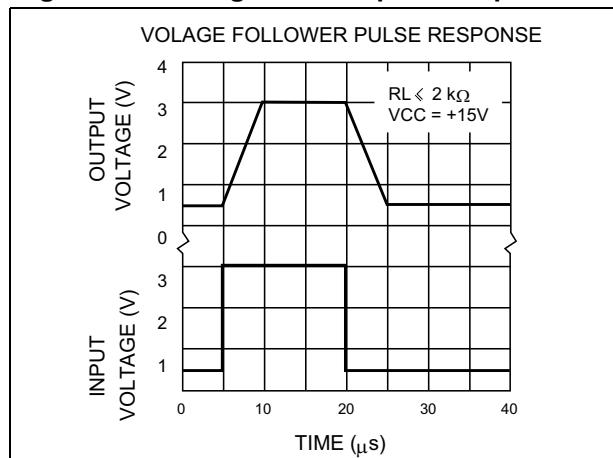
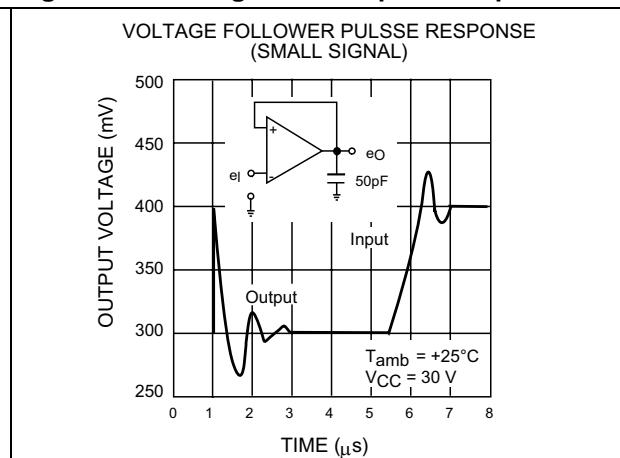
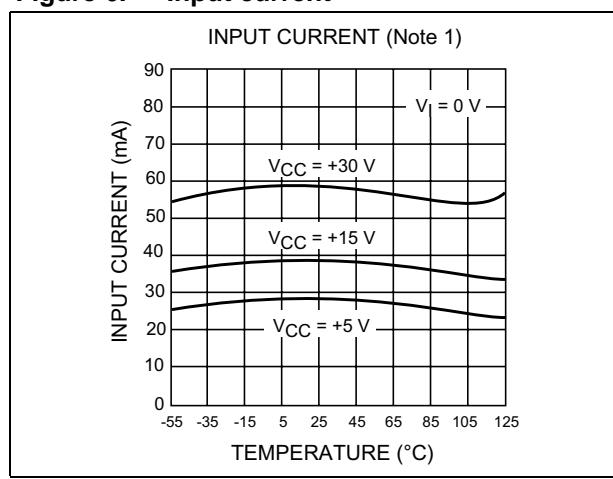
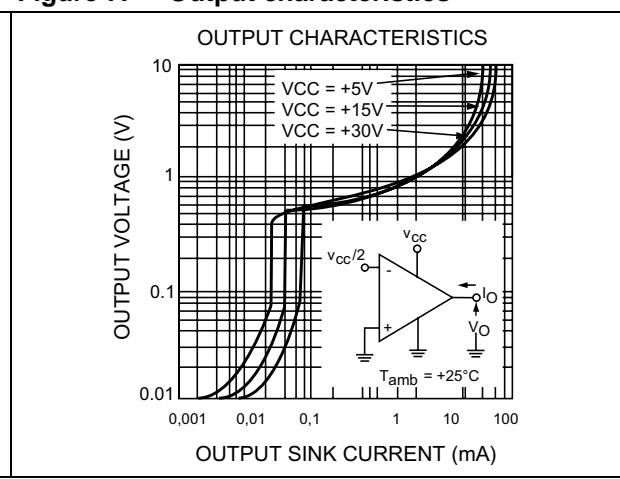
Figure 2. Open loop frequency response**Figure 3. Large signal frequency response****Figure 4. Voltage follower pulse response****Figure 5. Voltage follower pulse response****Figure 6. Input current****Figure 7. Output characteristics**

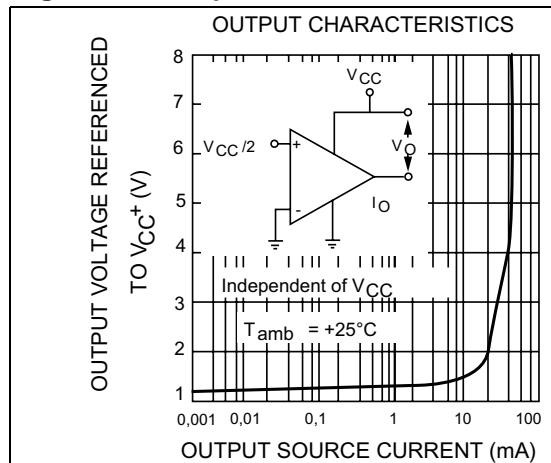
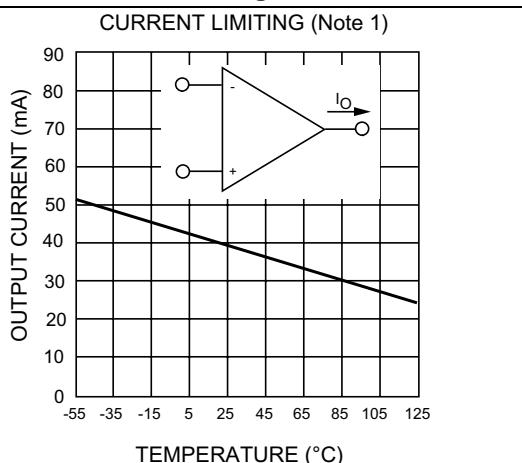
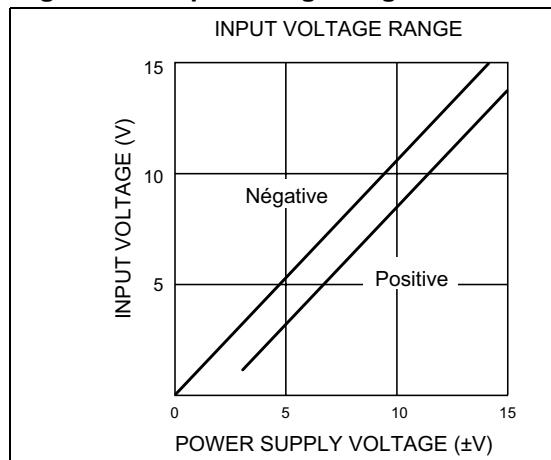
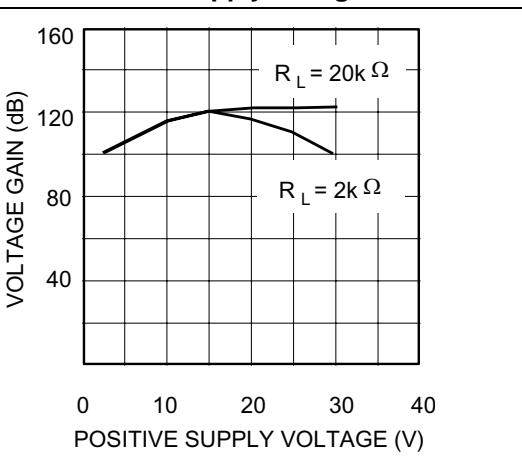
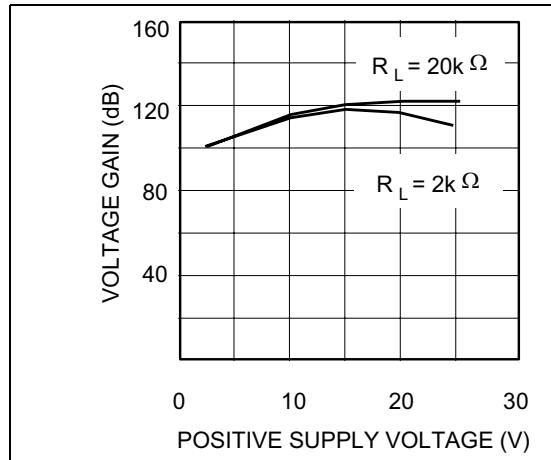
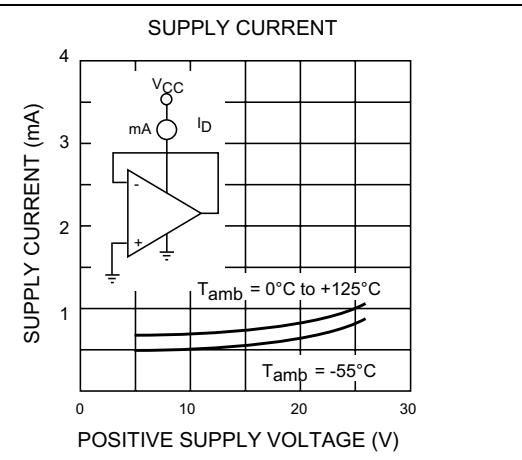
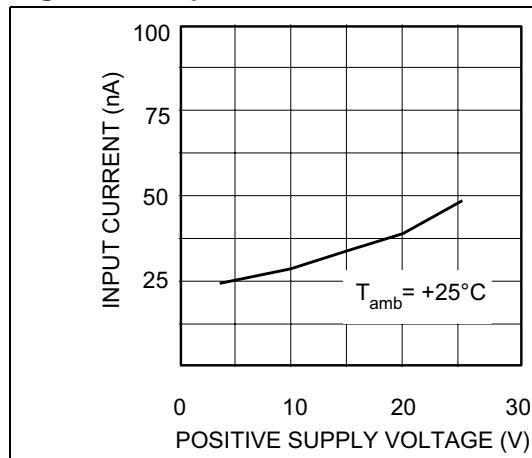
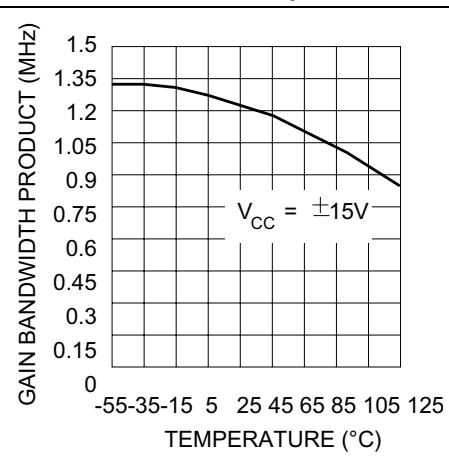
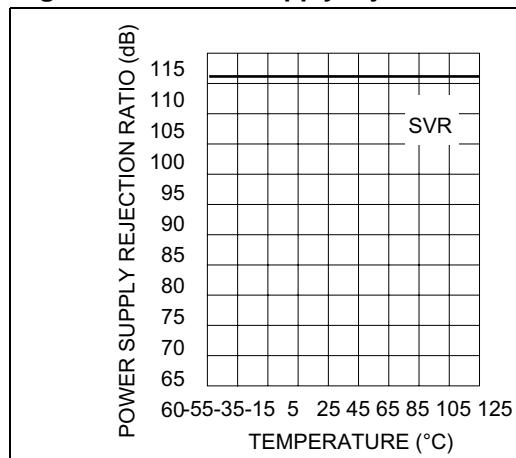
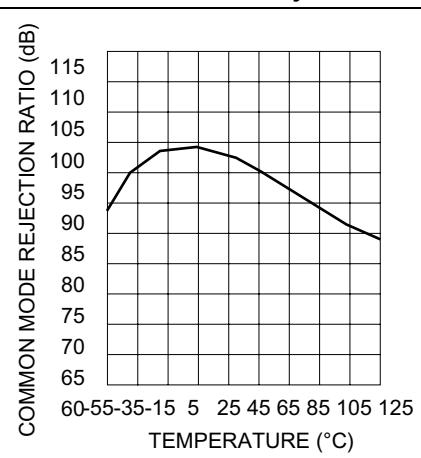
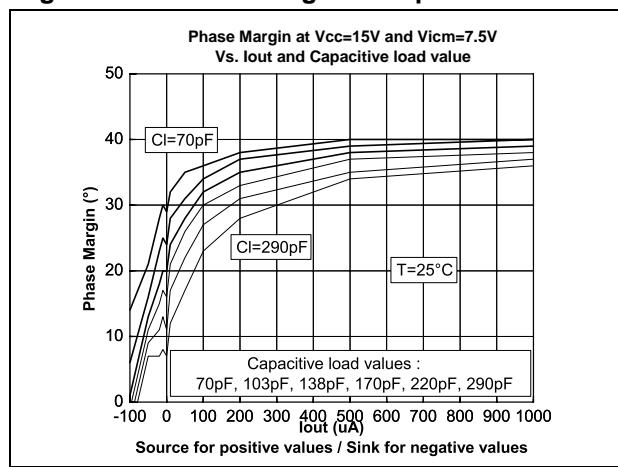
Figure 8. Output characteristics**Figure 9. Current limiting****Figure 10. Input voltage range****Figure 11. Positive supply voltage****Figure 12. Input voltage range****Figure 13. Supply current**

Figure 14. Input current**Figure 15. Gain bandwidth product****Figure 16. Power supply rejection ratio****Figure 17. Common mode rejection ratio****Figure 18. Phase margin vs capacitive load**

5 Typical applications

Single supply voltage $V_{CC} = +5V_{DC}$

Figure 19. AC coupled inverting amplifier

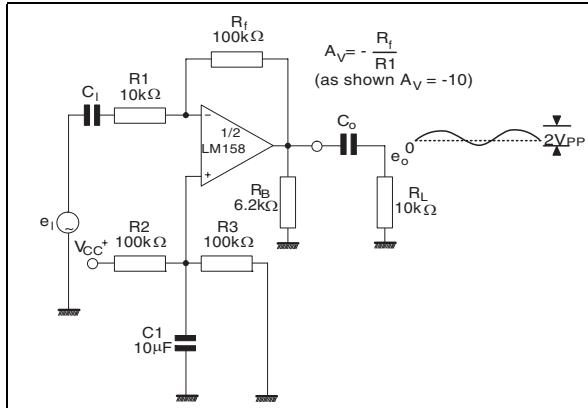


Figure 20. Non-inverting DC amplifier

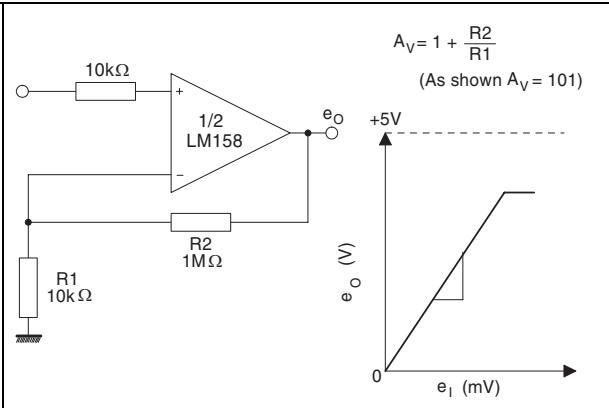


Figure 21. AC coupled non-inverting amplifier

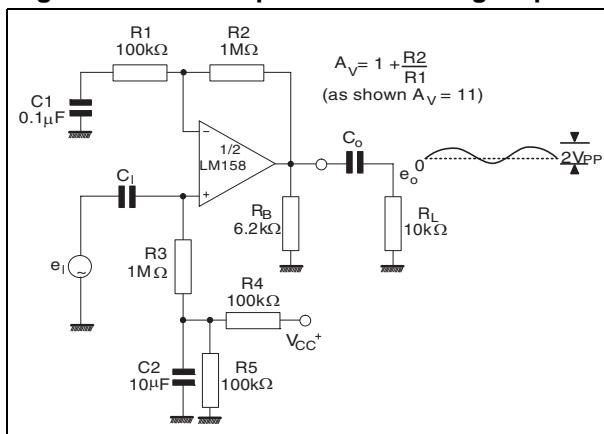


Figure 22. DC summing amplifier

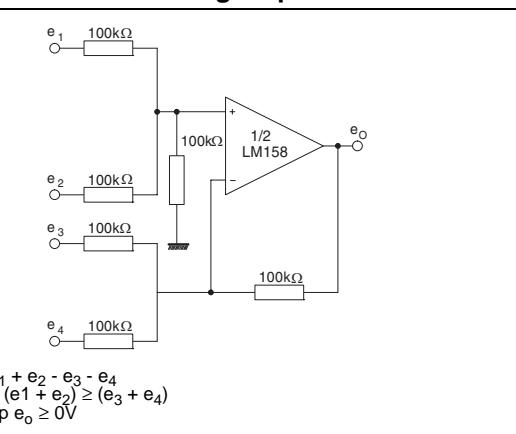


Figure 23. High input Z, DC differential amplifier

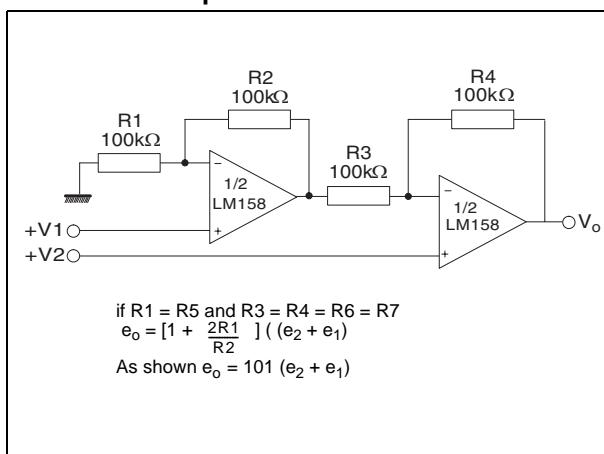


Figure 24. High input Z adjustable gain DC instrumentation amplifier

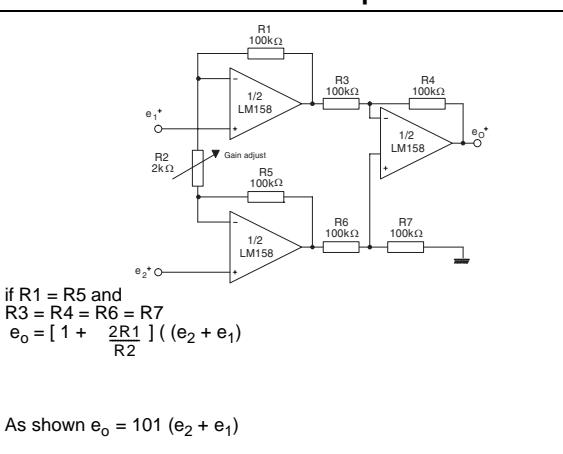


Figure 25. Using symmetrical amplifiers to reduce input current

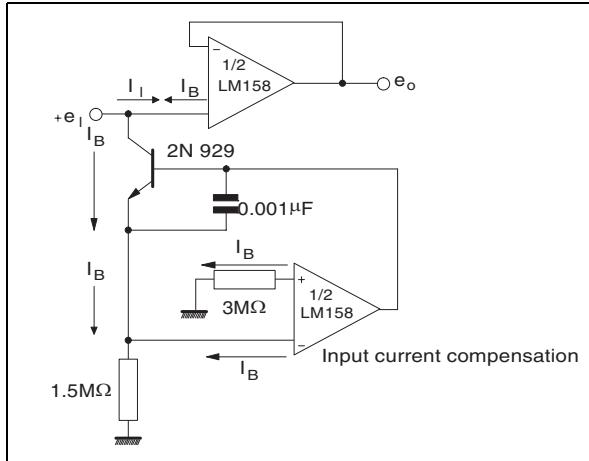


Figure 26. Low drift peak detector

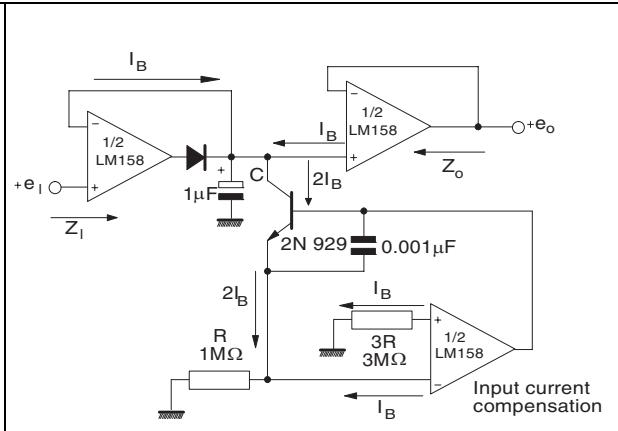
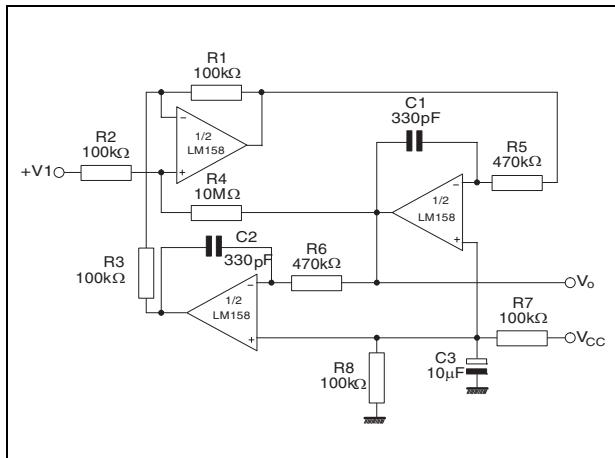


Figure 27. Active band-pass filter



6 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

6.1 DIP8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

The technical drawings illustrate the physical dimensions of the DIP8 package. The top view shows the footprint with pins numbered 1 through 8. The side view shows the height (E) and lead spacing (eA, eB). The cross-sectional view shows the lead thickness (c), lead height (E1), and the gauge plane at 0.38 mm from the bottom surface.

6.2 SO-8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

The technical drawings illustrate the physical dimensions and seating plane details for the SO-8 package. The top view shows the footprint with pins numbered 1 through 8. The side view shows height dimensions A, A1, A2, b, c, D, E, E1, h, L, and k. The cross-sectional view shows the lead profile with a gage plane at 0.25 mm above the seating plane C, and dimensions L1 and L.

6.3 MiniSO-8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004

The figure contains three technical drawings of the MiniSO-8 package. The top drawing is a top-down view showing the footprint and pin numbers (1 through 8). It includes dimensions for lead thickness (A1), lead height (D), lead width (E1), lead angle (K), lead spacing (b), and Pin 1 identification. The middle drawing is a side view showing lead height (A1) and lead angle (K). The bottom drawing is a cross-sectional view showing the seating plane (C), gage plane, lead thickness (L), lead height (L1), and lead angle (K).

6.4 TSSOP8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	

The figure contains two technical drawings of the TSSOP8 package. The top drawing is a side cross-sectional view showing the lead frame, bond wires, and chip. It labels dimensions A, A1, A2, b, c, D, E1, e, k, L, L1, and aaa. Below it is a top-down view of the package showing pin numbers 1 through 8 and a central circular feature. It also shows the seating plane, gage plane, and a dimension of 0.25 mm or .010 inch between the seating and gage planes. A vertical line labeled 'PIN 1 IDENTIFICATION' points to pin 1.

7 Ordering information

Part number	Temperature range	Package	Packaging	Marking	
LM158N	-55°C, +125°C	DIP-8	Tube	LM158N	
LM158D LM158DT		SO-8	Tube or tape & reel	158	
LM158YD LM158YDT ⁽¹⁾		SO-8 Automotive grade		158Y	
LM258AN	-40°C, +105°C	DIP-8	Tube	LM258A	
LM258AD LM258ADT		SO-8	Tube or tape & reel	258A	
LM258AYD LM258AYDT ⁽¹⁾		SO-8 Automotive grade		258AY	
LM258PT		TSSOP-8 (Thin shrink outline package)	Tape & reel	258	
LM258APT		TSSOP-8 Automotive grade		258A	
LM258YPT ⁽¹⁾				258Y	
LM258AYPT				258AY	
LM258AST		miniISO-8	Tape & reel	K408	
LM258N		DIP-8	Tube	LM258N	
LM258D LM258DT		SO-8	Tube or tape & reel	258	
LM258YD LM258YDT ⁽¹⁾		SO-8 Automotive grade		258Y	
LM358N	0°C, +70°C	DIP-8	Tube	LM358N	
LM358AN		SO-8	Tube or tape & reel	LM358AN	
LM358D LM358DT				358	
LM358YD LM358YDT ⁽¹⁾		SO-8 Automotive grade		358Y	
LM358AD LM358ADT		SO-8		358A	
LM358PT		TSSOP-8 (Thin shrink outline package)	Tape & reel	358	
LM358APT				358A	
LM358YPT ⁽¹⁾		TSSOP-8 Automotive grade		358Y	
LM358AYPT ⁽¹⁾				358AY	
LM358ST		miniISO-8	Tape & reel	K405	
LM358AST				K404	

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

8 Revision history

Date	Revision	Changes
1-Jul- 2003	1	First release.
2-Jan-2005	2	R_{thja} and T_j parameters added in AMR Table 1 on page 4 .
1-Jul-2005	3	ESD protection inserted in Table 1 on page 4 .
5-Oct-2006	4	Added Figure 18: Phase margin vs capacitive load .
30-Nov-2006	5	Added missing ordering information.
25-Apr-2007	6	Removed LM158A, LM258A and LM358A from document title. Corrected error in miniSO8 package data. L1 is 0.004 inch. Added automotive grade order codes in Section 7 on page 18 .

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