

HI-REL DATA SHEET

HM 65789

16 k x 4 HIGH SPEED CMOS SRAM WITH OUTPUT ENABLE

FEATURES

- FAST ACCESS TIME : 25/35/45/55 ns
- LOW POWER CONSUMPTION
ACTIVE : 267 mW (typ)
STANDBY : 75 mW (typ)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY
- OUTPUT ENABLE

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DESCRIPTION

The HM 65789 is a high speed CMOS static RAM organized as 16384 x 4 bits. It is manufactured using MHS's high performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 385 mW.

The HM 65789 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 60 % when the circuit is deselected.

Easy memory expansion is provided by an active low

chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.

All inputs and outputs of the HM 65789 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM 65789 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

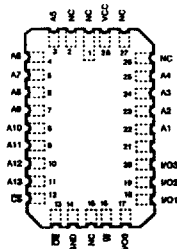
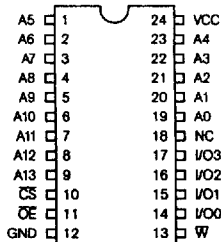
PACKAGES

Ceramic 300 mils, 24 pins, DIL.

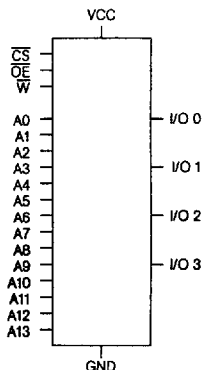
LCC, 28 pins.

Pinout DIL 24 pins (top view)

Pinout LCC 28 pins (top view)

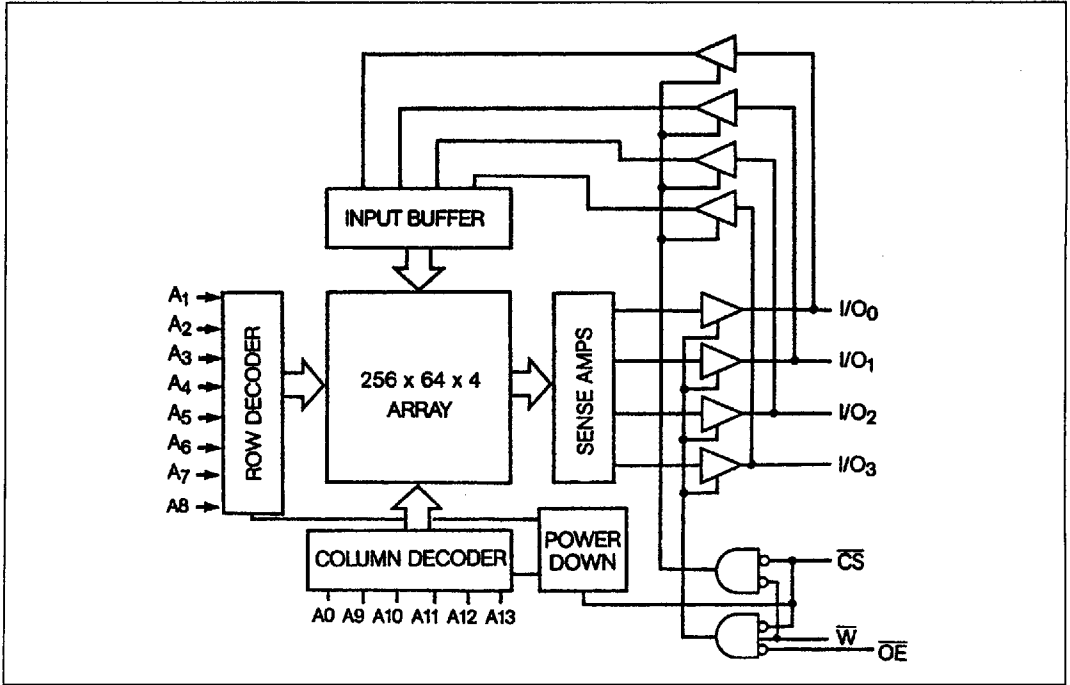


LOGIC SYMBOL



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BLOCK DIAGRAM



PIN NAMES

A0-A13 : Address inputs	$\overline{CS}$: Chip-Select
I/O0-I/O3 : Inputs/Outputs	$\overline{OE}$: Output enable
VCC : Power	$\overline{W}$: Write Enable
GND : Ground	

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	X	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
 DC input voltage : - 3.0 V to 7.0 V
 DC output voltage in high Z state : - 0.5 V to + 7.0 V
 Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20 mA
 Electro static discharge voltage : > 2001 V
 (MIL STD 883C method 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	5 V $\pm$ 10 %	- 55°C to + 125°C
Industrial	5 V $\pm$ 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS

DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65789 H	65789 K	65789 M	65789 N	Unit	Value	Note 6
ICCSB1 (1)	Standby supply current	20	20	20	20	mA	Max	M
ICCSB1 (1a)	Standby supply current	40	30	30	30	mA	Max	M
ICCOP (2)	Operating supply current	100	100	100	100	mA	Max	M
IIX (3)	Input leakage current	$\pm$ 10	$\pm$ 10	$\pm$ 10	$\pm$ 10	μ A	Max	M
IOZ (3)	Output leakage current	$\pm$ 10	$\pm$ 10	$\pm$ 10	$\pm$ 10	μ A	Max	M
VIL (4)	Input low voltage	0.8	0.8	0.8	0.8	V	Max	T
VIH (4)	Input high voltage	2.2	2.2	2.2	2.2	V	Min	T
VOL (5)	Output low voltage	0.4	0.4	0.4	0.4	V	Max	M
VOH (5)	Output high voltage	2.4	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	5	5	5	5	pF	Max	G
C OUT	Output capacitance	7	7	7	7	pF	Max	G

Notes : 1. $\overline{CS} \geq V_{CC} - 0.3V$, $V_{IN} > V_{CC} - 0.3V$ or $\leq 0.3V$

1a. $\overline{CS} \geq V_{IH} \text{ Max } V_{CC}$, Min Duty cycle = 100 %

2. V_{CC} max, Output current = 0 mA, Minimum cycle

3. V_{CC} max, $V_{IN} = Gnd$ to V_{CC}

4. V_{IL} min = - 3.0V, V_{IH} max = V_{CC}

5. V_{CC} Min, $I_{OL} = 8$ mA, $I_{OH} = - 4$ mA

6. Including open/short test or inputs clamp voltage.

G - Guaranteed - Not tested : Parameter measured at design validation and at any design change.

M - Measured : Parameter measured and data-log capability.

T - Tested : Parameter verification during testing.

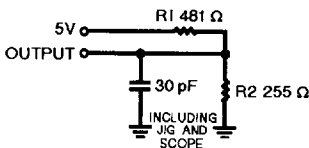
AC TEST LOADS AND WAVEFORMS

Fig.1a.

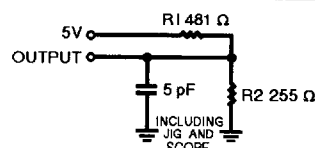


Fig.1b

Equivalent to : THEVENIN EQUIVALENT
 OUTPUT $\text{---} 167 \Omega \text{---} 1.73 V$

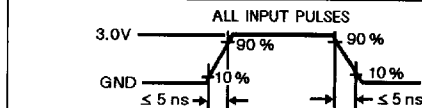


Fig.2 All input pulses

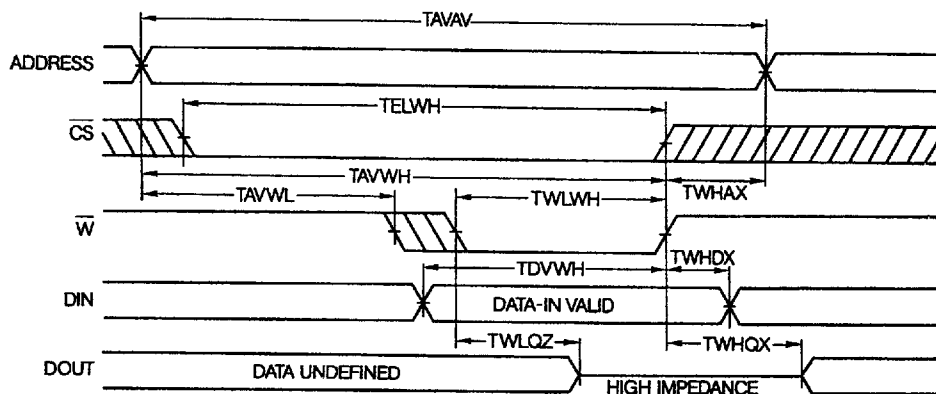
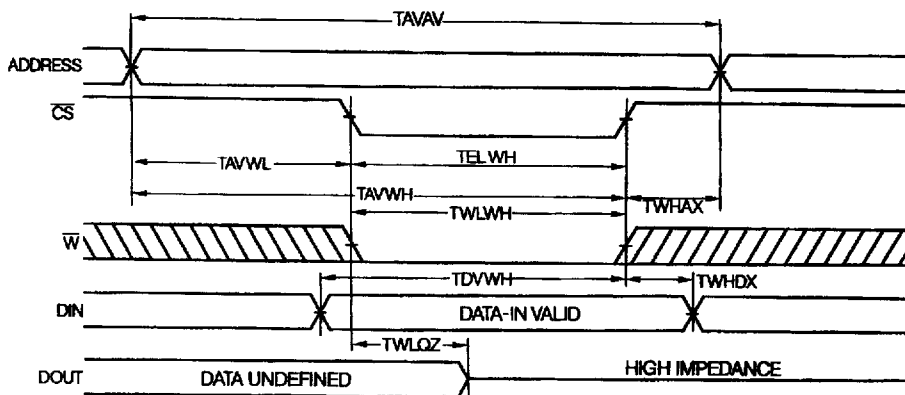
AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)**Conditions :**

VCC	5V $\pm$ 10 %
Input pulse levels	Gnd to 3.0V
Input rise	5 ns
Input timing reference levels	1.5V
Output loading IOL / IOH	+ 30 pF
Operating temperature	- 55°C to + 125°C

WRITE CYCLE :

SYMBOL	PARAMETER (8)	65789 H	65789 K	65789 M	65789 N	UNIT	VALUE
TAVAV	Write cycle time	20	25	40	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	20	25	30	ns	min
TDVWH	Data set-up time	10	15	25	30	ns	min
TELWH	$\overline{CS}$ low to write end	20	25	30	40	ns	min
TWLQZ (7)	Write low to high Z	7	10	15	20	ns	max
TWLWH	Write pulse width	15	20	20	25	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (7)	Write high to low Z	5	5	5	5	ns	min

- Notes :**
- 7. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
 - 8. All parameters tested only.
All parameters are screened during full speed functional test.
For subgroups 7 and 8 (functional test).
Tested at 1 MHz with VIL = 0V and VIH = 3V.
HM 65789 is verified with different patterns unit for basic function, latch-up, maximum rating, data-retention.

WRITE CYCLE 1 : $\overline{W}$ CONTROLLED (note 9)WRITE CYCLE 2 : $\overline{CS}$ CONTROLLED (note 9)

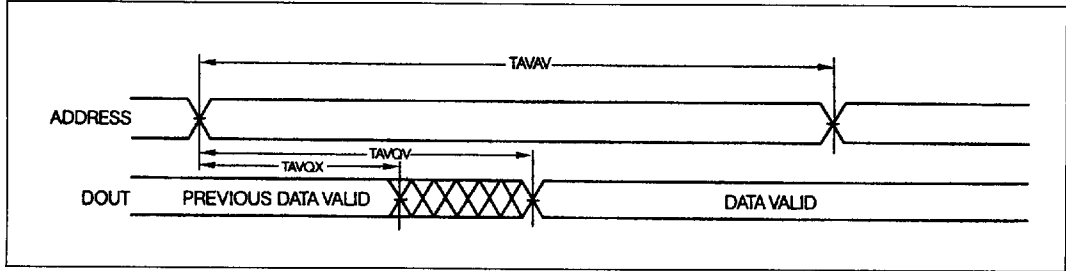
Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data-out will be high impedance if $\overline{OE} = V_{IH}$

READ CYCLE :

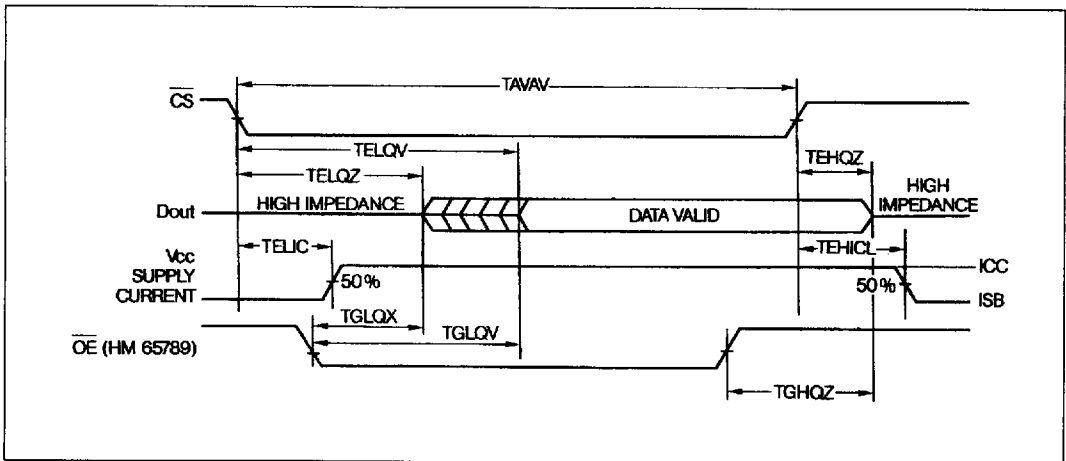
SYMBOL	PARAMETER (8)	65789 H	65789 K	65789 M	65789 N	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	15	15	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	30	ns	max
TGLQV	Output enable access time	12	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	12	15	15	ns	max

Note 8 : All parameters tested only.
 All parameters are screened during full speed functional test.
 For subgroups 7 and 8 (functional test).
 Tested at 1 MHz with $V_{IL} = 0V$ and $V_{IH} = 3V$.
 HM 65789 is verified with differents patterns unit for basic function, latch-up, maximum rating, data-retention.

READ CYCLE nb 1 (notes 10,11)



READ CYCLE nb 2 (notes 10, 12)

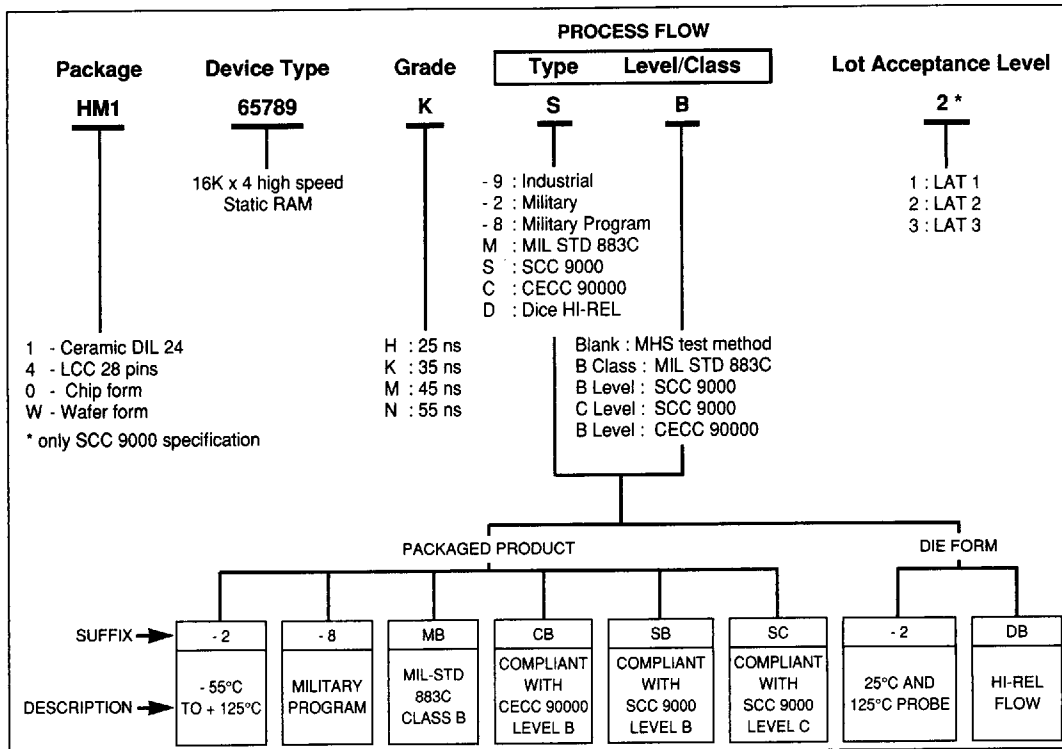


Notes : 10. $\overline{W}$ is high for read cycle.

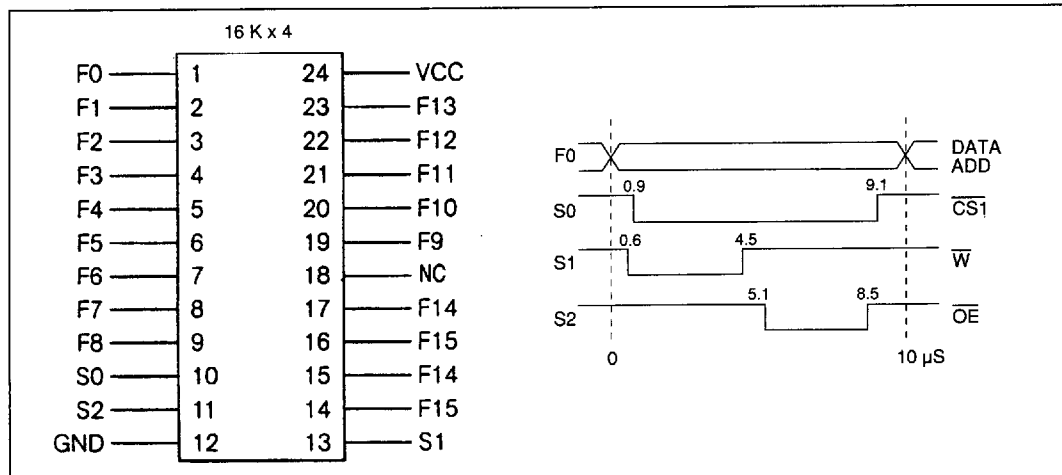
11. Device is continuously selected, $\overline{CS} = \text{VIL}$, $\overline{OE} = \text{VIL}$.

12. Address valid prior to or coincident with $\overline{CS}$ transitive low.

ORDERING INFORMATION



BURN IN SCHEMATICS



VCC = 5.5 V

R = 1KΩ per pin

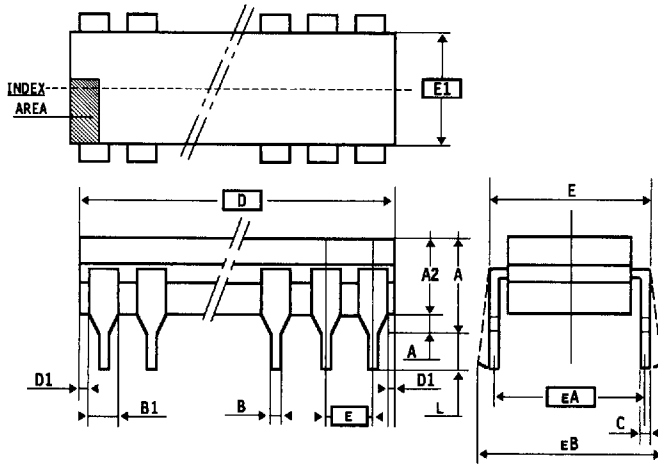
F0 = 50 KHz ± 20 %

Fn = 1/2 F n-1

S0 & S1 & 2S2 : programmable signals for write / read cycles

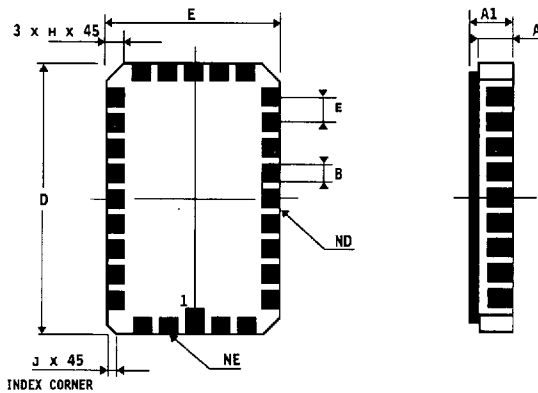
MHS
 electronic

PACKAGE OUTLINES



24 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	D1
MM	MIN	—	0.50	3.81	0.36	0.76	0.20	31.50	0.76	7.90	7.24	2.54	7.62	—	3.17
	MAX	5.71	—	4.95	—	1.78	0.38	32.26	—	8.38	7.87	BSC	BSC	10.92	5.08
INCHES	MIN	—	.020	.150	.014	.030	.008	1.240	.030	.311	.285	.100	.300	—	.125
	MAX	.225	—	.195	—	.070	.015	1.270	—	.330	.310	BSC	BSC	.430	.200



28 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER

		A	A1	B	D	E	e	h	j	ND	NE
MM	MIN	1.37	1.62	0.56	13.81	8.74	1.27	0.64	0.38	9	5
	MAX	1.65	2.00	0.71	14.22	9.14	BSC	Ref	Ref	9	5
INCHES	MIN	.054	.064	.022	.544	.344	.050	0.25	.015	9	5
	MAX	.065	.079	.028	.560	.360	BSC	Ref	Ref	9	5