The switching threshold at inputs DI and ENA can be adjusted between 1.5 V and 7 V via connection TS:

$V_{TS} = 0$ V; input threshold = 1.5 V (for 5 V logic)
$V_{TS} = 0$ to 5 V; input threshold = $V_{TS}$ +1.5 V
$V_{TS} = V_S$: input threshold = 7 V (for 12/15 V and 24/28 V logic)

If the output is disabled due to the logic states of inputs DI or ENA this disable is effective over the total supply voltage range between $V_S = 0$ V and $V_S = 35$ V.

The inputs are protected with clamp diodes.

**Maximum Ratings**

| Description | Symbol | min | max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage | $V_S$ | −0.3 | 35 | V | |
| Supply voltage | $V_S$ | −0.3 | 45 | V | 100 ms duration, 1 s interval |
| Input voltage at DI and ENA | $V_{DI, ENA}$ | −0.3 | 35 | V | 1) |
| Voltage at TS and SQ | $V_{TS, SQ}$ | −0.3 | 45 | V | |
| Output voltage $V_Q$ and voltage at C | $V_Q$, $V_C$ | −0.3 | $V_S$ | V | |
| Voltage at W | $V_W$ | −0.5 | $V_S$ | V | 2) |

## Characteristics

Supply voltage $4.5\ V \leq V_S \leq 30\ V$

FZL 4141 D $0\,°C \leq T_A \leq +70\,°C$

FZL 4145 D $-25\,°C \leq T_A \leq +85\,°C$

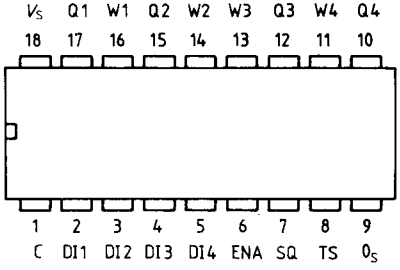
| Description | Symbol | Test conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply current | $I_S$ | $V_{ENA} = 0\ V$, $V_W = V_S$ | | 6 | 8.5 | mA |
| H input voltage at DI, ENA | $V_{IH}$ | $V_{TS} = 0\ V$ | 2 | | | V |
| H input voltage at DI, ENA | $V_{IH}$ | $V_{TS} = V_S$ | 8 | | | V |
| L input voltage at DI, ENA | $V_{IL}$ | $V_{TS} = 0\ V$ | | | 0.7 | V |
| L input voltage at DI, ENA | $V_{IL}$ | $V_{TS} = V_S$ | | | 6 | V |
| Input current at DI, ENA | $I_{DI,ENA}$ | $0.5\ V \leq V_{DI,ENA} \leq 30V$ | 50 | | 200 | µA |
| L output voltage at SQ | $V_{SQL}$ | $I_{SQ} = 5\ mA$ | | | 0.5 | V |
| Output current available[1] | $I_Q$ | $V_Q = V_S - 1.5\ V$ | 1.5 | 2.5 | | mA |
| | $I_Q$ | $T_A = 0\,°C$, $V_Q = V_S - 1.5\ V$ | 1.7 | | | mA |
| Current from TS | $-I_{TS}$ | $V_{TS} = 0\ V$ | | 2 | 10 | µA |
| Switching threshold at W | $V_W$ | | $V_S - 0.6$ | $V_S - 0.5$ | $V_S - 0.4$ | V |
| Current in W | $I_W$ | | | | 100 | µA |
| Current from C | $-I_C$ | $T_A = 20\,°C$ | 12 | 20 | 34 | µA |
| Current in C | $I_C$ | $T_A = 20\,°C$ | 0.6 | 1 | 1.7 | mA |
| Upper switching threshold at C | $V_{CU}$ | $T_A = 20\,°C$ | 1.6 | 2.1 | 1.7 | V |
| Lower switching threshold at C | $V_{CL}$ | $T_A = 20\,°C$ | 0.6 | 0.9 | 1.2 | V |
| Saturation voltage at T[2] | $V_{QR}$ | $V_W = V_S - 2V$, $I_Q = 0$ | | $V_S - 0.3$ | | V |
| H output voltage | $V_{QH}$ | $V_{ENA} = 0\ V$ | $V_S - 0.25$ | $V_S - 0.02$ | | V |

[1]) The actual output current is typically 0.5 mA higher, a value which is required as current for the short-circuit protection. However, only the value specified above is available to drive the external output transistors.

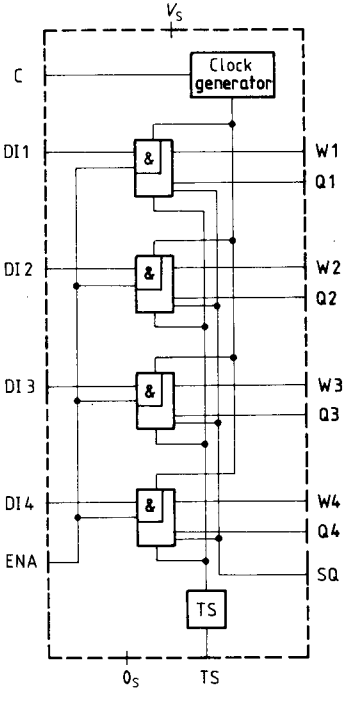
[2]) See block diagram

## Pin Configuration

top view

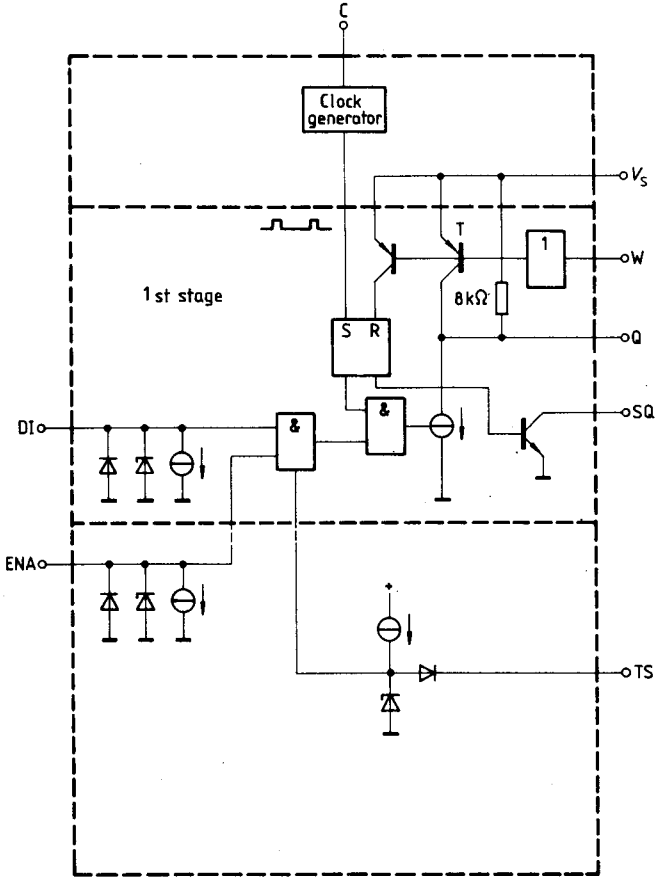



## Block Diagram



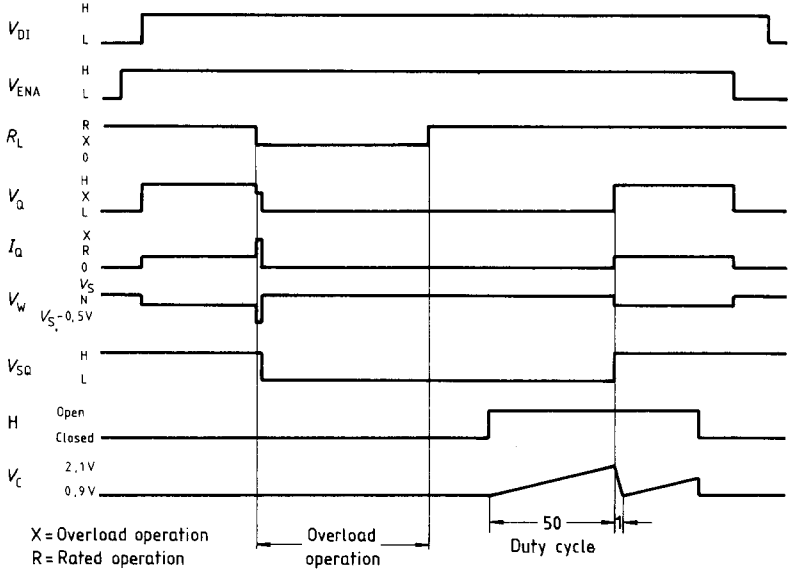

DI Driver input
ENA Enable input
C Clock capacitor
Q Output
TS Input for threshold switching
W Input for output current limiter
SQ Signaling output

**Schematic Circuit Diagram of One Stage**

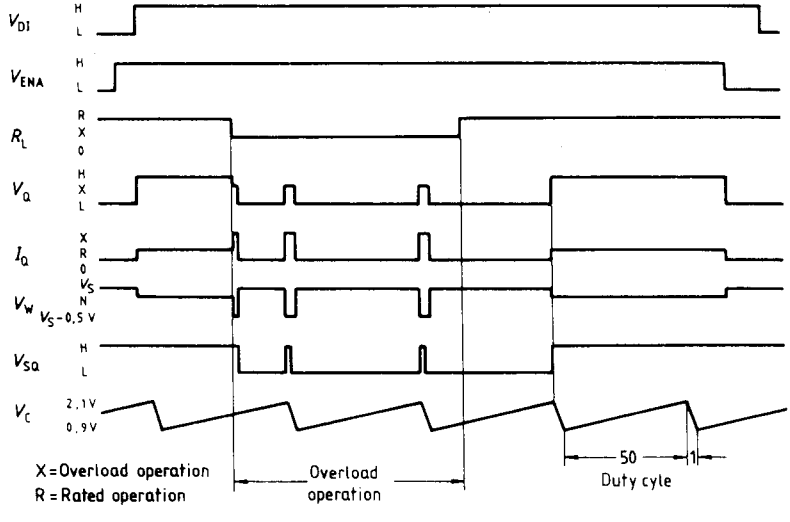



DI Driver input
ENA Enable input
C Clock capacitor
SQ Signaling output
Q Output
TS Input for threshold switching
W Input for output current limiter

**Mode of Operation: Switching-On again after Overload with Key H**




**Mode of Operation: Automatic Switching-On again after Overload**



**Typical Application Circuits**

The load conditions at Q depend on the permissible power dissipation of the power transistors used. The pulsed power dissipation in case of a short circuit must be observed.

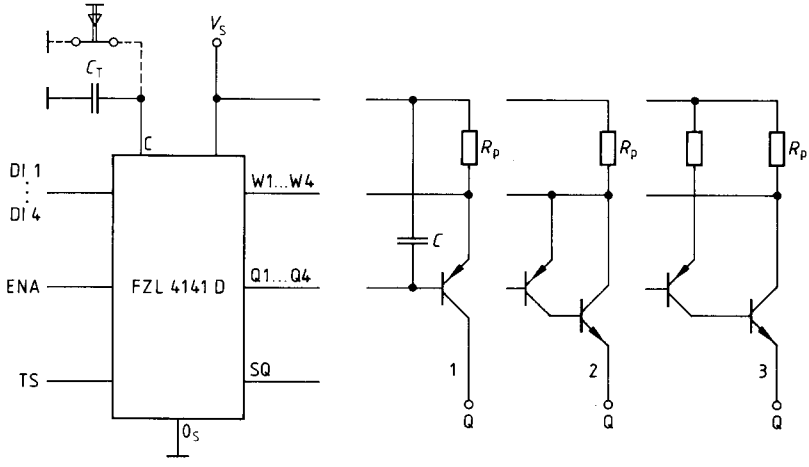
In order to suppress oscillations of the power stage in case of a short circuit, a capacitor C at Q 1 to Q 4 is necessary if e.g., fast switching transistors are used.

Typical value C approx. 20 nF.

The output circuit 1 is suited for currents up to approx. $I_Q = 100$ mA.

The output circuits 2 and 3 are suited for currents up to approx. $I_Q = 2$ A. A minimum power dissipation can be achieved with circuit 3.

A break key in parallel to $C_T$ allows a manual switch-on in case of short circuit.



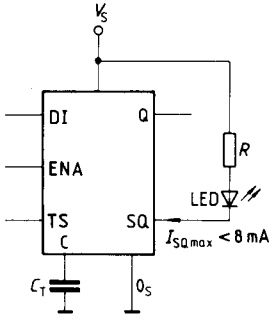

$R_P$ = Precision resistor (current measurement)
$C_T = 0.8 \times t_p$ ( nF, µs)
$t_p$ = Short-circuit current pulse length

**Note**

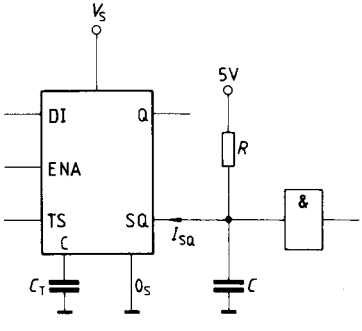
Circuit 1 does not permit a capacitor between Q 1 and Q 4 and the collector.
Circuit 2 does not permit a capacitor between Q 1 and Q 4 and base or emitter, respectively.
Otherwise too high current spikes would arise in case of a short circuit.

## Typical Application of Short-Circuit Signaling Output SQ

### 1. LED Display




### 2. TTL/CMOS/LSL Driving




If the pulses that appear at SQ during clocked operation disturb the remainder of the circuit, a lowpass filter will be necessary. For a load current of $I_{SQ} = 1$ mA a capacitor $C$ of approx. 10 nF is necessary to limit the output pulses of up to 10 µs (depending on $C_T$) to 1 V. Signaling occurs after approx. 50 µs.