256Kx16 Static RAM
High Speed CMOS, Module

Features

256Kx16 bit CMOS Static
Random Access Memory Module

- Fast Access Times:
  20, 25, and 35ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible

High Density Packaging

- 40 Pin DIP, No. 151

Single +5V (±10%) Supply Operation

The EDI8F16257C is a 256Kx16 CMOS Static RAM Module consisting of four (4) 256Kx4 CMOS Static RAMs in plastic chip carriers surface mounted onto a multi-layered epoxy laminate (FR4) substrate.
Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

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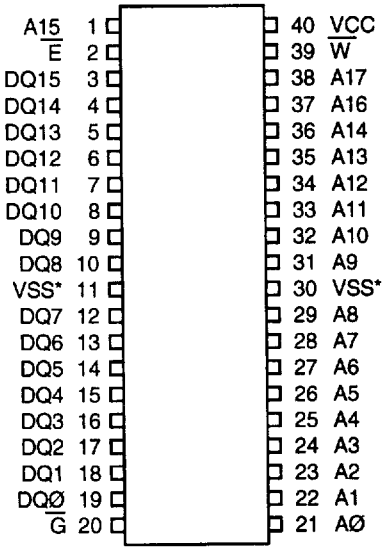
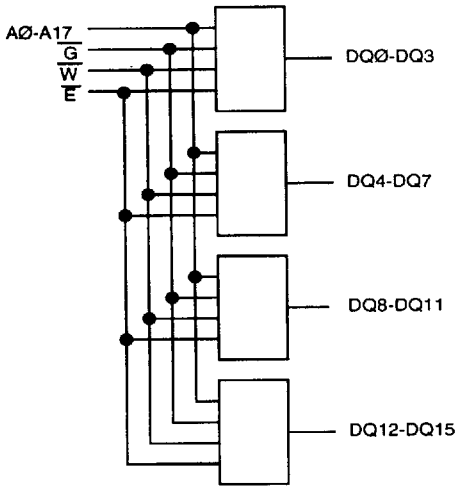
Pin Configurations and Block Diagram



Note: Both ground pins (VSS) need to be grounded for proper operation.

Pin Names

AØ-A17	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ15	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial.	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	4.0 Watt
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	300	720	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL or VIN $\geq$ VIH	--	50	100	mA
Full Standby CMOS Power Supply Current	ICC3	$\overline{E} \geq$ VCC-0.2V VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V	--	5	40	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±40	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC3
L	H	X	Read	DOUT	ICC1
L	L	H	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	35	pF
Capacitance Control (DQ Pins)	CD/Q	15	pF
Input Capacitance ($\overline{E}$, $\overline{G}$)	CC	40	pF
Input Capacitance ($\overline{W}$)	CN	35	pF

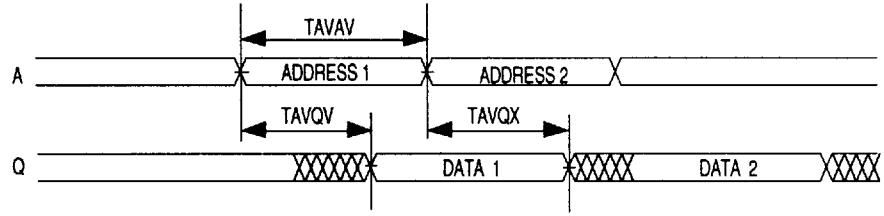
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

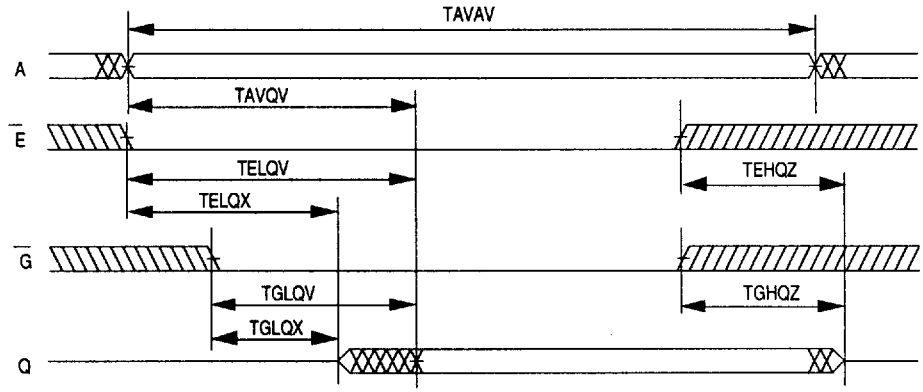
Parameter	Symbol JEDEC	Alt.	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Read Cycle Time	TAVAV	TRC	20		25		35		ns
Address Access Time	TAVQV	TAA		20		25		35	ns
Chip Enable Access Time	TELQV	TACS		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		10		12		20	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		13		15		20	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Enable to Output in High Z (1)	TGHQZ	TOHZ		8		12		20	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

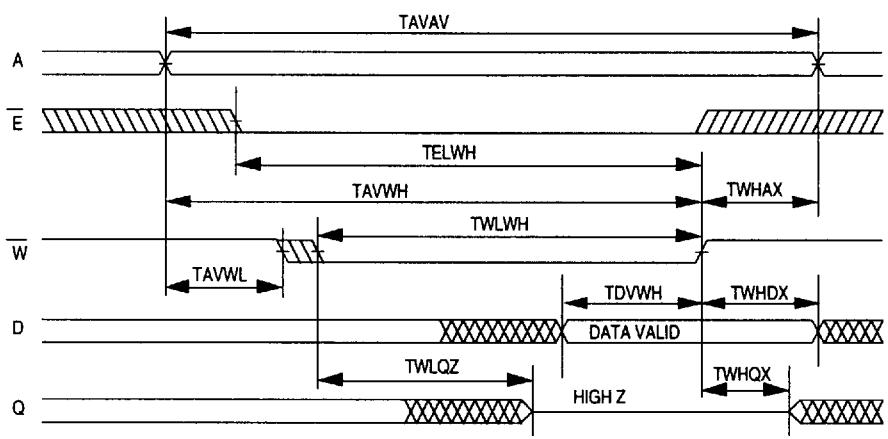


AC Characteristics Write Cycle

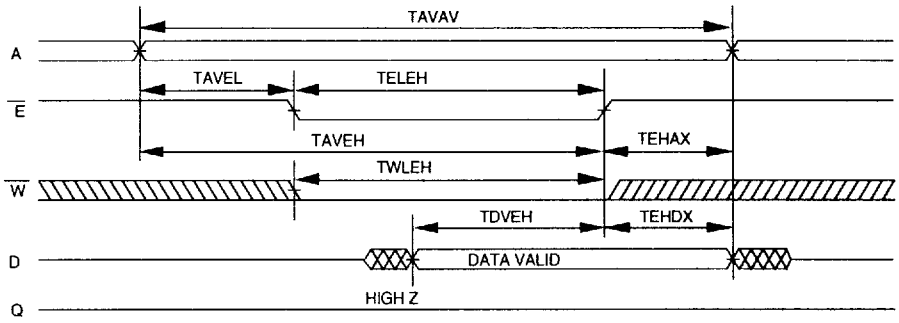
	Symbol		20ns		25ns		35ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	20		25		35		ns
Chip Enable to	TELWH	TCW	15		20		30		ns
End of Write	TELEH	TCW	15		20		30		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to	TAVWH	TAW	15		20		30		ns
End of Write	TAVEH	TAW	15		20		30		ns
Write Pulse Width	TWLWH	TWP	15		20		30		ns
	TWLEH	TWP	15		20		30		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		ns
	TEHDX	TD0	3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	10	0	12	0	15	ns
Data to Write Time	TDVWH	TDW	12		15		20		ns
	TDVEH	TDW	12		15		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 $\overline{E}$ Controlled



Ordering Information

Part Number	Speed (ns)	Package No.
EDI8F16257C20M6C	20	151
EDI8F16257C25M6C	25	151
EDI8F16257C35M6C	35	151

Package Description

Package No.151
40 Pin DIP