SGS-THOMSON MICROELECTRONICS

AN620 APPLICATION NOTE

ON-BOARD PROGRAMMING OF OTP EPROM

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In recent years interest has been growing in On-Board Programming of OTP EPROM memories. There are two main factors which have stimulated this interest: the growth of the FLASH Memory market and the increased use of surface mount packages.

THE GROWTH OF THE FLASH MEMORY MARKET

UV EPROMs and OTP EPROMs offer a higher degree of flexibility compared to Mask ROMs. This is due to their ability to be electrically programed and, in the case of the UV EPROM, erased by exposure to UV light, then re-programed. The ability to electrically program these parts is the most important feature which allows UV EPROMs or OTP EPROMs to be seen by users as ROMs which are programmable at the final moment in the exact quantity required.

Programming of the memories is mainly done by the use of dedicated programing equipment using software algorithms which match those specified by the major chip makers. Fast programming services are also offered by testing houses and by vendors themselves for a small price premium.

The plastic packaged OTP EPROMs are therefore regarded by many as 'flexible ROMs'.

Programming of OTP EPROMs in the application board itself, rather than in the dedicated programming equipment, has not been common until the recent introduction of FLASH Memories. One of the important features of the FLASH Memory is its programability (and erase and re-programability) on board, in the application. With the growth in the use of FLASH Memories today, OTP EPROMs are seen not only as flexible ROMs but now also as low cost FLASH Memory alternatives. For this reason many customers plan to use OTP EPROMs to replace FLASH Memories in low end applications as soon as production levels increase and codes become stable. These OTP EPROMs are mounted on board and thus must be programmed, like the FLASH Memory, in the application.

THE INCREASED USE OF SURFACE MOUNT PACKAGES

While the traditional Dual-In-Line insertion packages, both ceramic and plastic, remain popular, there is a strong trend towards surface mounting PLCC and TSOP types which offer small footprints and easy automatic assembly. The loading of these packages in the dedicated programming equipment and subsequent transfer to the application board, however, presents significant problems and expensive, dedicated handlers are needed. Users therefore prefer to abandon 'off line' programming and chose On-Board Programming techniques.

Programming a UV EPROM or OTP EPROM cell is performed by injecting electrons onto the cell MOS transistor floating gate. A voltage in excess of 6V must be applied to the drain of the cell, together with above 12V on the control gate to get an average energy of the electrons sufficiently large to make them jump the oxide barrier at a significant rate for a fast programming speed.

OBP AND PRODUCT TESTING

When UV EPROM or OTP EPROM products are programmed in dedicated programming equipment the V_{CC} supply voltage is raised to 6V to 6.5V. This level of V_{CC} cannot generally be applied to a board containing the OTP EPROM due to the possible damage to other components. Recent designs of UV EPROM and OTP EPROMs however derive the internal 6V or more used during the write mode from the V_{PP} supply and so are independent of the V_{CC} voltage applied. In fact cell writing can normally take place even if the V_{CC} is 5V or lower.

This feature is not, however, sufficient to guarantee On-Board Programming (OBP) performance. There remains the need to verify the memory content of programmed cells. When the read verify is performed with a 5V V_{CC} supply clearly this ensures that the cells are programmed to logic '0' at least up to 5V, but not more. A high level of confidence remains that the cells, programmed with the internal 6 Volts derived from the 12.75V V_{PP} supply, are in fact over-programmed with a satisfactory margin and would display the correct pattern if verified at above 5V V_{CC}, but to guarantee this to a high quality level is not possible with a read verify at 5V. Just one cell in 4 billion which is harder to program and is marginally written is sufficient to give reject quality of 1000 ppm for 4 Megabit OTP EPROMs!

So the challenge to provide OBP features for OTP EPROMs is not one of programming, but of testing and verification of the programmed pattern. The question that must be answered is "is it possible to guarantee the quality of the memory content when they are programmed at 5V V_{CC} on board?".

RELIABLE OTP EPROMS

The use of OBP for programming UV EPROMs or OTP EPROMs is to related to the confidence in the supplier to deliver a reliable and consistent product. The following section outlines the main issues which have been developed and are used by SGS-THOMSON to build confidence in the product's ability to perform reliably after On-Board Programming has been used.

WAFER LEVEL TESTING

While built-in reliability is obtained for our UV EPROM and OTP EPROM products through robust design, proven and stable processes and extensive characterisation, there are some specific routines that are used to ensure the quality of the product for On-Board Programming.

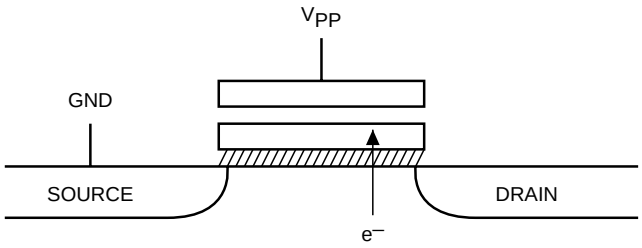
GATE STRESS AND DRAIN STRESS

The integrity of the critical thin oxides is checked by specially developed stress tests, these are performed by applying a fixed voltage to either the control gate (Gate Stress) or to the drains of the cells (Drain Stress). The gate stress is done firstly on the virgin cells (All "1"s) and then on programmed cells (All "0"s). Figures 1, 2, 3 describe the different stresses, the measurements and the specific defects they aim to detect or screen out.

These tests are particularly effective in screening out the chips which are potentially prone to programming errors because the same kind of stresses are applied to the cells during normal write operations. All the cells of the same row share a common word line and when a byte is programmed all those cells not being written, in the row which is at high V_{PP}, are submitted to a gate stress and could evidence the spurious effect of charge gain for virgin cells or charge loss for written cells. A similar argument applies for the cells of a column, biased at the same V_{CC} through the common bit line.

The stress times have been chosen to be equivalent to the total duration of the critical conditions encountered whenever writing of a whole memory pattern occurs.

Figure 1. Gate Stress Testing at Logic '1'

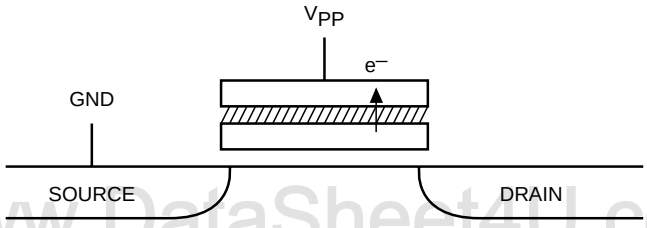


Gate stress, logic '1'
- V_{PP} = 13V
- t = 0.6 sec (≤ 2Mbit)
  t = 1.0 sec (≥ 4Mbit)

Detects 'charge gain' through the gate oxide

AI01342

Figure 2. Gate Stress Testing at Logic '0'

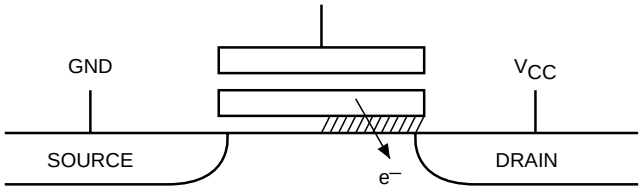


Gate stress, logic '0'
- V_{PP} = 13V
- t = 0.5 sec (≤ 2Mbit)
  t = 1.0 sec (≥ 4Mbit)

Detects 'charge loss' through interpoly oxide

AI01343

Figure 3. Drain Stress Testing at Logic '0'



Drain stress, logic '0'
- V_{PP} = 6.5V
- t = 0.5 sec (256 Kbit)
  t = 1.0 sec (≥ 512 Kbit)

Detects 'charge loss' through gate oxide in the Drain region

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BYTE VERIFY

Each byte used during the wafer level programming sequence is verified for both All "1"s before writing and for the correct pattern after writing. These two checks together ensure that the cells are programmable. Moreover the second check is made at a V_{CC} of 6.5V in MARGIN MODE™, a condition corresponding to such a strong over programming that the cells reaching it (that is the good cells) are definitely NOT hard for writing.

RETENTION BAKE

The flow of the sequence of wafer level testing is shown in Figure 4. The first part ends with the memory matrix fully programmed (All "0"s). The wafers are then submitted to a 48 hour storage at 250°C for a overstress retention bake. During the second test sequence the All "0"s pattern is verified at a V_{CC} of 6.5V and all chips failing the correct pattern, due to cells which have lost their charge, are rejected. This test at 250°C is equivalent to a test of more than 5 years at 70°C operating temperature.

MARGIN MODE VERIFY

The UV EPROM, OTP EPROM and FLASH Memory products of SGS-THOMSON have two different read modes, the normal Read Mode and a special MARGIN MODE which is automatically set during writing. This is a unique feature based on a patent of 1985(1) and a paper given in 1988(2) which disclosed the underlying principle of the design concept. The design uses an off-set current in the sense circuitry to shift the threshold detection for verification of programming of each cell.

The relationship of the array cell current to the current in a reference cell is shown in Figures 5 and 6. Figure 5 shows the normal Read Mode while Figure 6 shows the new MARGIN MODE relationship with the off-set current present which makes the verify of a programmed "0" in the cell at a new higher threshold level. In Figure 5 a threshold shift of 1V is sufficient to make I_{WRITE} lower than I_{REF}, while in Figure 6 for the MARGIN MODE a shift of 2V is needed. This assures a margin of 1V in the programmed threshold, or "0" level, of the cell.

Figure 4. OTP EPROM Testing Flow Chart

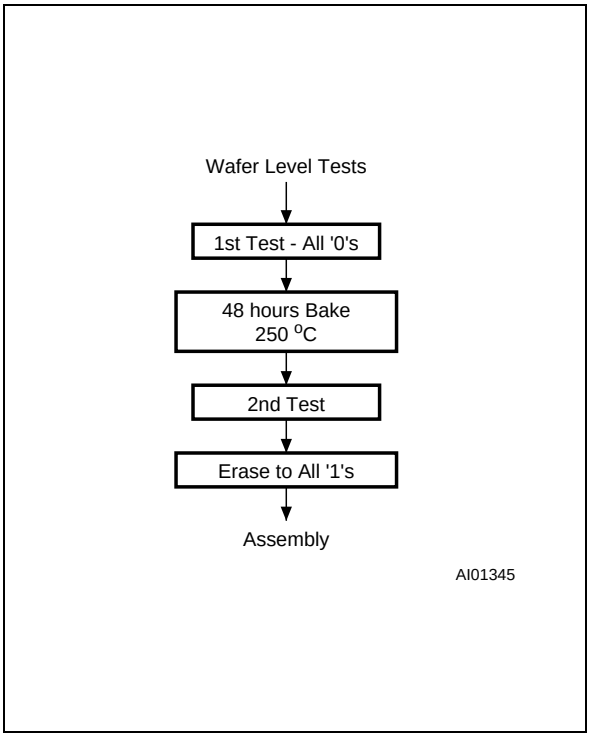
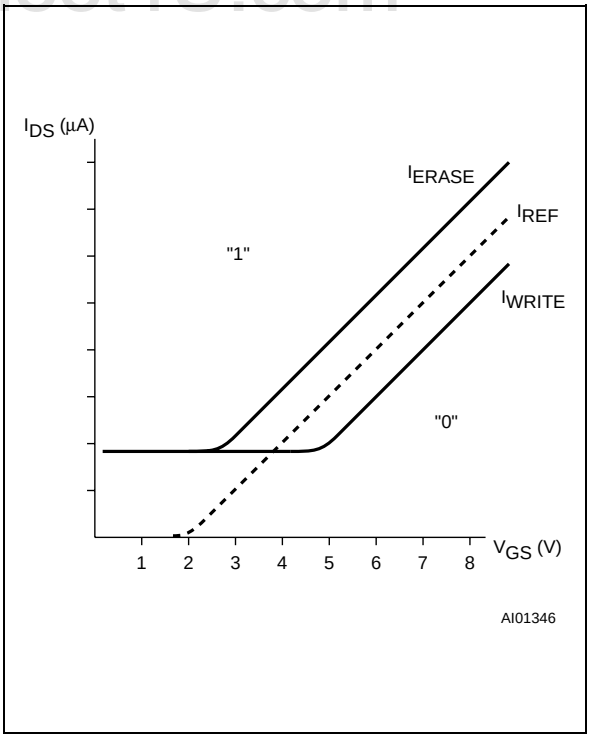


Figure 5. Cell Current in Read Mode



The same concept of MARGIN MODE verify continues to be used in all of the currently produced UV EPROMs and OTP EPROMs, although it is not implemented in the same way. Today's UV EPROMs, OTP EPROM and FLASH Memory products use a more sophisticated concept that allows precise setting of the reference cell current during testing. They have again a programming Verify Mode or MARGIN MODE which is different from the normal Read Mode to ensure a programming margin. Electrical characterisation of the 4 Megabit EPROM products shows that a minimum threshold shift of a cell equal to 2.7V is ensured when they are tested at V_{CC} = 5V in MARGIN MODE, the same result would be guaranteed at a V_{CC} = 6V in Read Mode. Conversely the 5V verify in Read Mode guarantees only a 2.2V shift in the cell threshold, or a programming shift of 0.5V lower. This is illustrated in Figure 7.

In conclusion, programming at V_{CC} = 5V with MARGIN MODE pattern verify automatically gives a programming margin needed to avoid in system noise problems and gives a guarantee of long term pattern stability.

Figure 6. Cell Current in Verify Mode

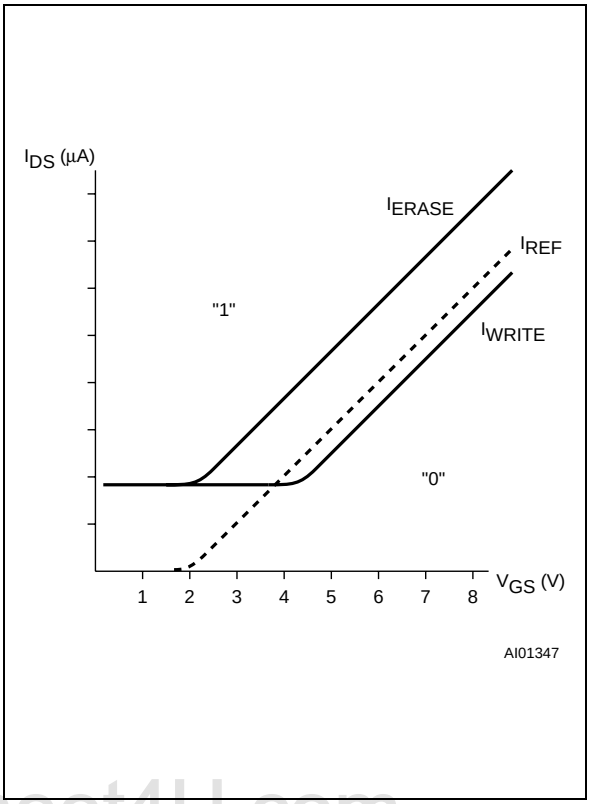


Figure 7. 4Mbit EPROM Threshold Shift

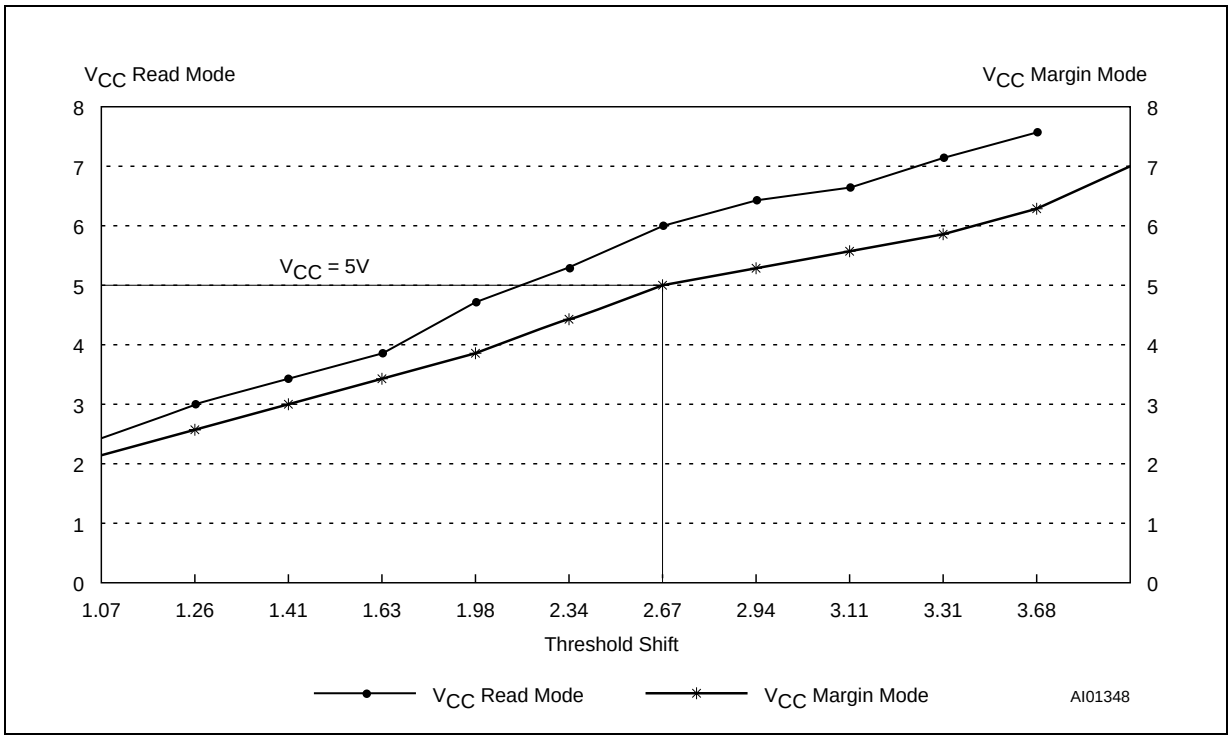


Figure 8. On-Board Programming Flowchart

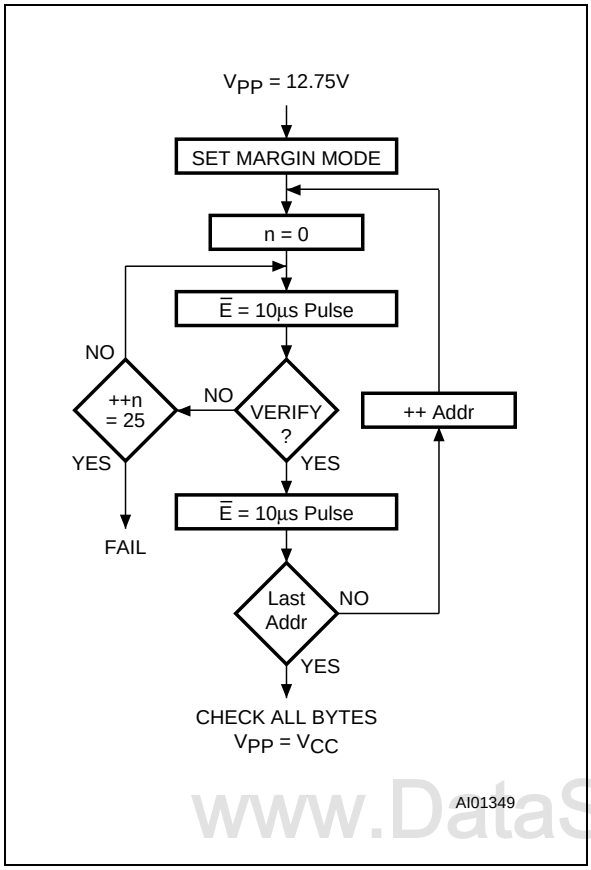
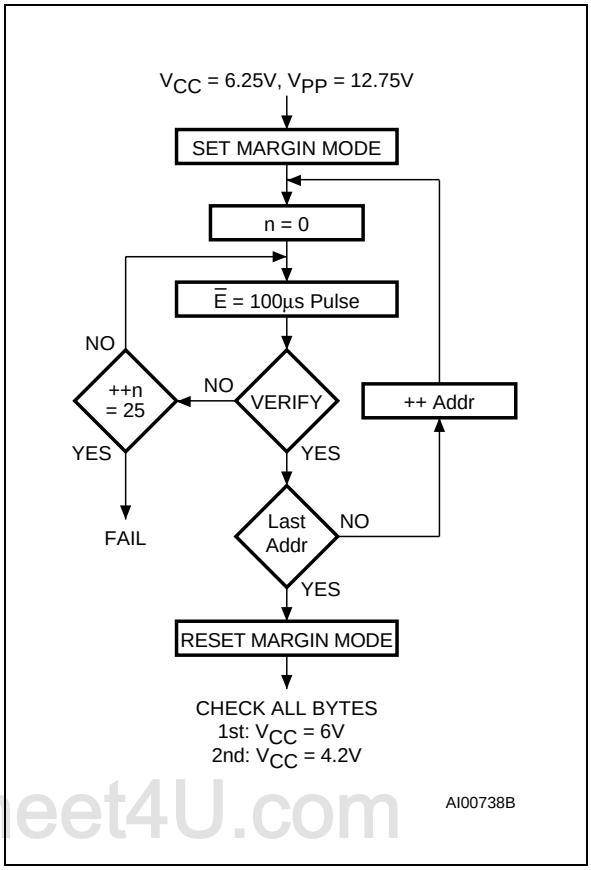


Figure 9. PRESTO II Programming Flowchart



SUGGESTED PROGRAMMING ALGORITHM

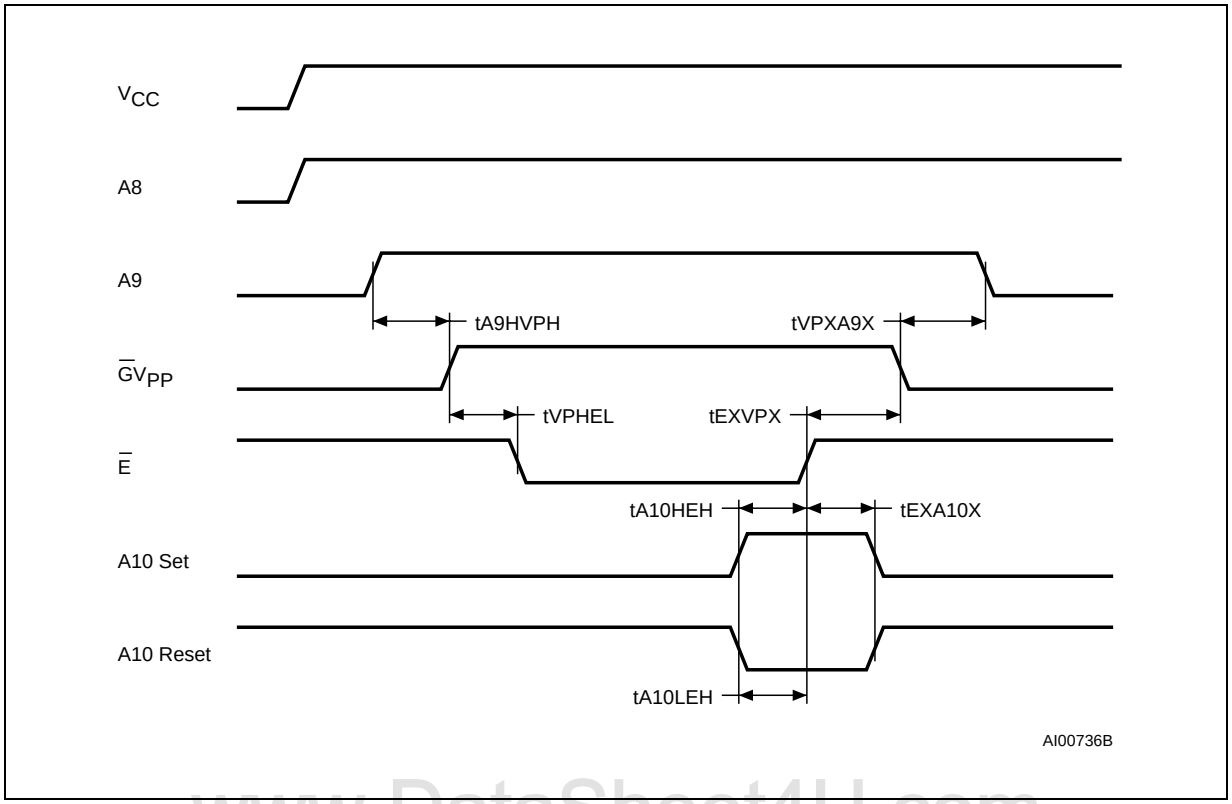
For On-Board Programming, a modified condition of the PRESTO II programming algorithm is used. This algorithm provides a faster, but still reliable programming operation, and is further in line with the in-circuit programming time for the equivalent flash memory device. The standard PRESTO II algorithm is still available for use in device programmers.

Figure 8 shows the new algorithm for On-Board Programming and can be compared to the normal PRESTO II algorithm shown in Figure 9. The new conditions for PRESTO OBP programming are that the applied V_{CC} is now 5V, and the V_{PP} = 12.75V is applied not only during byte-by-byte verify but also during the final pattern verify in order to maintain the read in MARGIN MODE and ensure the cells are all programmed to the MARGIN MODE threshold after the whole programming sequence and have not been affected by any gate or drain stresses that could cause a shift of the programmed charge levels.

The duration of the programming pulse is reduced to 10µs, with a maximum repetition cycle number of 25 in the case of non-validation of the data programmed. A final over-programming pulse of 10µs is needed before the final validation pass of all memory cells in the Margin Mode, but at the 5V(3V) level.

If possible, the V_{CC} applied should be as high as is possible (up to 5.5V for 5V systems, 3.5V maximum for 3V systems) while remaining suitable for other parts in the circuit of the application. As shown previously, a higher V_{CC} provides a higher level of validation of correct programming.

Figure 10. MARGIN MODE Setting AC Waveforms for Products with V_{PP} and $\overline{G}$ on the same pin.



IMPORTANT!

Compatibility Issues

Compatibility issues may arise when using the OTP EPROM to replace a single supply flash memory device (for example, for 4 Megabit devices, the M27C405 OTP EPROM and the M29F040 single supply FLASH Memory). In this case the V_{PP} pin of the M27C405 takes the position of the Write Enable ($\overline{W}$) control input of the M29F040. This pin of the flash memory can only accept normal TTL voltage levels and not the high 12.75V, so care must be taken in the implementation of the design if it is intended to eventually replace the flash memory with OTP EPROM once the contents are stable and production volumes and price pressure require the lower cost alternative OTP EPROM.

In addition, the M27C512 (512K) and M27C801 (8 Megabit) products have to be treated a little differently. In order to make them compatible with the 28 or 32 lead packages these two products share the same pin for V_{PP} and Output Enable ($\overline{G}$). Thus a high V_{PP} level cannot be set for reading, which requires $\overline{G}$ to be Low. For these products the MARGIN MODE must be set by a specific sequence of signals shown in Figure 10 before starting programming and through the final pattern verify.

REFERENCES

(1) *"Device for the verification of the memory cells on the basis of the threshold drop obtainable during writing"*, Giulio Casagrande, Roberto Gastaldi, patent filed with priority date 3/28/85

(2) Roberto Gastaldi et al, "*A 1 Mbit CMOS EPROM with enhanced verification"*, IEEE Journal of Solid State Circuits, Vol 23, No 5, October 1998