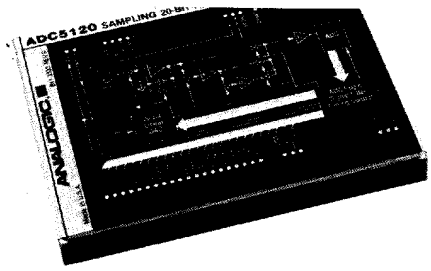
ANALOGIC®
The World Resource for Precision Signal Technology



ADC5120

Wide Dynamic Range Oversampling A/D Converter

Performance Features

The ADC5120 is a 20-bit, sampling A/D converter with a differential input. It has a data update rate of 48 kHz and a sampling rate of 144 kHz for a guaranteed minimum of 3X oversampling over a DC to 20 kHz bandwidth. The ADC5120 was designed for use in spectroscopic and professional digital audio applications where wide dynamic range, low noise and low distortion are required. It will digitize the input signal at a 144 kHz rate and pass the data through an FIR filter and decimator to produce a 20-bit, 48 kHz result with a signal-to-noise ratio of 105 dB. The data is available as 2's complement in two formats; parallel data in three 8-bit bytes and serial data that conforms to AES/EBU standards. The AES/ EBU interface has been designed so that two converters can drive the same data line to form a stereo data frame.

The ADC5120 is an easy to use, cost effective solution for professional digital audio workstations. It integrates an input differential amplifier with a single pole filter, a low distortion, low noise sample-and-hold amplifier containing a second single pole filter, a proven three pass, 18-bit sub-ranging A/D converter, a stable precision reference, a decimating FIR filter with AES/EBU serializer all in a fully shielded 3" x 4" package.

(cont. on pg. 3)

Features

- 20-Bit Data Output
- 48 kHz Data Update Rate
- 144 kHz Sampling Rate
- 3X Sampling Rate
- On Board FIR Filter
- 105 dB Signal to Noise Ratio
- -110 dB Peak Distortion
- AES/EBU Data Formats
- TTL Compatibility
- Electromagnetic/Electrostatic Shielding

Applications

- Professional Digital Audio
- Spectroscopy

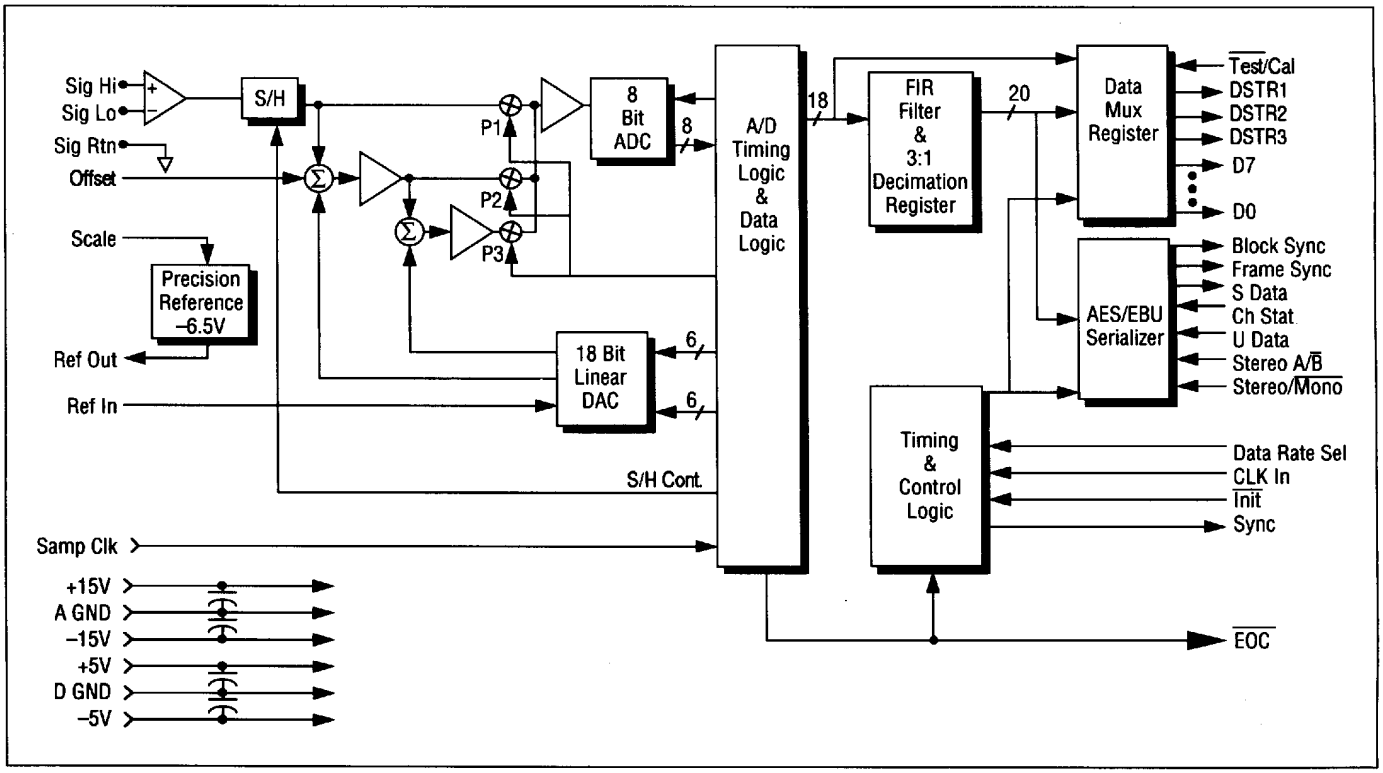


Figure 1. ADC5120 Functional Block Diagram.

ADC5120 SPECIFICATIONS (1)

T-51-10-90

ANALOG INPUT

Configuration	Differential
Input Voltage Range	±5V
Input Bias Current	500 nA
Offset Current	20 nA
Differential Impedance	4 kΩ
Input Capacitance	10 pF
Max. Input Without Damage	±18V
Common Mode Rejection	80 dB Min. @ DC

DIGITAL INPUTS

Logic Levels, TTL	
Logic "0"	0.8V Max.
Logic "1"	2.0V Min.
Logic Currents	
Logic "0"	-0.4 mA
Logic "1"	20 µA
$\overline{\text{INIT}}$ Pulse width	350 ns Min., Active "low"
SAMPCLK Pulse Width(2)	50 ns Min., Positive edge triggered
Rate for 44.1 kHz Update	132.3 kHz
Rate for 48 kHz Update	144 kHz
Clock Frequency(2)	
44.1 kHz Update Rate	11.2896 MHz
48 kHz Update Rate	12.288 MHz

DIGITAL OUTPUTS

Fan-Out	1 TTL Load
Logic "0"	0.4V Max
Logic "1"	2.4V Min.
End of Conversion	High During Conversion
Output Coding	2's Complement Offset Binary

INTERNAL REFERENCE

Voltage	-6.5V Typ.
Stability	±5 ppm/°C Typ.
Available Current	1 mA Max. , load to remain stable during conversion
Ref. Input Impedance	720µ ll 10 µF, -1.5 mA Typ.
Ref. Input Without Damage	+0.5V to -8.5V

DYNAMIC CHARACTERISTICS

Throughput Rate	1/3 Sampling Rate
Max. Sampling Rate	144 kHz Min.
A/D Conversion Time	4.8 µs Typ.
S/H Acquisition Time	2.1 µs Typ.
S/H Aperture Delay	30 ns Typ., 60 ns Max.
S/H Feedthrough (3)	-90 dB Max., -95 dB Typ.
Full Power Bandwidth	25 kHz Min.
Small Signal Bandwidth	142 kHz Typ.
1 kHz @ -1 dB	
Signal to Noise Ratio (4)	103 dB Typ., 100 dB Min.
Peak Distortion (5)	-110 dB Typ., -102 dB Max.
Total Harmonic Dist. (6)	-105 dB Typ., -98 dB Max.
1 kHz @ -15 dB	
Signal to Noise Ratio (4)	89 dB Typ., 86 dB Min.
Peak Distortion (5)	-104 dB Typ., -99 dB Max.
Total Harmonic Dist. (6)	-94 dB Typ., -90 dB Max.

TRANSFER CHARACTERISTICS

Data Output	20 Bits
Monotonicity	Guaranteed
Offset Error	±2 mV Max.
A/D Gain Error	±0.02 % FSR Max.
Filter Error	-0.1% FSR Max. @ 48 kHz -0.4% FSR Max. @ 44.1 kHz
Phase Linearity	0.053 Degrees
Phase Delay	8.0 ±0.2 Degrees

FIR FILTER CHARACTERISTICS

Gain Flatness	±0.05 dB DC to 20 kHz
Stop Band	-75 dB Max. @ 28 kHz to 116 kHz

STABILITY (0 C to +60°C)

Diff. Non-Linearity TC	±0.5 ppm/°C Typ.
Offset TC	±10 ppm/°C Typ.
Gain TC	±5 ppm/°C Typ.
Warm-Up Time	5 Min. Typ.
Supply Rejection / % change in any supply	
Offset	±5 ppm FSR Typ.
Gain	±5 ppm FSR Typ.

POWER REQUIREMENTS

Supply Range	
±15V Supplies	11.65V Min., 15.45V Max.
±5V Supplies	4.75V Min., 5.25V Max.
Current Drain	
+15V	55 mA Typ.
-15V	55 mA Typ.
+5V	75 mA Typ.
-5V	70 mA Typ.
Total Power Consumption	2.38 W Typ.

ENVIRONMENTAL - MECHANICAL

Specified Temp. Range	0°C to +60°C
Storage Temp. Range	-40°C to +80°C
Relative Humidity	0 to 85 % Non-condensing up to 60°C
Dimensions	
Inches	3 x 4 x 0.44
Millimeters	7.62 x 12.7 x 1.1
Shielding	
Electromagnetic	5 sides
Electrostatic	6 sides
Case Potential	Ground

NOTES:

1. All specifications guaranteed at 25°C and power supplies at ±15V and ±5V unless otherwise noted.
2. SAMP CLK and clock must be phase locked.
3. Measured with a full scale 20 kHz sinewave.
4. Signal to Noise ratio represents the ratio of the rms value of the signal to the total rms noise from DC to 24 kHz.
5. Peak distortion represents the ratio of the highest spurious frequency component below the Nyquist rate to the signal.
6. Total harmonic distortion represents the ratio of the rms sum of all harmonics up to the 100th harmonic to the rms value of the signal. Measured over a DC to 24 kHz bandwidth.

Performance Features (cont.)

The on-board filtering and 3X oversampling virtually eliminate the input anti-aliasing filter requirements. Superior performance and ease of use make the ADC5120 the ideal professional digital audio workstation solution. Having all the required building blocks integrated into a single package benefits the system designer in two ways. First, all critical circuits have been designed to complement the performance of the A/D converter; for example, the S/H amplifier acquisition time, Hold mode settling and droop rate have been optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves optimal performance, avoiding degradation due to ground loops, signal coupling, jitter and digital noise introduced when individual components are interconnected. Furthermore, the accuracy, speed, and quality of the ADC5120 are fully ensured by thorough, computer controlled factory tests of each unit.

Layout Considerations

Because of the high resolution of the ADC5120 A/D converter, it is necessary to pay careful attention to the printed circuit layout for the device. It is for example, important to separate analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or "glitchy", and these glitches can have adverse affects on the performance of the ADC5120 if they are introduced to the analog portions of the A/D converter's circuitry. Any noise in the analog ground return can result in erroneous or missing codes resulting in signal distortion. It is therefore important to configure a low-impedance ground-plane return on the printed-circuit board. This is the point where the analog and digital power returns should be made common, NOT at the supplies. Note that the ground-potential metal case used for the ADC5120 provides shielding against electromagnetic interference on 5 sides and against electrostatic interference on 6 sides.

ADC5120 SPECIFICATIONS

Coding and Trim Procedure

Frequency domain applications such as digital audio, generally do not require offset and gain adjustments beyond the accuracies stated in the specifications. If better accuracy is required in a stereo application to match channels A and B, refer to figures 2 and 3 for the ADC5120 coding and trim procedure. Figure 2 shows the external Offset and Gain Adjust configuration. Figure 3 shows the output 2's complement Offset Binary coding of the ADC5120 A/D converter.

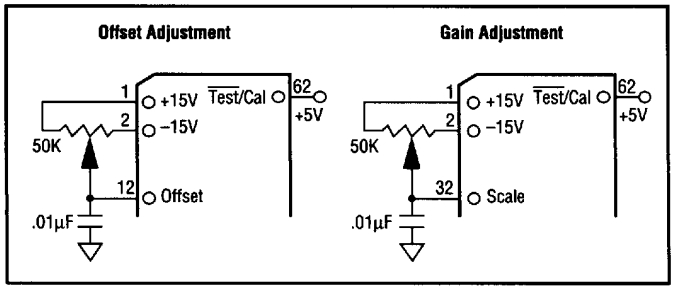


Figure 2. External offset and gain adjust configuration

To trim the offset and gain of the ADC5120, the internal FIR filter and decimator must be bypassed. It is the "raw" 18-bit data out of the ADC that is calibrated. This can be done by applying a logic "1" to the TEST/CAL pin #62. In this mode, the 18-bit data is presented at DATA OUT at the full SAMPCLK conversion rate. Bits 19 & 20 can be ignored at this time.

To trim the offset of the ADC5120, apply -19 µV to the analog input. Adjust the external trim potentiometer such that each of the 18 bits alternates equally between "0" and "1". To trim the gain of the ADC5120, apply -4.999981V to the analog input and adjust the external gain trim potentiometer such that the MSB is "1", Bits 2-17 are "0", and the LSB (Bit 18) alternates equally between "0" and "1".

Using the setup as described in figure 2, the sensitivity of the offset adjustment is typically 13 LSBs per volt, 26 LSB's per volt for gain. Utilizing a ±10V DAC in place of the potentiometers is an alternative method of trimming.

Timing Considerations

The timing diagrams of figures 4 and 5 show the timing characteristics of the ADC5120 A/D converter. To begin the operation, INIT IN must be low in coincidence with a minimum of 4 clock pulses to set the internal logic to a known state. Once INIT returns high, SAMPCLK can be applied and begin converting. It must be phase locked with CLOCK IN. After 65 conversions, SYNC OUT falls "low" indicating synchronization, when in the stereo mode. Also at this time BLOCK SYNC and FRAME SYNC go "high" indicating the beginning of subframe "A" and the first of a 192 frame AES/EBU block. A "high" at BLOCK SYNC indicates frame 1; a "high" at FRAME SYNC indicates channel "A" serial data is being transmitted.

ANA INPUT	OUTPUT CODE	
	MSB	B18
+4.999990 V =	01111111111111111111XX	
0.000000 V =	00000000000000000000XX	
-5.000000 V =	10000000000000000000XX	

Figure 3. Output Coding for the ADC5120.

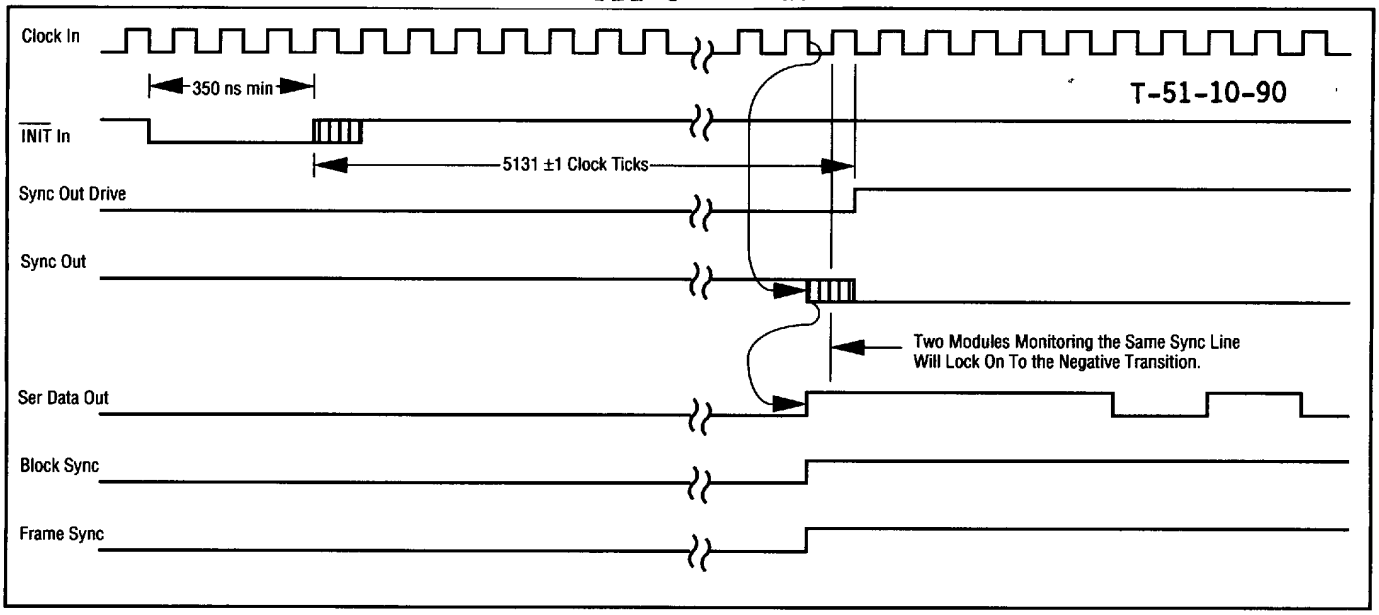


Figure 4. ADC5120 Initialization/Sync Timing.

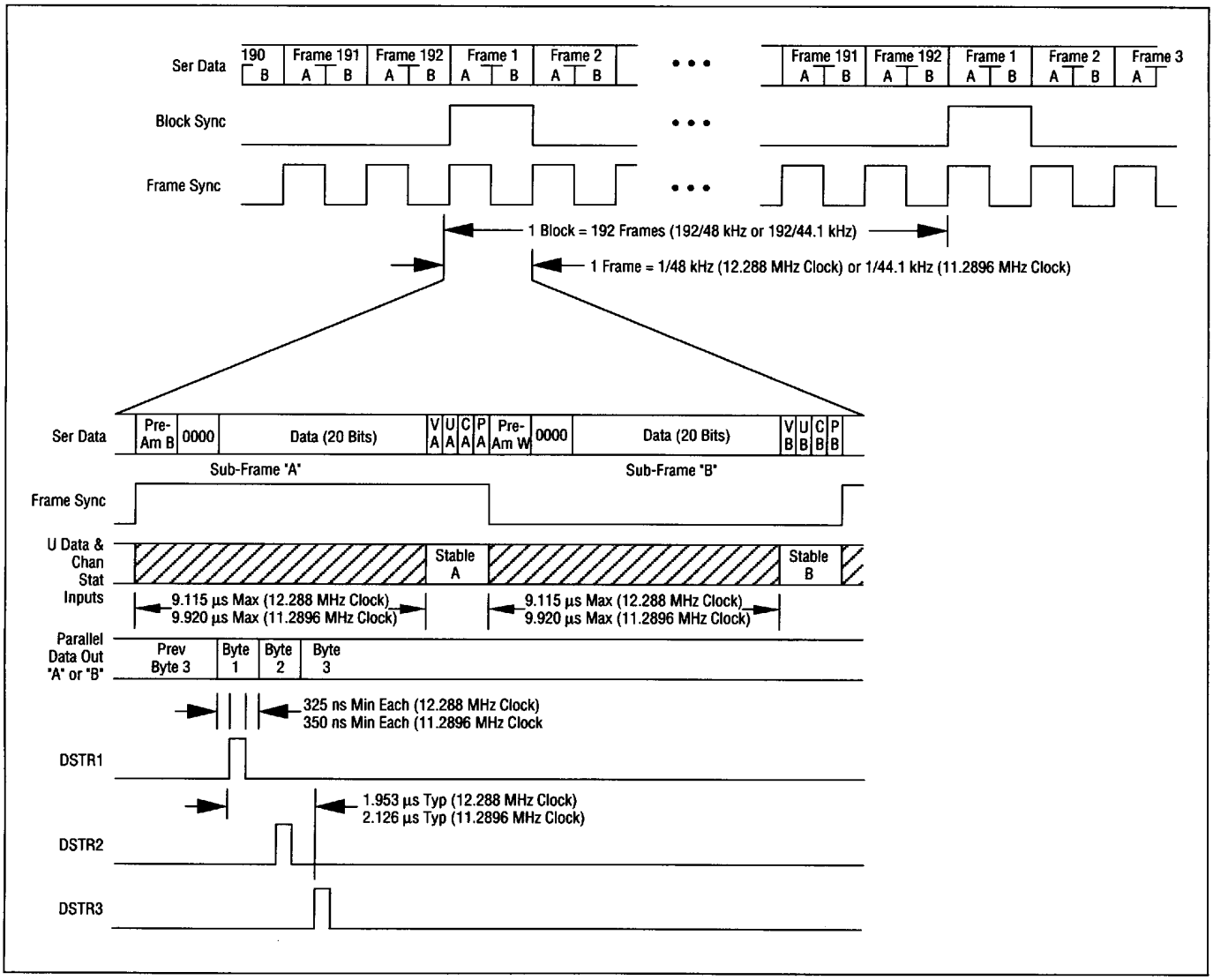


Figure 5. AES/EBU Block & Frame Timing; User Data & Channel Status Input Timing; Parallel Data & Data Strobe Timing.

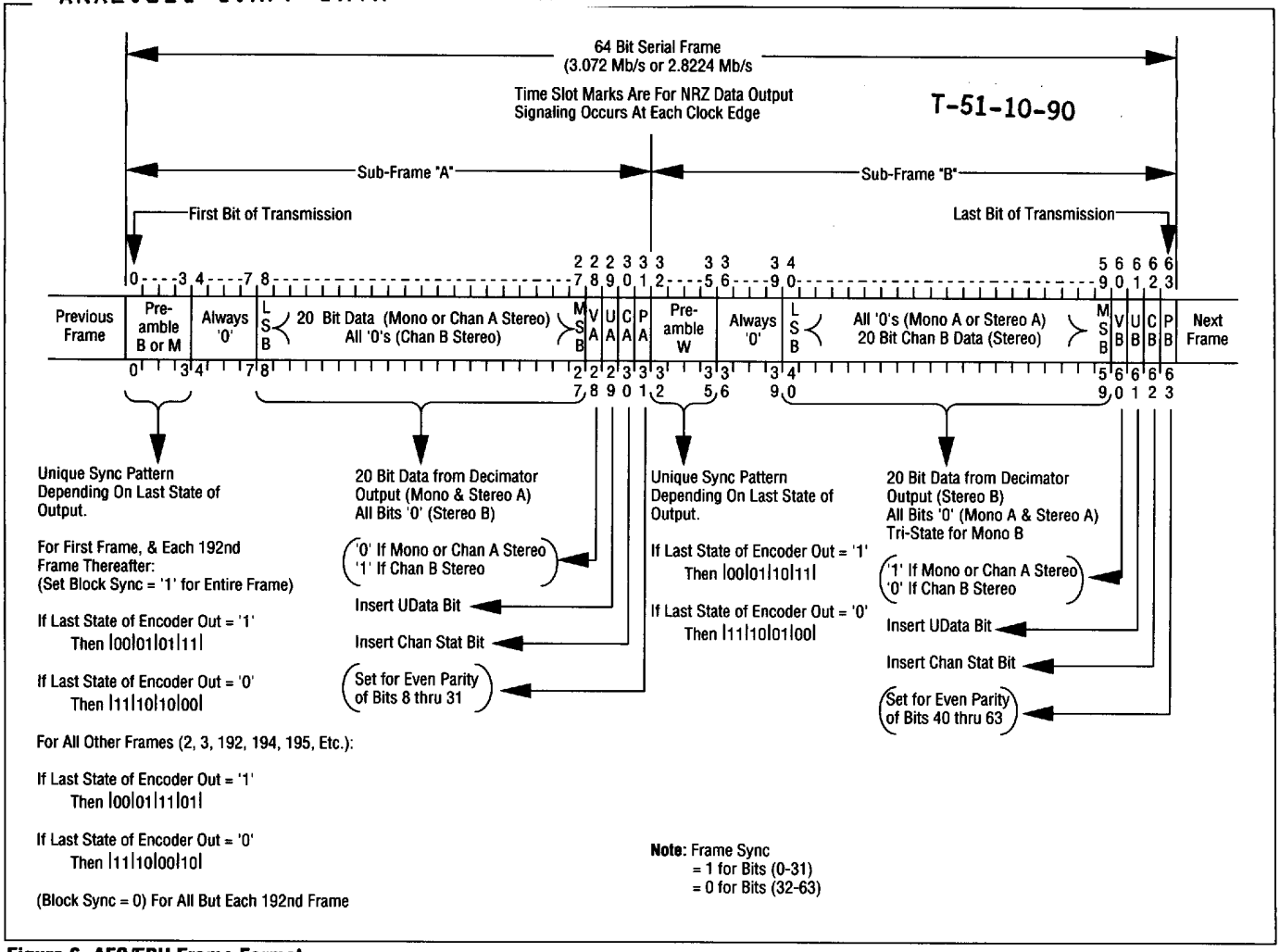


Figure 6. AES/EBU Frame Format.

PRINCIPLES OF OPERATION

To understand the operating principles of the ADC5120 A/D converter, refer to the timing and interface figures of 4 through 9. The front end of the ADC5120 is a low-noise, low distortion Sample-and-Hold amplifier with a differential input single-pole filter. The heart of this unique A/D converter is an 18-bit, 3-pass sub-ranging ADC. All the timing and logic for the A/D converter, the FIR filter, 3:1 decimation register, and AES/EBU serializer are all contained in a single gate array.

The internal 18-bit ADC will convert at a rate determined by the SAMPCLK input; 144 kHz for a 48 kHz update rate and 132.3 kHz for a 44.1 kHz update rate or three times the required data update rate. The coefficient of the internal FIR filter changes with the data rate therefore the DR SELECT pin must have the correct logic applied; "high" for 44.1 kHz, "low" for 48 kHz. The SAMPCLK must be preceded by an initialization ($\overline{INIT}$) command to set the internal logic state to a known start up condition. All SAMPCLK commands are ignored until $\overline{INIT}$ returns "high". $\overline{INIT}$ also serves to synchronize timing of two modules in the stereo mode. Logic circuitry timing is provided by an external clock of 12.288 MHz (48 kHz update rate) or 11.2896 MHz (44.1 kHz update rate). The 18-bit data then "loads up" the 64 tap, 20 kHz FIR filter. After 64 conversions, the filter begins to output a 35-bit word truncated down to 20 bits. The 20-bit data is fed to a 3:1 decimation filter that transmits the 20-bit word at a 48 kHz or 44.1 kHz rate to the data mux register for parallel data and to the AES/EBU serializer.

Parallel Data

In a monophonic or stereo system requiring parallel data operation, the ADC5120 (or both ADC5120s if stereo)* should be configured as monophonic, channel A as shown in figure 7, with the output data multiplexed. DSTRI, DSTR2, and DSTR3 indicate the presence of the eight MSBs, the middle eight bits, and the four LSBs respectively at DO-D7 with D7 representing the MSB; DO the LSB.

Serial Data

Stereophonic AES/EBU serial data can be achieved by first synchronizing two ADC5120s with $\overline{INIT}$ (see figure 4). Both channels monitoring the common sync line will lock on to the negative transition of SYNC OUT. 65 conversions are required to load up the FIR filter before data is available and can be synchronized. The two ADC5120s must be identified as A or B (see figures 7 - 9) and the stereo mode chosen. Monophonic AES/EBU serial data can also be achieved by following the instructions in figure 7.

*Note: In a stereo application using parallel data, the sync lines must be common.

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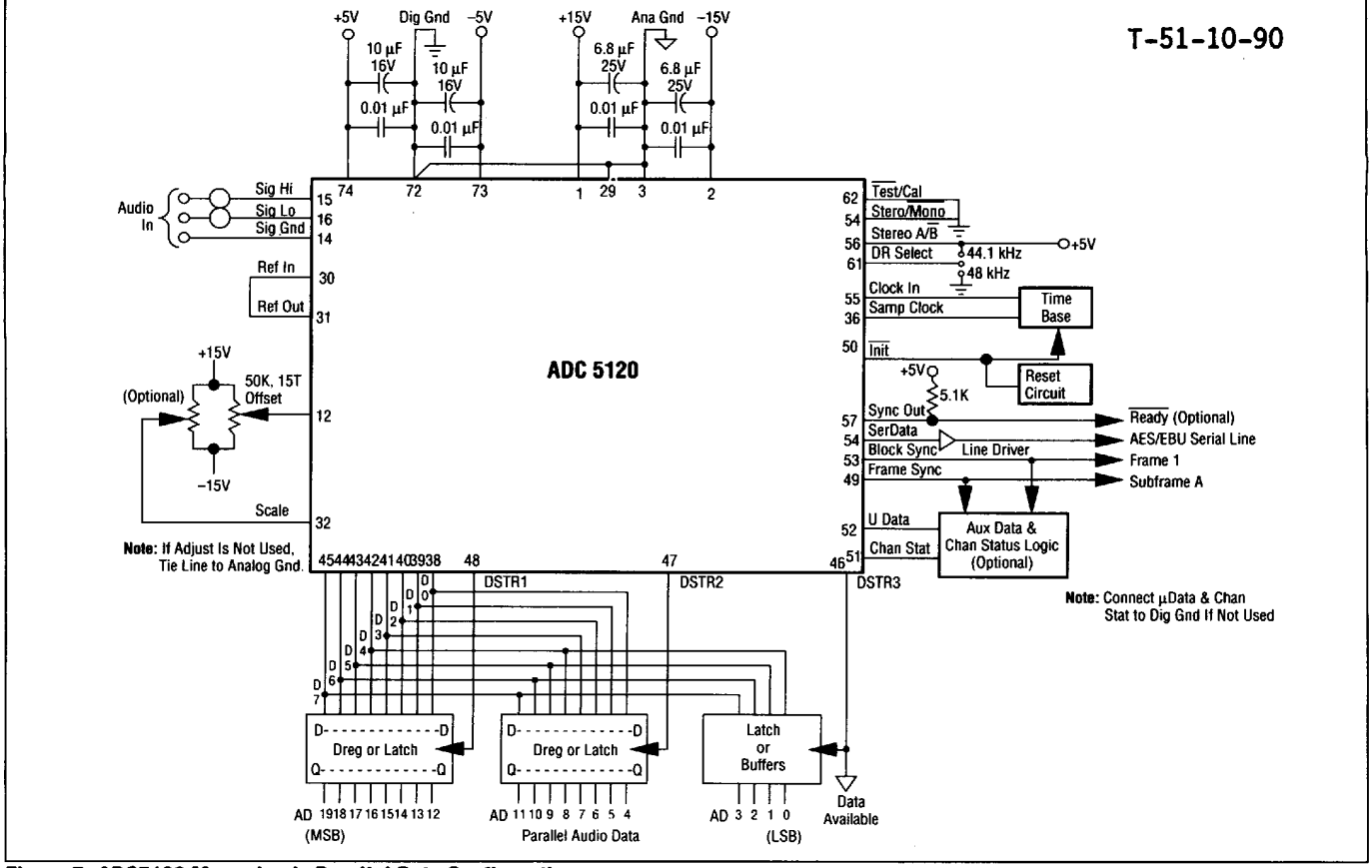


Figure 7. ADC5120 Monophonic Parallel Data Configuration.

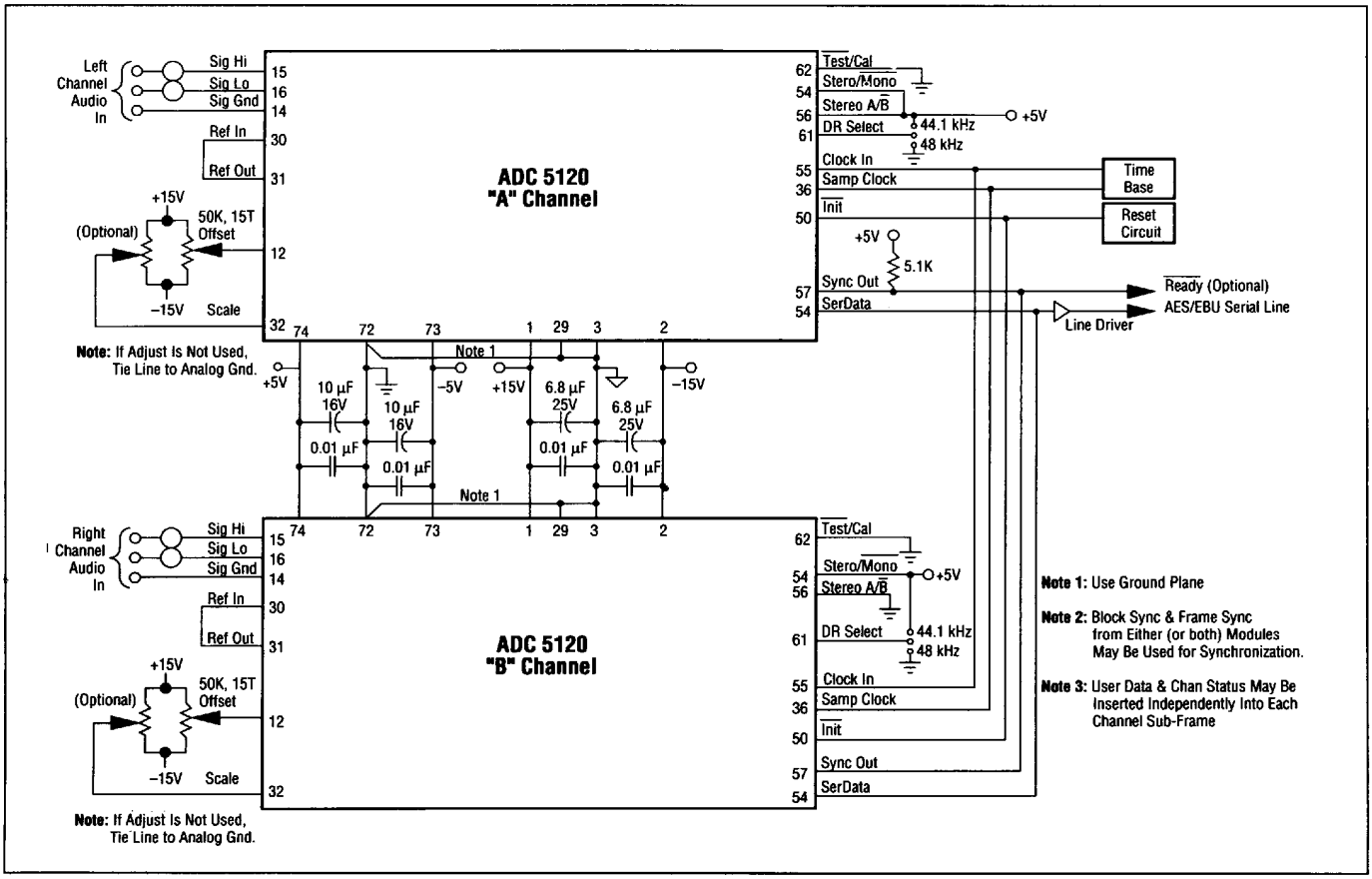


Figure 8. ADC 5120 Stereophonic Serial Data Configuration.

ADC5120 PIN ASSIGNMENTS

AES/EBU COMPATIBLE SERIAL INTERFACE

PIN		
54	SERDATA	AES/EBU standard serial data output. TTL/CMOS compatible (line driver not included).
60	STEREO/$\overline{\text{MONO}}$	Low identifies the channel as a monophonic channel and the SERDATA output will be formatted accordingly. High indicates the channel is one of two stereo channels. Control of the SERDATA transmission and output data format will depend on the state of the STEREO $\overline{\text{A/B}}$ line.
56	STEREO A/$\overline{\text{B}}$	When low, identifies the channel as the "B" stereo channel (right channel). When high, identifies the channel as the "A" stereo channel (left channel). Should be set for "A" if true MONO operation is desired. If set for "B" while MONO is selected, the second half of each frame will be tri-stated to allow transmission of auxiliary or sub-channel data by an external device.
53	BLOCK SYNC	Active high output that occurs during serial transmission of the first frame of each 192 frame AES/EBU block.
49	FRAME SYNC	Active high during first subframe (A subframe) of each AES/EBU frame transmission.
52	UDATA	Single bit user data input channel. Used in conjunction with BLOCK SYNC and FRAME SYNC to insert blocks of user data into the serial transmission. High = '1'.
51	CHAN STAT	Single bit channel status input data channel. Used in conjunction with BLOCK SYNC and FRAME SYNC to insert channel status information into the serial transmission. High = '1'.
61	DR SELECT	Data rate (sampling rate) select. High selects 44.1 kHz sample rate. Low selects 48 kHz sample rate.

PARALLEL DATA OUTPUT

PIN		
45	D7 (MSB)	Eight bits of multiplexed 2's complement parallel binary output data. First byte is most significant 8 bits. Second byte is middle eight bits . Last byte is 4 LSBs of 20 bit data (in MSB positions of byte).
44	D6	
43	D5	
42	D4	
41	D3	
40	D2	
39	D1	
38	D0 (LSB)	
48	DSTR1	Active high timing strobes indicate presence of byte 1, 2, or 3 at DATA OUT.
47	DSTR2	
46	DSTR3	

INTERFACE CONTROL & TIMING SIGNALS

PIN		
55	CLK IN	TTL compatible clock input: 12.288 MHz for 48 kHz sampling rate, 11.2896 MHz for 44.1 kHz sampling rate.
50	$\overline{\text{INIT}}$	Initialization input, active low. Used to initialize all internal circuits to a known state. Also used to synchronize timing for two modules operating in stereo mode.
62	$\overline{\text{TEST/CAL}}$	Active high input causes FIR filter and decimator to be bypassed. In this mode, eighteen bit data is presented at DATA OUT at the full SAMPCLK rate. (2's comp. binary).
36	SAMPCLK	Sample clock input, TTL/CMOS compatible. Establishes the analog signal sampling rate. 144 kHz for 48 kHz output data rate. 132.3 kHz for 44.1 kHz output data rate. Must be synchronous to system clock, CLK IN.
37	$\overline{\text{EOC}}$	End of conversion. High during each conversion at SAMPCLK rate. Falling edge indicates end of SAMPCLK conversion.
57	SYNC OUT	Open drain output signal indicating synchronization is in process. The falling edge indicates a "lock". Should be wire-or'd with the SYNC OUT lines of all other simultaneous channels.

ANALOG CONNECTIONS AND SIGNAL INTERFACE

PIN		
15	SIG HI	Audio signal hi (+) input.
16	SIG LO	Audio signal lo (-) input.
31	REF OUT	Reference voltage output (-6.5 volts).
30	REF IN	Reference voltage input (-6.5 volts).
14	SIG GND	Analog signal ground. Electrically connected to analog power ground.
12	OFFSET	Offset adjust pin. A voltage applied to this terminal will change the input offset approximately +500 µV/V.
32	SCALE	Scale factor adjust pin. A voltage applied to this terminal will change the input scaling approximately -1 mV/V.

POWER & GROUND CONNECTIONS

PIN		
74	+5V	+5 volts digital supply.
73	-5V	-5 volts digital supply.
1	+15V	+15 volts analog supply.
2	-15V	-15 volts analog supply.
3	AGND	Analog power ground. +15V and -15V returns — electrically connected to SIG GND.
29	AGND	
72	DGND	Digital power ground. +5V and -5V returns.

	PARALLEL DATA			SERIAL DATA		
	MONO	STEREO		MONO	STEREO	
		L (A)	R (B)		L (A)	R (B)
STEREO/$\overline{\text{MONO}}$ (pin 60)	0	0	0	0	1	1
STEREO A/$\overline{\text{B}}$ (pin 56)	1	1	1	1	1	0

Figure 9. Data Format Configuration Chart.

ADC5120 PERFORMANCE TESTING

To further instill confidence in our customers, Analogic supplies with each ADC5120 a data sheet as proof of 100% testing performed on each device prior to shipping. Such data sheets reflect testing performed in the "Frequency Domain".

Frequency Domain Testing

The Frequency Domain Testing is performed by means of proprietary automatic test equipment inclusive of an ultra-high speed Array Processor manufactured by Analogic. The power of the processor provides us with a great deal of flexibility in both gathering and formatting the data. While a Rosenfeld window is applied on a standard basis, other types of windows such as Blackman-Harris and Blackman are available for customized testing. The number of samples can be varied from 512 to 8192, and the system can average up to 64 FFT's. A block diagram of the "Frequency Domain" test system is shown in Figure 10; a typical data sheet of an ADC5120 tested over frequency is shown in Figure 11.

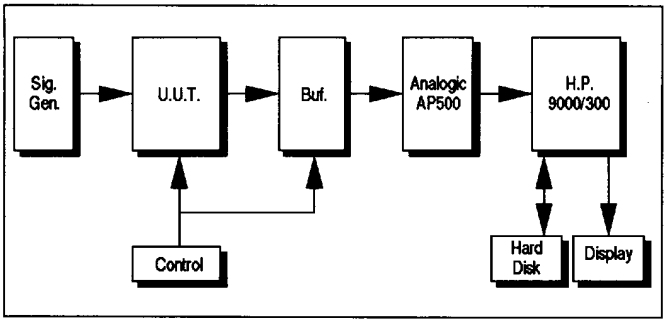


Figure 10. "Frequency Domain" Test System.

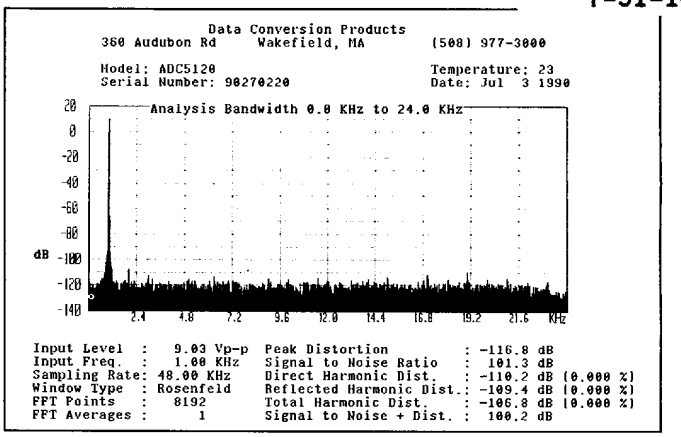
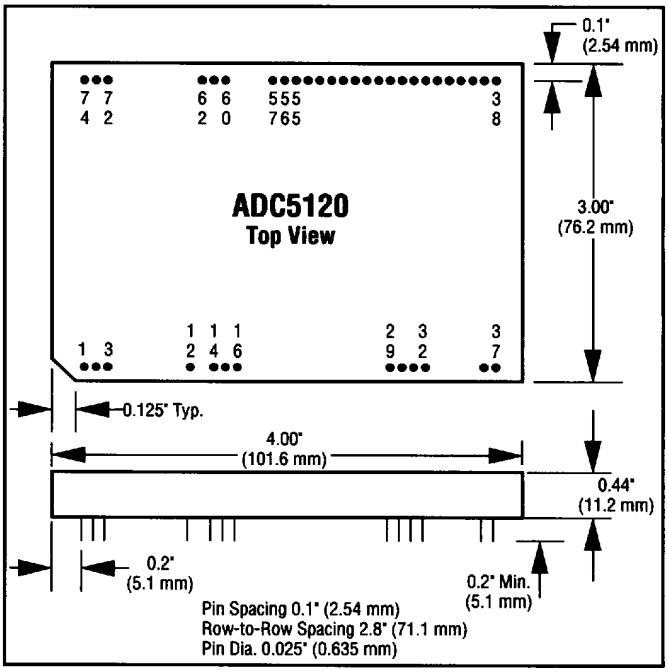


Figure 11. Frequency Domain" Data Sheet.

ADC5120 Mechanical



Ordering Guide

Simply Specify

ADC5120-M4

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Bulletin No. 16-100395 REV 0 Printed in U.S.A.