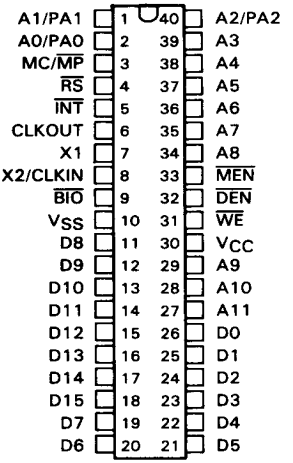
JANUARY 1987—REVISED MAY 1989

- 160-ns Instruction Cycle
- 144/256-Word On-Chip Data RAM
- 1.5K/4K-Word On-Chip Program ROM
- 4K-Word On-chip Program EPROM (TMS320E15/E17)
- EPROM Code Protection for Copyright Security
- 4K-Word Total External Memory at Full Speed
- 32-Bit ALU/Accumulator
- 16 × 16-Bit Multiplier with a 32-Bit Product
- 0 to 16-Bit Barrel Shifter
- Eight Input and Eight Output Channels
- Dual-Channel Serial Port (TMS320C17/E17)
- 16-Bit Bidirectional Data Bus with 50-Mbps Transfer Rate
- Single 5-V Supply
- Packaging: 40-Pin DIP, 44-Lead PLCC, and 44-Lead CER-QUAD
- Commercial and Military Versions Available
- NMOS Technology:
  - TMS32010 . . . . . 200-ns cycle time
- CMOS Technology:
  - TMS320C10 . . . . . 200-ns cycle time
  - TMS320C10-14 . . . . . 280-ns cycle time
  - TMS320C10-25 . . . . . 160-ns cycle time
  - TMS320C15 . . . . . 200-ns cycle time
  - TMS320C15-25 . . . . . 160-ns cycle time
  - TMS320E15 (EPROM) . . . . 200-ns cycle time
  - TMS320E15-25 (EPROM) . . 160-ns cycle time
  - TMS320C17 . . . . . 200-ns cycle time
  - TMS320E17 (EPROM) . . . . 200-ns cycle time

TMS32010, TMS320C10
N PACKAGE
(TOP VIEW)



This data sheet provides complete design documentation for all the first-generation devices of the TMS320 family. This facilitates the selection of the devices best suited for user applications by providing all specifications and special features for each TMS320 member. This data sheet is divided into four major sections: architecture, electrical specifications (NMOS and CMOS), timing diagrams, and mechanical data. In each of these sections, generic information is presented first, followed by specific device information. An index is provided for quick reference to specific information about a device.

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description

The TMS320 family of 16/32-bit single-chip digital signal processors combines the flexibility of a high-speed controller with the numerical capability of an array processor, thereby offering an inexpensive alternative to multichip bit-slice processors. The highly paralleled architecture and efficient instruction set provide speed and flexibility to produce a MOS microprocessor family capable of executing 6.4 MIPS (million instructions per second). The TMS320 family optimizes speed by implementing functions in hardware that other processors implement through microcode or software. This hardware-intensive approach provides the design engineer with processing power previously unavailable on a single chip.

The TMS320 family consists of two generations of digital signal processors. The first generation contains the TMS32010 and its spinoffs, as described in this data sheet. The TMS32020 and TMS320C25 are the second-generation processors, designed for higher performance. Many features are common among the TMS320 processors. Specific features are added in each processor to provide different cost/performance tradeoffs. Software compatibility is maintained throughout the family to protect the user's investment in architecture. Each processor has software and hardware tools to facilitate rapid design.

introduction

The TMS32010, the first NMOS digital signal processor in the TMS320 family, was introduced in 1983. Its powerful instruction set, inherent flexibility, high-speed number-crunching capabilities, and innovative architecture have made this high-performance, cost-effective processor the ideal solution to many telecommunications, computer, commercial, industrial, and military applications. Since that time, the TMS320C10, a low-power CMOS version of the industry-standard TMS32010, and other spinoff devices have been added to the first generation of the TMS320 family.

The TMS32010 microprocessor executes at 20 MHz or 5 MIPS. It is capable of executing a 16 x 16-bit multiply with a 32-bit result in a single instruction cycle. On-chip data RAM of 144 words and on-chip program ROM of 1.5K words are available. Full-speed execution of 4K words of off-chip program memory is also possible.

The TMS320C10 is object-code and pin-for-pin compatible with the TMS32010. It is processed in CMOS technology, achieving a power dissipation less than one-sixth that of the NMOS device. The lower power dissipation makes the TMS320C10 ideal for power-sensitive applications such as digital telephony and portable products. The TMS320C10-25, a 25-MHz version of the TMS320C10, has a 160-ns instruction cycle time and is well suited for high-performance DSP applications. The TMS320C10 is also available in a 280-ns version, the TMS320C10-14. This device provides a low-cost alternative for DSP applications not requiring the maximum operating frequency of the TMS320C10.

The TMS320C15 and TMS320E15 CMOS devices are object-code and pin-for-pin compatible with the TMS32010 and offer expanded on-chip RAM of 256 words and on-chip program ROM or EPROM of 4K words. These devices allow the capability of upgrading performance and reducing power, board space, and system cost without hardware redesign. The TMS320C15/E15 are available in 160-ns versions, the TMS320C15-25 and TMS320E15-25.

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introduction (continued)

The TMS320C17 and TMS320E17 also offer expanded on-chip RAM of 256 words and on-chip program ROM or EPROM of 4K words. These devices provide a dual-channel serial interface, on-chip μ-law/A-law companding hardware, and a serial port timer. In addition, a 16-bit coprocessor interface provides a direct communication channel to common 4/8-bit microcomputers (no glue logic required), and minimal logic interface to most common 16/32-bit microprocessors. The devices are object-code compatible with the TMS32010 and processed in CMOS technology.

Table 1 provides an overview of the first generation of TMS320 processors with comparisons of memory, I/O, cycle timing, power, package type, technology, and military support. For specific availability, contact the nearest TI Field Sales Office.

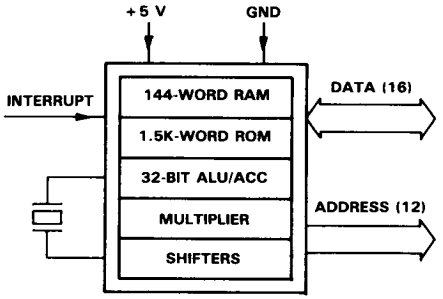
TABLE 1. TMS320 FIRST-GENERATION DEVICE OVERVIEW

DEVICE		MEMORY				I/O†			CYCLE TIME	TYP POWER	PACKAGE TYPE‡		
		ON-CHIP			OFF-CHIP								
		RAM	ROM	EPROM	EXPANSION	SER	PAR	CPX	(ns)	(mW)	DIP	PLCC	CER-QUAD
TMS32010§	(NMOS)	144	1.5K	—	4K	—	8 x 16	—	200	900	40	—	—
TMS320C10§	(CMOS)	144	1.5K	—	4K	—	8 x 16	—	200	165	40	44	—
TMS320C10-14	(CMOS)	144	1.5K	—	4K	—	8 x 16	—	280	140	40	44	—
TMS320C10-25	(CMOS)	144	1.5K	—	4K	—	8 x 16	—	160	200	40	44	—
TMS320C14¶	(CMOS)	256	4K	—	4K	1	7 x 16	—	160	—	—	68	—
TMS320E14¶	(CMOS)	256	—	4K	4K	1	7 x 16	—	160	—	—	—	68
TMS320C15¶	(CMOS)	256	4K	—	4K	—	8 x 16	—	200	225	40	44	—
TMS320C15-25	(CMOS)	256	4K	—	4K	—	8 x 16	—	160	250	40	44	—
TMS320E15¶	(CMOS)	256	—	4K	4K	—	8 x 16	—	200	275	40	—	44
TMS320E15-25	(CMOS)	256	—	4K	4K	—	8 x 16	—	160	325	40	—	44
TMS320C17	(CMOS)	256	4K	—	—	2	6 x 16	YES	200	250	40	44	—
TMS320E17	(CMOS)	256	—	4K	—	2	6 x 16	YES	200	275	40	—	44

† SER = serial; PAR = parallel; CPX = coprocessor interface.
‡ DIP = dual in-line pin; PLCC = plastic-leaded chip carrier;
CER-QUAD = surface mount ceramic-leaded chip carrier.
§ Military version available.
¶ Military version planned; contact nearest TI Field Sales Office for availability.

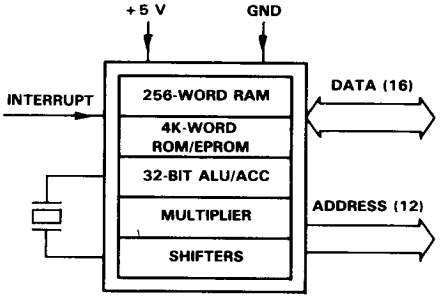
Key Features: TMS32010/C10

- Instruction Cycle Timing:
  - 160 ns (TMS320C10-25)
  - 200 ns (TMS32010/C10)
  - 280 ns (TMS320C10-14)
- 144 Words of On-Chip Data RAM
- 1.5K Words of On-Chip Program ROM
- External Memory Expansion up to 4K Words at Full Speed
- 16 x 16-Bit Multiplier with 32-Bit Product
- 0 to 16-Bit Barrel Shifter
- On-Chip Clock Oscillator
- Single 5-V Supply
- Device Packaging:
  - 40-Pin DIP (all devices)
  - 44-Lead PLCC (CMOS only)
- Technology
  - NMOS: TMS32010
  - CMOS: TMS320C10/C10-14/C10-25



Key Features: TMS320C15/E15

- Instruction Cycle Timing:
  - 160 ns (TMS320C15-25/E15-25)
  - 200 ns (TMS320C15/E15)
- 256 Words of On-Chip Data RAM
- 4K Words of On-Chip Program ROM (TMS320C15/C15-25)
- 4K Words of On-Chip Program EPROM (TMS320E15/E15-25)
- EPROM Code Protection for Copyright Security
- External Memory up to 4K Words at Full Speed
- Object-Code and Pin-For-Pin Compatible with TMS32010
- 16 x 16-Bit Multiplier with 32-Bit Product
- 0 to 16-Bit Barrel Shifter
- On-Chip Clock Oscillator
- Single 5-V Supply
- Device Packaging:
  - 40-Pin DIP (all devices)
  - 44-Lead PLCC (TMS320C15/C15-25)
  - 44-Lead CER-QUAD (TMS320E15/E15-25)
- CMOS Technology



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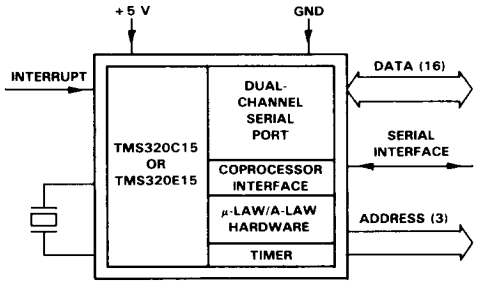
Key Features: TMS320C17/E17

- **Instruction Cycle Timing:**
  — 200 ns (TMS320C17/E17)
- **256 Words of On-Chip Data RAM**
- **4K Words of On-Chip Program ROM (TMS320C17)**
- **4K Words of On-Chip Program EPROM (TMS320E17)**
- **EPROM Code Protection for Copyright Security**
- **Object-Code Compatible with TMS32010**
- **Dual-Channel Serial Port for Full-Duplex Serial Communication**
- **Serial Port Timer for Standalone Serial Communications**
- **On-Chip Companding Hardware for μ-law/A-law PCM Conversions**
- **16-Bit Coprocessor Interface for Common 4/8/16/32-Bit Microcomputers/Microprocessors**
- **Device Packaging:**
  — 40-Pin DIP (all devices)
  — 44-Lead PLCC (TMS320C17)
  — 44-Lead CER-QUAD (TMS320E17)
- **CMOS Technology**



architecture

The TMS320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of instruction fetch and execution. The TMS320 family's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

32-bit ALU/accumulator

The TMS320 first-generation devices contain a 32-bit ALU and accumulator for support of double-precision, two's-complement arithmetic. The ALU is a general-purpose arithmetic unit that operates on 16-bit words taken from the data RAM or derived from immediate instructions. In addition to the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller. The accumulator stores the output from the ALU and is often an input to the ALU. It operates with a 32-bit wordlength. The accumulator is divided into a high-order word (bits 31 through 16) and a low-order word (bits 15 through 0). Instructions are provided for storing the high- and low-order accumulator words in memory.

shifters

Two shifters are available for manipulating data. The ALU barrel shifter performs a left-shift of 0 to 16 places on data memory words loaded into the ALU. This shifter extends the high-order bit of the data word and zero-fills the low-order bits for two's-complement arithmetic. The accumulator parallel shifter performs a left-shift of 0, 1, or 4 places on the entire accumulator and places the resulting high-order accumulator bits into data RAM. Both shifters are useful for scaling and bit extraction.

16 x 16-bit parallel multiplier

The multiplier performs a 16 x 16-bit two's-complement multiplication with a 32-bit result in a single instruction cycle. The multiplier consists of three units: the T Register, P Register, and multiplier array. The 16-bit T Register temporarily stores the multiplicand; the P Register stores the 32-bit product. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the device to perform fundamental operations such as convolution, correlation, and filtering.

data and program memory

Since the TMS320 devices use a Harvard architecture, data and program memory reside in two separate spaces. The first-generation devices have 144 or 256 words of on-chip data RAM and 1.5K or 4K words of on-chip program ROM. On-chip program EPROM of 4K words is provided on the TMS320E15/E17. The EPROM cell utilizes standard PROM programmers and is programmed identically to a 64K CMOS EPROM (TMS27C64).

program memory expansion

The first-generation devices are capable of executing up to 4K words of external memory at full speed for those applications requiring external program memory space. This allows for external RAM-based systems to provide multiple functionality. The TMS320C17/E17 provides no memory expansion capability.

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microcomputer/microprocessor operating modes (TMS32010/C10/C15/E15)

The TMS32010/C10 and TMS320C15/E15 devices offer two modes of operation defined by the state of the MC/$\overline{MP}$ pin: the microcomputer mode (MC/$\overline{MP}$ = 1) or the microprocessor mode (MC/$\overline{MP}$ = 0). In the microcomputer mode, on-chip ROM is mapped into the memory space with up to 4K words of external memory available. In the microprocessor mode, all 4K words of memory are external.

interrupts and subroutines

The TMS320 first-generation devices contain a four-level hardware stack for saving the contents of the program counter during interrupts and subroutine calls. Instructions are available for saving the device's complete context. PUSH and POP instructions permit a level of nesting restricted only by the amount of available RAM. The interrupts used in these devices are maskable.

input/output

The 16-bit parallel data bus can be utilized to perform I/O functions in two cycles. The I/O ports are addressed by the three LSBs on the address lines. In addition, a polling input for bit test and jump operations ($\overline{BIO}$) and an interrupt pin ($\overline{INT}$) have been incorporated for multitasking.

serial port (TMS320C17/E17)

Two of the I/O ports on the TMS320C17/E17 are dedicated to the serial port and companding hardware. I/O port 0 is dedicated to control register 0, which controls the serial port, interrupts, and companding hardware. I/O port 1 accesses control register 1, as well as both serial port channels, and the companding hardware. The six remaining I/O ports are available for external parallel interfaces.

The dual-channel serial port is capable of full-duplex serial communication and offers direct interface to combo-codecs. Receive and transmit registers that operate with 8-bit data samples are I/O-mapped. Either internal or external framing signals for serial data transfers are selected through the system control register. The serial port clock provides the bit timing for transfers with the serial port, and may be either an input or output. A framing pulse signal provides framing pulses for combo-codec circuits, an 8-kHz sample clock for voice-band systems, or a timer for control applications.

companding hardware (TMS320C17/E17)

On-chip hardware enables the TMS320C17/E17 to compand (COMpress/exPAND) data in either μ-law or A-law format. The companding logic operation is configured via the system control register. Data may be companded in either a serial mode for operation on serial port data (converting between linear and logarithmic PCM) or a parallel mode for computation inside the device. The TMS320C17/E17 allows the hardware companding logic to operate with either sign-magnitude or two's-complement numbers.

coprocessor port (TMS320C17/E17)

The coprocessor port on the TMS320C17/E17 provides a direct connection to most 4/8-bit microcomputers and 16/32-bit microprocessors. The port is accessed through I/O port 5 using IN and OUT instructions. The coprocessor interface allows the device to act as a peripheral (slave) microcomputer to a microprocessor, or as a master to a peripheral microcomputer. In the microcomputer mode, the 16 data lines are used for the 6 parallel 16-bit I/O ports. In the coprocessor mode, the 16-bit parallel port is reconfigured to operate as a 16-bit latched bus interface. For peripheral transfer, an 8-bit or 16-bit length of the coprocessor port can be selected.

instruction set

A comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general-purpose operations, such as high-speed control. All of the first-generation devices are object-code compatible and use the same 60 instructions. The instruction set consists primarily of single-cycle single-word instructions, permitting execution rates of more than six million instructions per second. Only infrequently used branch and I/O instructions are multicycle. Instructions that shift data as part of an arithmetic operation execute in a single cycle and are useful for scaling data in parallel with other operations.

Three main addressing modes are available with the instruction set: direct, indirect, and immediate addressing.

direct addressing

In direct addressing, seven bits of the instruction word concatenated with the 1-bit data page pointer form the data memory address. This implements a paging scheme in which the first page contains 128 words, and the second page contains up to 128 words.

indirect addressing

Indirect addressing forms the data memory address from the least-significant eight bits of one of the two auxiliary registers, AR0 and AR1. The Auxiliary Register Pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented and the ARP changed in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

immediate addressing

Immediate instructions derive data from part of the instruction word rather than from the data RAM. Some useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

instruction set summary

Table 2 lists the symbols and abbreviations used in Table 3, the instruction set summary. Table 3 contains a short description and the opcode for each TMS320 first-generation instruction. The summary is arranged according to function and alphabetized within each functional group.

TABLE 2. INSTRUCTION SYMBOLS

SYMBOL	MEANING
ACC	Accumulator
D	Data memory address field
I	Addressing mode bit
K	Immediate operand field
PA	3-bit port address field
R	1-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

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TABLE 3. TMS320 FIRST-GENERATION INSTRUCTION SET SUMMARY

ACCUMULATOR INSTRUCTIONS

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ABS	Absolute value of accumulator	1	1	0 1 1 1 1 1 1 1 1 0 0 0 0 1 0 0 0
ADD	Add to accumulator with shift	1	1	0 0 0 0 ◄— S —► I ◄—— D ——►
ADDH	Add to high-order accumulator bits	1	1	0 1 1 0 0 0 0 0 1 ◄—— D ——►
ADDS	Add to accumulator with no sign extension	1	1	0 1 1 0 0 0 0 1 1 ◄—— D ——►
AND	AND with accumulator	1	1	0 1 1 1 1 0 [illegible] ◄—— D ——►
LAC	Load accumulator with shift	1	1	0 0 1 0 ◄— S —► I ◄—— D ——►
LACK	Load accumulator immediate	1	1	0 1 1 1 1 1 1 0 ◄———— K ————►
OR	OR with accumulator	1	1	0 1 1 1 1 0 1 0 I ◄—— D ——►
SACH	Store high-order accumulator bits with shift	1	1	0 1 0 1 1 ◄X► I ◄—— D ——►
SACL	Store low-order accumulator bits	1	1	0 1 0 1 0 0 0 0 I ◄—— D ——►
SUB	Subtract from accumulator with shift	1	1	0 0 0 1 ◄— S —► I ◄—— D ——►
SUBC	Conditional subtract (for divide)	1	1	0 1 1 0 0 1 0 0 I ◄—— D ——►
SUBH	Subtract from high-order accumulator bits	1	1	0 1 1 0 0 0 1 0 I ◄—— D ——►
SUBS	Subtract from accumulator with no sign extension	1	1	0 1 1 0 0 0 1 1 I ◄—— D ——►
XOR	Exclusive OR with accumulator	1	1	0 1 1 1 1 0 0 0 I ◄—— D ——►
ZAC	Zero accumulator	1	1	0 1 1 1 1 1 1 1 1 0 0 0 1 0 0 1
ZALH	Zero accumulator and load high-order bits	1	1	0 1 1 0 0 1 0 1 I ◄—— D ——►
ZALS	Zero accumulator and load low-order bits with no sign extension	1	1	0 1 1 0 0 1 1 0 I ◄—— D ——►

AUXILIARY REGISTER AND DATA PAGE POINTER INSTRUCTIONS

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
LAR	Load auxiliary register	1	1	0 0 1 1 1 0 0 R I ◄—— D ——►
LARK	Load auxiliary register immediate	1	1	0 1 1 1 0 0 0 R ◄———— K ————►
LARP	Load auxiliary register pointer immediate	1	1	0 1 1 0 1 0 0 0 1 0 0 0 0 0 0 0 K
LDP	Load data memory page pointer	1	1	0 1 1 0 1 1 1 1 I ◄—— D ——►
LDPK	Load data memory page pointer immediate	1	1	0 1 1 0 1 1 1 0 0 0 0 0 0 0 0 0 K
MAR	Modify auxiliary register and pointer	1	1	0 1 1 0 1 0 0 0 I ◄—— D ——►
SAR	Store auxiliary register	1	1	0 0 1 1 0 0 0 R I ◄—— D ——►

TABLE 3. TMS320 FIRST-GENERATION INSTRUCTION SET SUMMARY (CONTINUED)

BRANCH INSTRUCTIONS

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
B	Branch unconditionally	2	2	1 1 1 1 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BANZ	Branch on auxiliary register not zero	2	2	1 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BGEZ	Branch if accumulator ≥ 0	2	2	1 1 1 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BGZ	Branch if accumulator > 0	2	2	1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BIOZ	Branch on $\overline{BIO}$ = 0	2	2	1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BLEZ	Branch if accumulator ≤ 0	2	2	1 1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BLZ	Branch if accumulator < 0	2	2	1 1 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BNZ	Branch if accumulator ≠ 0	2	2	1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BV	Branch on overflow	2	2	1 1 1 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
BZ	Branch if accumulator = 0	2	2	1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
CALA	Call subroutine from accumulator	2	1	0 1 1 1 1 1 1 1 1 0 0 0 1 1 0 0
CALL	Call subroutine immediately	2	2	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ← BRANCH ADDRESS →
RET	Return from subroutine or interrupt routine	2	1	0 1 1 1 1 1 1 1 1 0 0 0 1 1 0 1

T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
APAC	Add P register to accumulator	1	1	0 1 1 1 1 1 1 1 1 0 0 0 1 1 1 1
LT	Load T register	1	1	0 1 1 0 1 0 1 0 I ← D →
LTA	LTA combines LT and APAC into one instruction	1	1	0 1 1 0 1 1 0 0 I ← D →
LTD	LTD combines LT, APAC, and DMOV into one instruction	1	1	0 1 1 0 1 0 1 1 I ← D →
MPY	Multiply with T register, store product in P register	1	1	0 1 1 0 1 1 0 1 I ← D →
MPYK	Multiply T register with immediate operand; store product in P register	1	1	1 0 0 ← K →
PAC	Load accumulator from P register	1	1	0 1 1 1 1 1 1 1 1 0 0 0 1 1 1 0
SPAC	Subtract P register from accumulator	1	1	0 1 1 1 1 1 1 1 1 0 0 1 0 0 0 0

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TABLE 3. TMS320 FIRST-GENERATION INSTRUCTION SET SUMMARY (CONCLUDED)

CONTROL INSTRUCTIONS																			
MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DINT	Disable interrupt	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0
LST	Load status register	1	1	0	1	1	1	1	0	1	1	I	◄			D			►
NOP	No operation	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
POP	POP stack to accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	0	1
PUSH	PUSH stack from accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	0	0
ROVM	Reset overflow mode	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	1	0
SOVM	Set overflow mode	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	1
SST	Store status register	1	1	0	1	1	1	1	1	0	0	I	◄			D			►

I/O AND DATA MEMORY OPERATIONS																			
MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMOV	Copy contents of data memory location into next higher location	1	1	0	1	1	0	1	0	0	1	I	◄			D			►
IN	Input data from port	2	1	0	1	0	0	0	◄	PA	►	I	◄			D			►
OUT	Output data to port	2	1	0	1	0	0	1	◄	PA	►	I	◄			D			►
TBLR	Table read from program memory to data RAM	3	1	0	1	1	0	0	1	1	1	I	◄			D			►
TBLW	Table write from data RAM to program memory	3	1	0	1	1	1	1	1	0	1	I	◄			D			►

oevelopment support products

Together, Texas Instruments and its authorized third-party suppliers offer an extensive line of development support products to assist the user in all aspects of TMS320 first-generation-based design and development. These products range from development and application software to complete hardware development and evaluation systems. Table 4 lists the development support products for the first-generation TMS320 devices.

System development may begin with the use of the simulator, evaluation module (EVM), or emulator (XDS), along with an assembler/linker. These tools give the TMS320 user various means of evaluation, from software simulation of the first-generation TMS320s (simulator) to full-speed in-circuit emulation with hardware and software break point tracing and timing capabilities (XDS).

Software and hardware can be developed simultaneously by using the macro assembler/linker or simulator for software development, the XDS for hardware development, and the evaluation module for both software development and limited hardware development.

Many third-party vendors offer additional development support for the first-generation TMS320s, including assembler/linkers, simulators, high-level languages, applications software, algorithm development tools, application boards, software development boards, and in-circuit emulators. Refer to the *TMS320 Family Development Support Reference Guide* (SPRU011A) for further information about TMS320 development support products offered by both Texas Instruments and its third-party suppliers.

Additional support for the TMS320 products consists of an extensive library of product and applications documentation. Three-day DSP design workshops are offered by the TI Regional Technology Centers (RTCs). These workshops provide insight into the architecture and the instruction set of the first-generation TMS320s as well as hands-on training with the TMS320 development tools. When technical questions arise in regard to a TMS320 member, contact Texas Instruments TMS320 Hotline at (713) 274-2320. Or, keep informed on the latest TI and third-party development support tools by accessing the libraries of application source code via the DSP Bulletin Board Service (BBS) at (713) 274-2323. The BBS provides access for the 2400-/1200-/300-bps modems.

TABLE 4. TMS320 FIRST-GENERATION SOFTWARE AND HARDWARE SUPPORT

SOFTWARE TOOLS	PART NUMBER
Macro Assembler/Linker	
PC/MS-DOS	TMDS3242850-02
VAX/VMS	TMDS3242250-08
VAX ULTRIX	TMDS3242260-08
SUN-3 UNIX	TMDS3242550-08
Simulator	
PC/MS-DOS	TMDS3240811-02
VAX/VMS	TMDS3240211-08
Digital Filter Design Package (DFDP)	
IBM PC PC-DOS	DFDP/IBM002
DSP Software Library	
PC/MS-DOS	TMDC3240812-12
VAX/VMS	TMDC3240212-18
TMS320 Bell 212A Modem Software	
PC/MS-DOS	TMDX3240813-12
Data Encryption Standard Software	
PC/MS-DOS	TMDX3240814-12
HARDWARE TOOLS	**PART NUMBER**
Evaluation Tools	
Evaluation Module (EVM)	RTC/EVM320A-03
Analog Interface Board 1 (AIB1)	RTC/EVM320C-06
Analog Interface Board 2 (AIB2)	RTC/AIB320A-06
EPROM DSP Starter Kit (TMS320E15)	RTC/EVM320E-15
XDS/22 Emulators	
TMS320C10/C15	TMDS3262211
TMS320C14	TMDX3262214
TMS320C17	TMDX3262217
XDS/22 Upgrade Kits	
TMS32010 → TMS320C10/C15	TMDS3282215
TMS320C10/C15 → TMS320C14	TMDX3285010 and TMDX3285018
TMS320C10/C15 → TMS320C17	TMDX3285014 and TMDX3285018
EPROM Programming Adaptor Sockets	
40- to 28-pin (TMS320E15/E17)	RTC/PGM320A-06
44- to 28-pin (TMS320E15/E17)	RTC/PGM320C-06
68- to 28-pin (TMS320E14)	TMDX3270110
Additional Target Connector	
44-lead PLCC (TMS320C10)	TMDX3288810

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documentation support

Extensive documentation supports the first-generation TMS320 devices from product announcement through applications development. The types of documentation include data sheets with design specifications, complete user's guides, and 750 pages of application reports published in *Digital Signal Processing Applications with the TMS320 Family* (SPRA012A).

A series of DSP textbooks is being published to support digital signal processing research and education. The first book, *DFT/FFT and Convolution Algorithms,* is now available. The TMS320 newsletter, *Details on Signal Processing,* is published quarterly and distributed to update TMS320 customers on product information. The TMS320 DSP bulletin board service provides access to large amounts of information pertaining to the TMS320 family.

Refer to the *TMS320 Family Development Support Reference Guide* (SPRU011A) for further information about TMS320 documentation. To receive copies of first-generation TMS320 literature, call the Customer Response Center at 1-800-232-3200.

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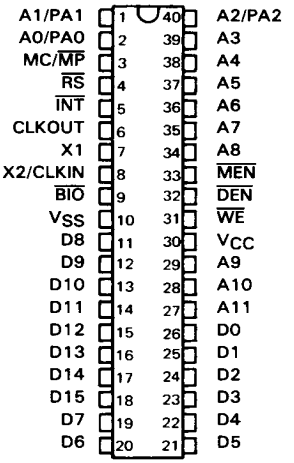
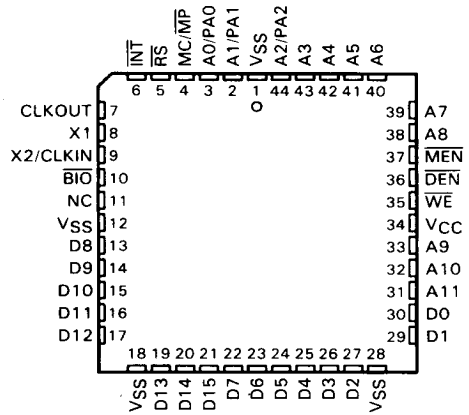
description

Since the TMS32010 was the first digital signal processor in the TMS320 family, its architecture has served as the basis from which first-generation spinoff devices have evolved. The TMS320C10 is a low-power CMOS version of the TMS32010 and identical to it. The TMS320C15/E15 is object-code and pin-for-pin compatible with the TMS32010 and offers expanded on-chip RAM and ROM or EPROM.

TMS32010, TMS320C10
TMS320C15, TMS320E15
N/JD PACKAGE
(TOP VIEW)



TMS320C10, TMS320C15, TMS320E15
FN AND FZ PACKAGES
(TOP VIEW)

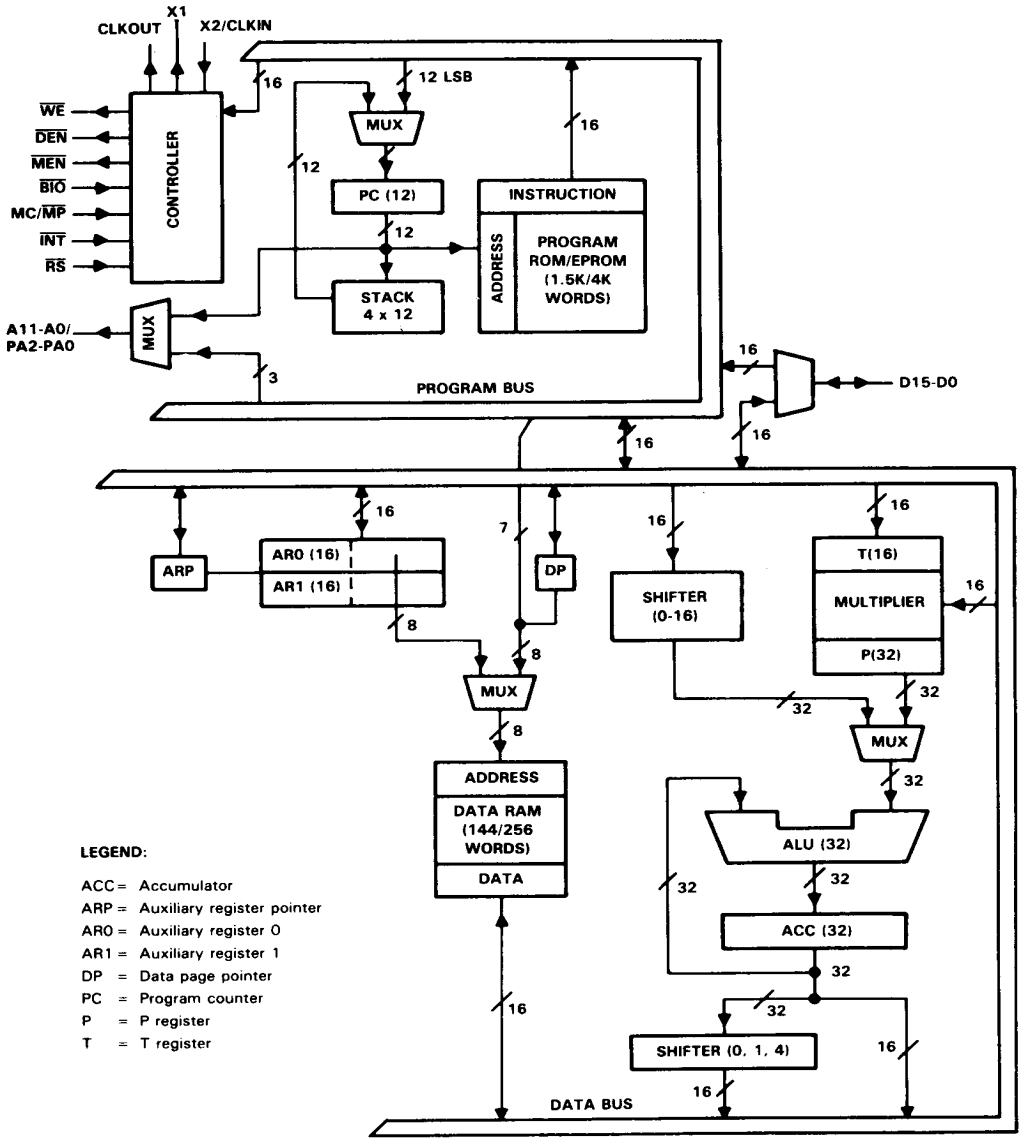


PIN NOMENCLATURE (TMS32010, TMS320C10, TMS320C15, TMS320E15†)

NAME	I/O‡	DEFINITION
A11-A0/PA2-PA0	O	External address bus. I/O port address multiplexed over PA2-PA0.
$\overline{BIO}$	I	External polling input
CLKOUT	O	System clock output, ¼ crystal/CLKIN frequency
D15-D0	I/O	16-bit parallel data bus
$\overline{DEN}$	O	Data enable for device input data on D15-D0
$\overline{INT}$	I	External interrupt input
MC/$\overline{MP}$	I	Memory mode select pin. High selects microcomputer mode. Low selects microprocessor mode.
$\overline{MEN}$	O	Memory enable indicates that D15-D0 will accept external memory instruction.
NC	O	No connection
$\overline{RS}$	I	Reset for initializing the device
V_{CC}	I	+5 V supply
V_{SS}	I	Ground
$\overline{WE}$	O	Write enable for device output data on D15-D0
X1	O	Crystal output for internal oscillator
X2/CLKIN	I	Crystal input for internal oscillator or external system clock input

†See EPROM programming section.
‡Input/Output/High-impedance state.

functional block diagram (TMS32010, TMS320C10, TMS320C15, TMS320E15)



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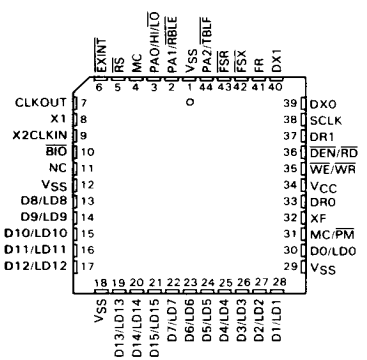
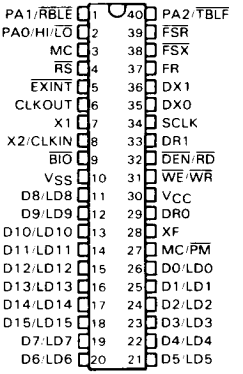
description

The TMS320C17, like the TMS320C15, has 256 words of on-chip data RAM and 4K words of on-chip program ROM. The TMS320C17 is object-code compatible with the TMS32010. The TMS320C17 provides a dual-channel serial port and is designed specifically to interface to two combo-codecs. A 16-bit coprocessor interface is also provided for interfacing to common 4/8/16/32-bit microcomputers/microprocessors.

TMS320C17, TMS320E17
FN AND FZ PACKAGES
(TOP VIEW)



TMS320C17, TMS320E17
N/JD PACKAGE
(TOP VIEW)

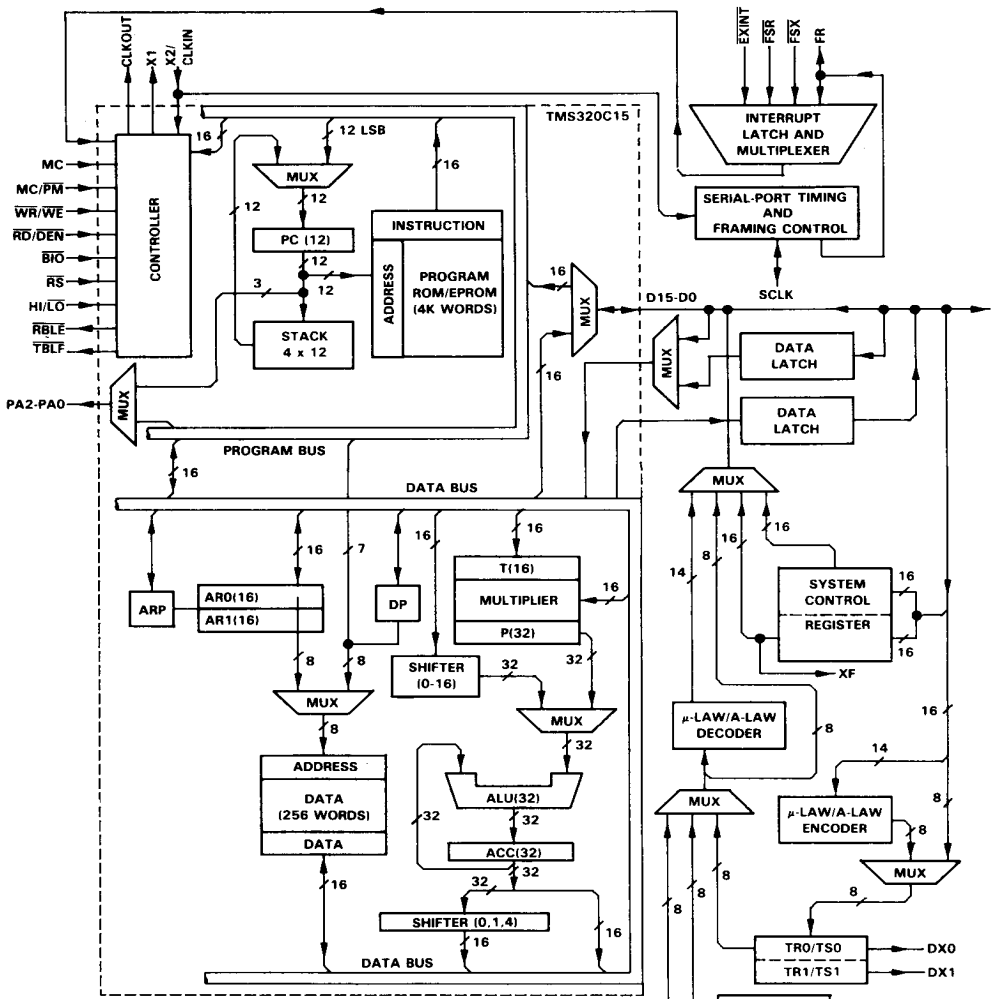


PIN NOMENCLATURE (TMS320C17, TMS320E17†)

NAME	I/O‡	DEFINITION
BIO	I	External polling input
CLKOUT	O	System clock output, ¼ crystal/CLKIN frequency
D15/LD15-D0/LD0	I/O	16-bit parallel data bus/data lines for coprocessor latch
DEN/RD	I/O	Data enable for device input data/external read for output latch
DR1, DR0	I	Serial-port receive-channel inputs
DX1, DX0	O	Serial-port transmit-channel outputs
EXINT	I	External interrupt input
FR	O	Internal serial-port framing output
FSR	I	External serial-port receive framing input
FSX	I	External serial-port transmit framing input
MC	I	Microcomputer select (must be same state as MC/PM)
MC/PM	I	Microcomputer/peripheral coprocessor select (must be same state as MC)
PA0/HI/LO	I/O	I/O port address output/latch byte select pin
PA1/RBLE	O	I/O port address output/receive buffer latch empty flag
PA2/TBLF	O	I/O port address output/transmit buffer latch full flag
RS	I	Reset for initializing the device
SCLK	I/O	Serial-port clock
VCC	I	+5 V Supply
VSS	I	Ground
WE/WR	O	Write enable for device output data/external write for input latch
X1	O	Crystal output for internal oscillator
X2/CLKIN	I	Crystal input for internal oscillator or external oscillator system clock input
XF	O	External-flag output pin

†See EPROM programming section.
‡Input/Output/High-impedance state.

functional block diagram (TMS320C17, TMS320E17)



LEGEND:

ACC = ACCUMULATOR	PC = PROGRAM COUNTER
ARP = AUXILIARY REGISTER POINTER	P = P REGISTER
AR0 = AUXILIARY REGISTER 0	T = T REGISTER
AR1 = AUXILIARY REGISTER 1	TR = TRANSMIT REGISTER
DP = DATA PAGE POINTER	RR = RECEIVE REGISTER

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architecture

The TMS320C17 consists of five major functional units: the TMS320C15 microcomputer, a system control register, a full-duplex dual-channel serial port, companding hardware, and a coprocessor port.

Three of the I/O ports are used by the serial port, companding hardware, and the coprocessor port. Their operation is determined by the 32 bits of the system control register (see Table 5 for the TMS320C17/E17 control register bit definitions). Control register 0, accessed through port 0, consists of the lower 16 register bits (CR15-CR0 bit), and is used to control the interrupts, serial port connections, and companding hardware operation. Port 1 accesses control register 1, consisting of the upper 16 control bits (CR31-CR16), as well as both serial port channels, the companding hardware, and the coprocessor port channels. Communication with the control register is via IN and OUT instructions to ports 0 and 1.

Interrupts fully support the TMS320C17/E17 serial port interface. Four maskable interrupts ($\overline{\text{EXINT}}$, FR, $\overline{\text{FSX}}$, and $\overline{\text{FSR}}$) are mapped into I/O port 0 via control register 0. When disabled, these interrupts may be used as single-bit logic inputs polled by software.

serial port

The dual-channel serial port is capable of full-duplex serial communication and offers direct interface to two combo-codecs. Two receive and two transmit registers are mapped into I/O port 1, and operate with 8-bit data samples. Internal and external framing signals for serial port transfers (MSB first) are selected via the system control register. The serial port clock, SCLK, provides the bit timing for transfers with the serial port, and may be either an input or output. As an input, an external clock provides the timing for data transfers and framing pulse synchronization. As an output, SCLK provides the timing for standalone serial communication and is derived from the TMS320C17/E17 system clock, X2/CLKIN and system control register bits CR27-CR24 (see Table 6 for the available divide ratios). The internal framing (FR) pulse frequency is derived from the serial port clock (SCLK) and system control register bits CR23-CR16. This framing pulse signal provides framing pulses for combo-codecs, for a sample clock for voice-band systems, or for a timer used in control applications.

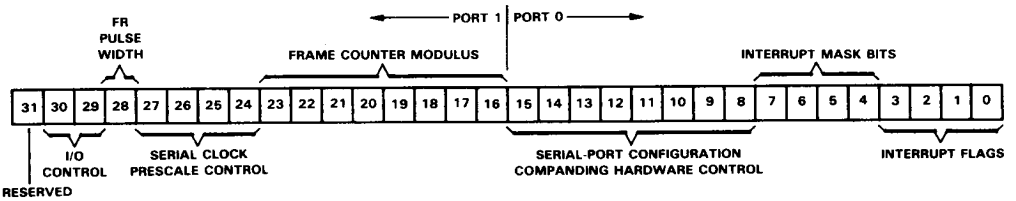
μ-law/A-law companding hardware

The TMS320C17/E17 features hardware companding logic that can operate in either μ-law or A-law format with either sign-magnitude or two's-complement numbers. Data may be companded in either a serial mode for operation on serial port data or a parallel mode for computation inside the device. The companding logic operation is selected through CR14. No bias is required when operating in two's-complement. A bias of 33 is required for sign-magnitude in μ-law companding. Upon reset, the device is programmed to operate in sign-magnitude mode. This mode can be changed by modifying control bit 29 (CR29) in control register 1. For further information on companding, see the *TCM29C13/TCM29C14/TCM29C16/TCM29C17 Combined Single-Chip PCM Codec and Filter Data Sheet*, and the application report, *"Companding Routines for the TMS32010/TMS32020,"* in the book, *Digital Signal Processing Applications with the TMS320 Family* (SPRA012A), both documents published by Texas Instruments.

In the serial mode, sign-magnitude linear PCM (13 magnitude bits plus 1 sign bit for μ-law format or 12 magnitude bits plus 1 sign bit for A-law format) is compressed to 8-bit sign-magnitude logarithmic PCM by the encoder and sent to the transmit register for transmission on an active framing pulse. The decoder converts 8-bit sign-magnitude log PCM from the serial port receive registers to sign-magnitude linear PCM.

In the parallel mode, the serial port registers are disabled to allow parallel data from internal memory to be encoded or decoded for computation inside the device. In the parallel encode mode, the encoder is enabled and a 14-bit sign-magnitude value written to port 1. The encoded value is returned with an IN instruction from port 1. In the parallel decode mode, the decoder is enabled and an 8-bit sign-magnitude log PCM value written to port 1. On the successive IN instruction from port 1, the decoded value is returned. At least one instruction should be inserted between an OUT and the successive IN when companding is performed with two's-complement values.

TABLE 5. CONTROL REGISTER CONFIGURATION



BIT	DESCRIPTION AND CONFIGURATION
0	$\overline{\text{EXINT}}$ interrupt flag†
1	$\overline{\text{FSR}}$ interrupt flag†
2	$\overline{\text{FSX}}$ interrupt flag†
3	FR interrupt flag†
4	$\overline{\text{EXINT}}$ interrupt enable mask. When set to logic 1, an interrupt on $\overline{\text{EXINT}}$ activates device interrupt circuitry.
5	$\overline{\text{FSR}}$ interrupt enable mask. Same as $\overline{\text{EXINT}}$ control.
6	$\overline{\text{FSX}}$ interrupt enable mask. Same as $\overline{\text{EXINT}}$ control.
7	FR interrupt enable mask. Same as $\overline{\text{EXINT}}$ control.
8	Port 1 configuration control: 0 = port 1 connects to either serial-port registers or companding hardware. 1 = port 1 accesses CR31-CR16.
9	External framing enable: 0 = serial-port data transfers controlled by active FR. 1 = serial-port data transfers controlled by active $\overline{\text{FSX}}$/$\overline{\text{FSR}}$.
10	XF external logic output flag latch
11	Serial-port enable: 0 = parallel companding mode; serial port disabled. 1 = serial companding mode; serial port registers enabled.
12	μ-law/A-law encoder enable: 0 = disabled. 1 = data written to port 1 is μ-law or A-law encoded.
13	μ-law/A-law decoder enable: 0 = disabled. 1 = data read from port 1 is μ-law or A-law decoded.
14	μ-law or A-law encode/decode select: 0 = companding hardware performs μ-law conversion. 1 = companding hardware performs A-law conversion.
15	Serial clock control: 0 = SCLK is an output, derived from the prescaler in timing logic. 1 = SCLK is an input that provides the clock for serial port and frame counter in timing logic.
23-16	Frame counter modulus. Controls FR frequency = SCLK/(CNT + 2) where CNT is binary value of CR23-CR16.‡
27-24	SCLK prescale control bits. (See Table 6 for divide ratios.)
28	FR pulse-width control: 0 = fixed-data rate; FR is 1 SCLK cycle wide. 1 = variable-data rate; FR is 8 SCLK cycles wide.
29	Two's-complement μ-law/A-law conversion enable: 0 = sign-magnitude companding 1 = two's-complement companding
30	8/16-bit length coprocessor mode select: 0 = 8-bit byte length 1 = 16-bit word length
31	Reserved for future expansion: Should be set zero.

† Interrupt flag is cleared by writing a logic 1 to the bit with an OUT instruction to port 0.
‡ All ones in CR23-CR16 indicate a degenerative state and should be avoided. Bits are operational whether SCLK is an input or an output. CNT must be greater than 7.

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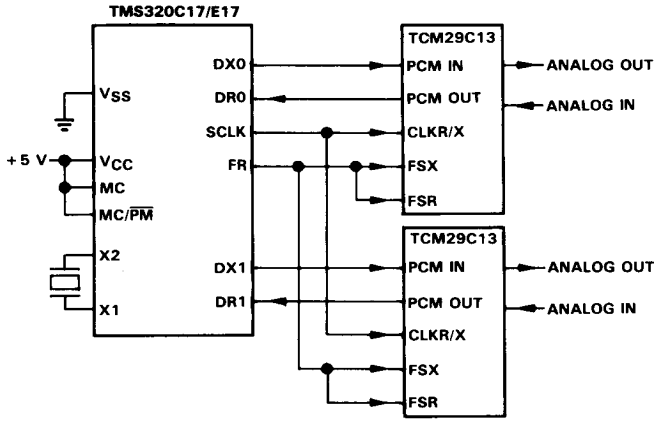
TABLE 6. SERIAL CLOCK (SCLK) DIVIDE RATIOS (X2/CLKIN = 20.48 MHZ)

CR27	CR26	CR25	CR24	DIVIDE RATIO	SCLK FREQUENCY	UNIT
0	0	0	0	32	0.640	MHz
0	0	0	1	28	0.731	MHz
0	0	1	0	24	0.853	MHz
0	1	0	0	20	1.024	MHz
1	0	0	0	16	1.280	MHz
1	0	0	1	14	1.463	MHz
1	0	1	0	12	1.706	MHz
1	1	0	0	10	2.048	MHz

The specification for μ-law and A-law log PCM coding is part of the CCITT G.711 recommendation. The following diagram shows a TMS320C17/E17 interface to two codecs as used for μ-law or A-law companding format.



coprocessor port

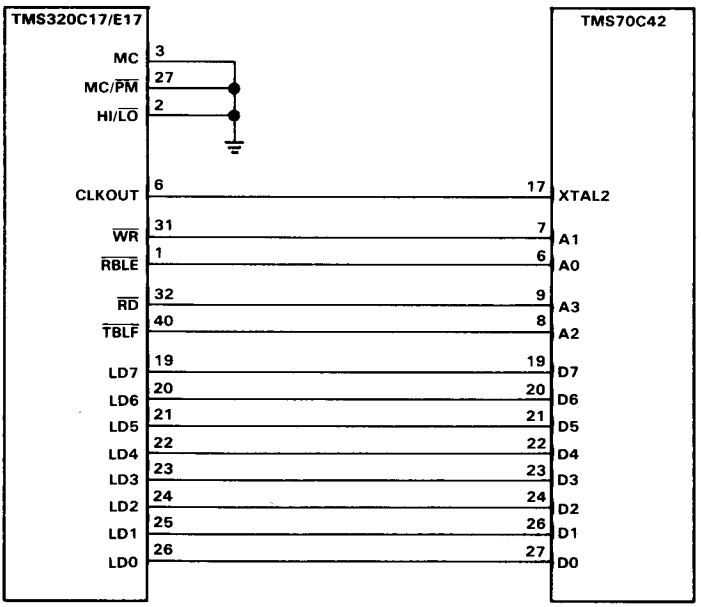
The coprocessor port, accessed through I/O port 5 using IN and OUT instructions, provides a direct connection to most 4/8-bit microcomputers and 16/32-bit microprocessors. The coprocessor interface allows the TMS320C17/E17 to act as a peripheral (slave) microcomputer to a microprocessor, or a master to a peripheral microcomputer such as TMS7042. The coprocessor port is enabled by setting MC/$\overline{\text{PM}}$ and MC low. The microcomputer mode is enabled by setting these two pins high. (Note that MC/$\overline{\text{PM}}$ $\neq$ MC is undefined.) In the microcomputer mode, the 16 data lines are used for the 6 parallel 16-bit I/O ports.

In the coprocessor mode, the 16-bit coprocessor port is reconfigured to operate as a 16-bit latched bus interface. Control bit 30 (CR30) in control register 1 is used to configure the coprocessor port to either an 8-bit or a 16-bit length. When CR30 is high, the coprocessor port is 16 bits wide, thereby making all 16 bits of the data port available for 16-bit transfers to 16 and 32-bit microprocessors. When CR30 is low, the port is 8 bits wide and mapped to the low byte of the data port for interfacing to 8-bit microcomputers. When operating in the 8-bit mode, both halves of the 16-bit latch can be addressed using the HI/$\overline{\text{LO}}$ pin, thus allowing 16-bit transfers over 8 data lines. When not in the coprocessor mode, port 5 can be used as a generic I/O port.

coprocessor port (continued)

The external processor recognizes the coprocessor interface, in which both processors run asynchronously, as a memory-mapped I/O operation. The external processor lowers the $\overline{WR}$ line and places data on the bus. It next raises the $\overline{WR}$ line to clock the data into the on-chip latch. The rising edge of $\overline{WR}$ automatically creates an interrupt to the TMS320C17/E17, and the falling edge of $\overline{WR}$ clears the $\overline{RBLE}$ (receive buffer latch empty) flag. When the TMS320C17/E17 reads the coprocessor port, it causes the $\overline{RBLE}$ signal to transition to a logic low state clears the data in the latch, and allows the interrupt condition to be cleared internally. Likewise, the external processor reads from the latch by driving the $\overline{RD}$ line active low, thus enabling the output latch to drive the latched data. When the data has been read, the external device will again bring the $\overline{RD}$ line high. This activates the $\overline{BIO}$ line to signal that the transfer is complete and the latch is available for the next transfer. The falling edge of $\overline{RD}$ resets the $\overline{TBLF}$ (transmit buffer latch full) flag. Note that the $\overline{EXINT}$ and $\overline{BIO}$ lines are reserved for coprocessor interface and cannot be driven externally when in the coprocessor mode.

An example of the use of a coprocessor interface is shown below, in which the TMS320C17/E17 is interfaced to the TMS70C42, an 8-bit microcontroller.



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NMOS DEVICE ELECTRICAL SPECIFICATIONS

This section contains all the electrical specifications for the TMS320 NMOS first-generation devices. Refer to the top corner for the specific device.

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}‡ . . . . . −0.3 V to 7 V
Input voltage range . . . . . −0.3 V to 15 V
Output voltage range . . . . . −0.3 V to 15 V
Continuous power dissipation . . . . . 1.5 W
Air temperature range above operating device . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to +150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permananet damage to the device. This is a stress rating only, and functional operation of the device or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except CLKIN	2			V
		CLKIN	2.8			
V_{IL}	Low-level input voltage (all inputs)				0.8	V
I_{OH}	High-level output current (all outputs)				−300	μA
I_{OL}	Low-level output current (all outputs)				2	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		2.4	3		V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.3	0.5	V
I_{OZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V			20	μA
				V_O = 0.4 V			−20	
I_I	Input current		V_I = V_{SS} to V_{CC}	All inputs except CLKIN			±20	μA
				CLKIN			±50	
I_{CC}‡	Supply current		V_{CC} = MAX	T_A = 0°C		180	275	mA
				T_A = 70°C			235§	
C_i	Input capacitance	Data bus	f = 1 MHz, All other pins 0 V			25§		pF
		All others				15§		
C_o	Output capacitance	Data bus				25§		pF
		All others				10§		

†All typical values except for I_{CC} are at V_{CC} = 5 V, T_A = 25°C.
‡I_{CC} characteristics are inversely proportional to temperature; i.e., I_{CC} decreases approximately linearly with temperature.
§Value derived from characterization data and not tested.

PARAMETER MEASUREMENT INFORMATION

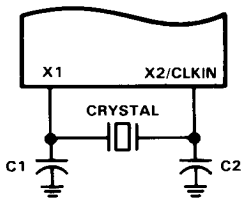

FIGURE 1. INTERNAL CLOCK OPTION

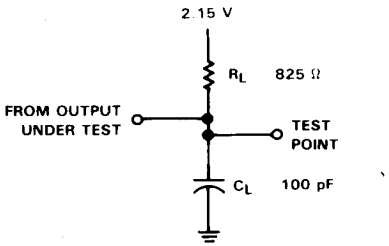

FIGURE 2. TEST LOAD CIRCUIT

input synchronization requirements

For systems using asynchronous inputs to the $\overline{INT}$ and $\overline{BIO}$ pins on the TMS32010, the external hardware shown in the diagrams below is recommended to ensure proper execution of interrupts and the BIOZ instruction. This hardware synchronizes the $\overline{INT}$ and $\overline{BIO}$ input signals with the rising edge of CLKOUT on the TMS32010. The pulse width required for these input signals is $t_{C(C)}$, which is one TMS32010 clock cycle, plus sufficient setup time for the flip-flop (dependent upon the flip-flop used). Note that these input synchronization requirements apply only to NMOS versions of the TMS32010 and not to other members of the TMS320 family.

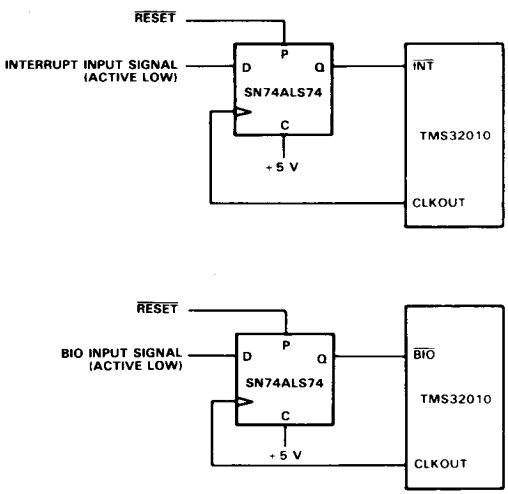

FIGURE 3. ASYNCHRONOUS INPUT SYNCHRONIZATION CIRCUITS

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CLOCK CHARACTERISTICS AND TIMING

The TMS32010 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER	TEST CONDITIONS	TMS32010			UNIT
		MIN	NOM	MAX	
Crystal frequency, f_x	0°C to 70°C	6.7		20.5	MHz
C1, C2	0°C to 70°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS32010			UNIT
			MIN	NOM	MAX	
$t_{c(C)}$	CLKOUT cycle time†	R_L = 825 Ω, C_L = 100 pF, See Figure 2	195.12	200		ns
$t_{r(C)}$	CLKOUT rise time			10		ns
$t_{f(C)}$	CLKOUT fall time			8		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			92		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			90		ns
$t_{d(MCC)}$	Delay time CLKIN↑ to CLKOUT↓		25‡		60‡	ns

†$t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4*t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
‡Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS32010			UNIT
		MIN	NOM	MAX	
$t_{c(MC)}$	Master clock cycle time	48.78	50	150	ns
$t_{r(MC)}$	Rise time master clock input		5†	10†	ns
$t_{f(MC)}$	Fall time master clock input		5†	10†	ns
$t_{w(MCP)}$	Pulse duration master clock	$0.475t_{c(MC)}$†		$0.525t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration master clock high, $t_{c(MC)}$ = 50 ns		20†		ns
$t_{w(MCH)}$	Pulse duration master clock high, $t_{c(MC)}$ = 50 ns		20†		ns

†Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS32010 MIN	TMS32010 TYP	TMS32010 MAX	UNIT
t_{d1}	Delay time CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF, See Figure 2	10†		50	ns
t_{d2}	Delay time CLKOUT↓ to $\overline{MEN}$↓		¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 15	ns
t_{d3}	Delay time CLKOUT↓ to $\overline{MEN}$↑		−10†		15	ns
t_{d4}	Delay time CLKOUT↓ to $\overline{DEN}$↓		¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 15	ns
t_{d5}	Delay time CLKOUT↓ to $\overline{DEN}$↑		−10†		15	ns
t_{d6}	Delay time CLKOUT↓ to $\overline{WE}$↓		½$t_{c(C)}$ − 5†		½$t_{c(C)}$ + 15	ns
t_{d7}	Delay time CLKOUT↓ to $\overline{WE}$↑		−10†		15	ns
t_{d8}	Delay time CLKOUT↓ to data bus OUT valid				¼$t_{c(C)}$ + 65	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		¼$t_{c(C)}$ − 5†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven				¼$t_{c(C)}$ + 30†	ns
t_v	Data bus OUT valid after CLKOUT↓		¼$t_{c(C)}$ − 10			ns
$t_{h(A\text{-}WMD)}$	Address hold time after $\overline{WE}$↑, $\overline{MEN}$↑ or $\overline{DEN}$↑ (see Note 1)		0			ns
$t_{su(A\text{-}MD)}$	Address bus setup time prior to $\overline{MEN}$↓ or $\overline{DEN}$↓		¼$t_{c(C)}$ − 45			ns

†Values derived from characterization data and not tested.
NOTE 1: Address bus will be valid upon $\overline{WE}$↑, $\overline{DEN}$↑, or $\overline{MEN}$↑.

timing requirements over recommended operating conditions

TEST CONDITIONS			TMS32010 MIN	TMS32010 NOM	TMS32010 MAX	UNIT
$t_{su(D)}$	Setup time data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF, See Figure 2	50			ns
$t_{h(D)}$	Hold time data bus held valid after CLKOUT↓ (see Note 2)		0			ns

NOTE 2: Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓.

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RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time $\overline{DEN}$↑, $\overline{WE}$↑, and $\overline{MEN}$↑ from $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF, See Figure 2			$\frac{1}{2}t_{c(C)}+50^{\dagger}$	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				$\frac{1}{4}t_{c(C)}+50^{\dagger}$	ns

†Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS32010			UNIT
		MIN	NOM	MAX	
$t_{su(R)}$	Reset $\overline{RS}$ setup time prior to CLKOUT (see Note 3)	50			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			ns

NOTE 3: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{INT}$) TIMING

timing requirements over recommended operating conditions

		TMS32010			UNIT
		MIN	NOM	MAX	
$t_{f(INT)}$	Fall time ($\overline{INT}$)			15	ns
$t_{w(INT)}$	Pulse duration $\overline{INT}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time $\overline{INT}$↓ before $\overline{CLKOUT}$↓	50			ns

I/O ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		TMS32010			UNIT
		MIN	NOM	MAX	
$t_{f(IO)}$	Fall time $\overline{BIO}$			15	ns
$t_{w(IO)}$	Pulse duration $\overline{BIO}$	$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time $\overline{BIO}$↓ before CLKOUT↓	50			ns

CMOS DEVICE ELECTRICAL SPECIFICATIONS

This section contains all the electrical specifications for the TMS320 CMOS first-generation devices. Refer to the top corner for the specific device.

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}‡ . . . . . −0.3 V to 7 V
Input voltage range . . . . . −0.3 V to 15 V
Output voltage range . . . . . −0.3 V to 15 V
Continuous power dissipation: 20-MHz version . . . . . 0.3 W
25-MHz version . . . . . 0.35 W
Air temperature range above operating device: L version . . . . . 0°C to 70°C
A version . . . . . −40°C to 85°C
Storage temperature range . . . . . −55°C to +150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	EPROM devices	4.75	5	5.25	V
		All other devices	4.5	5	5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except CLKIN	2			V
		CLKIN	3			
V_{IL}	Low-level input voltage	All inputs except MC/$\overline{MP}$			0.8	V
		MC/$\overline{MP}$			0.6	
I_{OH}	High-level output current (all outputs)				−300	μA
I_{OL}	Low-level output current (all outputs)				2	mA
T_A	Operating free-air temperature	L version	0		70	°C
		A version	−40		85	°C

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = MAX		2.4	3		V
			I_{OH} = 20 μA (see Note 4)		V_{CC}−0.4‡			V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.3	0.5	V
I_{OZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V			20	μA
				V_O = 0.4 V			−20	
I_I	Input current		V_I = V_{SS} to V_{CC}	All inputs except CLKIN			±20	μA
				CLKIN			±50	
C_i	Input capacitance	Data bus	f = 1 MHz, All other pins 0 V			25‡		pF
		All others				15‡		
C_o	Output capacitance	Data bus				25‡		pF
		All others				10‡		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Values derived from characterization data and not tested.
NOTE 4: This voltage specification is included for interface to HC logic. However, note that all of the other timing parameters defined in this data sheet are specified for TTL logic levels and will differ for HC logic levels.

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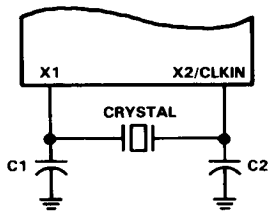

FIGURE 4. INTERNAL CLOCK OPTION

PARAMETER MEASUREMENT INFORMATION

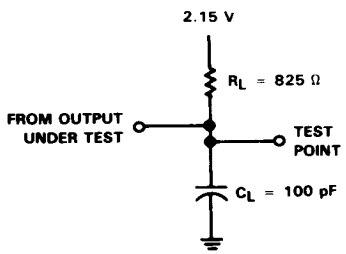

FIGURE 5. TEST LOAD CIRCUIT

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}‡ Supply current	TMS320C10	f = 20.5 MHz, V_{CC} = 5.5 V, T_A = −40°C to 85°C		33	55	mA
	TMS320C10-25	f = 25.6 MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C		40	65	mA

†All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependance on temperature, frequency, and loading, see Figure 9.

CLOCK CHARACTERISTICS AND TIMING

The TMS320C10/C10-25 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 4). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_x	TMS320C10	T_A = −40°C to 85°C	6.7		20.5	MHz
	TMS320C10-25	T_A = 0°C to 70°C	6.7		25.6	MHz
C1, C2		T_A = −40°C to 85°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C10			TMS320C10-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(C)}$	CLKOUT cycle time†	R_L = 825 Ω, C_L = 100 pF, See Figure 5	195.12	200		156.25	160		ns
$t_{r(C)}$	CLKOUT rise time			10‡			10‡		ns
$t_{f(C)}$	CLKOUT fall time			8‡			8‡		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			92‡			72‡		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			90‡			70‡		ns
$t_{d(MCC)}$	Delay time CLKIN↑ to CLKOUT↓		25‡		60‡	25‡		50‡	ns

†$t_{c(C)}$ is the cycle time of CLKOUT, i.e., 4*$t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
‡Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS320C10			TMS320C10-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(MC)}$	Master clock cycle time	48.78	50	150	39.06	40	150	ns
$t_{r(MC)}$	Rise time master clock input		5†	10†		5†	10†	ns
$t_{f(MC)}$	Fall time master clock input		5†	10†		5†	10†	ns
$t_{w(MCP)}$	Pulse duration master clock	0.4$t_{c(MC)}$†		0.6$t_{c(MC)}$†	0.45$t_{c(MC)}$†		0.55$t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration master clock low		20†			15†		ns
$t_{w(MCH)}$	Pulse duration master clock high		20†			15†		ns

†Values derived from characterization data and not tested.

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POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C10			TMS320C10-25			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{d1}	Delay time CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF, See Figure 5	10†		50	10†		40	ns
t_{d2}	Delay time CLKOUT↓ to $\overline{MEN}$↓		¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 15	¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 12	ns
t_{d3}	Delay time CLKOUT↓ to $\overline{MEN}$↑		−10†		15	−10†		12	ns
t_{d4}	Delay time CLKOUT↓ to $\overline{DEN}$↓		¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 15	¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 12	ns
t_{d5}	Delay time CLKOUT↓ to $\overline{DEN}$↑		−10†		15	−10†		12	ns
t_{d6}	Delay time CLKOUT↓ to $\overline{WE}$↓		¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 15	½$t_{c(C)}$ − 5†		½$t_{c(C)}$ + 12	ns
t_{d7}	Delay time CLKOUT↓ to $\overline{WE}$↑		−10†		15	−10†		12	ns
t_{d8}	Delay time CLKOUT↓ to data bus OUT valid				¼$t_{c(C)}$ + 65			¼$t_{c(C)}$ + 52	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		¼$t_{c(C)}$ − 5†			¼$t_{c(C)}$ − 5†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven				¼$t_{c(C)}$ + 40†			¼$t_{c(C)}$ + 40†	ns
t_v	Data bus OUT valid after CLKOUT↓		¼$t_{c(C)}$ − 10			¼$t_{c(C)}$ − 10			ns
$t_{h(A\text{-}WMD)}$	Address hold time after $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑ (see Note 5)		−10†			−10†			ns
$t_{su(A\text{-}MD)}$	Address bus setup time prior to $\overline{MEN}$↓ or $\overline{DEN}$↓		¼$t_{c(C)}$ − 45			¼$t_{c(C)}$ − 35			ns

†Values derived from characterization data and not tested.
NOTE 5: For interfacing I/O devices, see Figure 6.

timing requirements over recommended operating conditions

		TEST CONDITIONS	TMS320C10			TMS320C10-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{su(D)}$	Setup time data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF, See Figure 5	50			40			ns
$t_{h(D)}$	Hold time data bus held valid after CLKOUT↓ (see Note 2)		0			0			ns

NOTE 2: Data may be removed from the data bus upor $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓.

SUGGESTED I/O DECODE CIRCUIT

The circuit shown in Figure 6 is a design example for interfacing I/O devices to the TMS320C10/C10-25. This circuit decodes the address for output operations using the OUT instruction. The same circuit can be used to decode input and output operations if the inverter ('ALS04) is replaced with a NAND gate and both $\overline{DEN}$ and $\overline{WE}$ are connected. Inputs and outputs can be decoded at the same port provided the output of the decoder ('AS137) is gated with the appropriate signal ($\overline{DEN}$ or $\overline{WE}$) to select read or write (using an 'ALS32). Access times can be increased when the circuit shown in Figure 6 is repeated to support IN instructions with $\overline{DEN}$ connected rather than $\overline{WE}$.

The table write (TBLW) function requires a different circuit. A detailed discussion of an example circuit for this function is described on page 315 of the application report, "Interfacing External Memory to the TMS32010," published in the book, *Digital Signal Processing Applications with the TMS320 Family* (SPRA012A). A schematic of this circuit is shown on page 318 of that book.

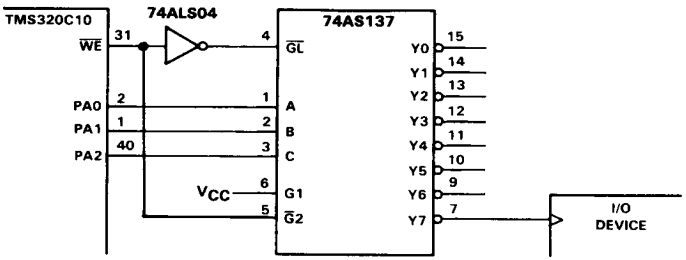

FIGURE 6. I/O DECODE CIRCUIT

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time $\overline{DEN}$↑, $\overline{WE}$↑, and $\overline{MEN}$↑ from $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF, See Figure 5			½$t_{c(C)}$ + 50†	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				¼$t_{c(C)}$ + 50†	ns

†These values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS320C10			TMS320C10-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 3)	50			40			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	5$t_{c(C)}$			5$t_{c(C)}$			ns

NOTE 3: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{INT}$) TIMING

timing requirements over recommended operating conditions

		TMS320C10			TMS320C10-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{f(INT)}$	Fall time $\overline{INT}$			15			15	ns
$t_{w(INT)}$	Pulse duration $\overline{INT}$	$t_{c(C)}$			$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time $\overline{INT}$↓ before CLKOUT↓	50			40			ns

I/O ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		TMS320C10			TMS320C10-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{f(IO)}$	Fall time $\overline{BIO}$			15			15	ns
$t_{w(IO)}$	Pulse duration $\overline{BIO}$	$t_{c(C)}$			$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time $\overline{BIO}$↓ before CLKOUT↓	50			40			ns

TEXAS INSTRUMENTS
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electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}‡ Supply current	f = 14.4 MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C		28	55	mA

†All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependence on temperature, frequency, and loading, see Figure 9.

CLOCK CHARACTERISTICS AND TIMING

The TMS320C10-14 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 4). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_x	T_A = 0°C to 70°C	6.7		14.4	MHz
C1, C2	T_A = 0°C to 70°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time†	R_L = 825 Ω, C_L = 100 pF, See Figure 5	277.78			ns
$t_{r(C)}$	CLKOUT rise time			10		ns
$t_{f(C)}$	CLKOUT fall time			8		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			131		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			129		ns
$t_{d(MCC)}$	Delay time CLKIN↑ to CLKOUT↓		25‡		60‡	ns

†$t_{c(C)}$ is the cycle time of CLKOUT, i.e., 4*$t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
‡Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time	69.5		150	ns
$t_{r(MC)}$	Rise time master clock input		5†	10†	ns
$t_{f(MC)}$	Fall time master clock input		5†	10†	ns
$t_{w(MCP)}$	Pulse duration master clock	0.4$t_{c(MC)}$†		0.6$t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration master clock low, $t_{c(MC)}$ = 50 ns		20†		ns
$t_{w(MCH)}$	Pulse duration master clock high, $t_{c(MC)}$ = 50 ns		20†		ns

†Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF, See Figure 5	10†		50	ns
t_{d2}	Delay time CLKOUT↓ to $\overline{MEN}$↓		¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 15	ns
t_{d3}	Delay time CLKOUT↓ to $\overline{MEN}$↑		−10†		15	ns
t_{d4}	Delay time CLKOUT↓ to $\overline{DEN}$↓		¼$t_{c(C)}$ − 5†		¼$t_{c(C)}$ + 15	ns
t_{d5}	Delay time CLKOUT↓ to $\overline{DEN}$↑		−10†		15	ns
t_{d6}	Delay time CLKOUT↓ to $\overline{WE}$↓		½$t_{c(C)}$ − 5†		½$t_{c(C)}$ + 15	ns
t_{d7}	Delay time CLKOUT↓ to $\overline{WE}$↑		−10†		15	ns
t_{d8}	Delay time CLKOUT↓ to data bus OUT valid				¼$t_{c(C)}$ + 65	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		¼$t_{c(C)}$ − 5†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven				¼$t_{c(C)}$ + 40†	ns
t_v	Data bus OUT valid after CLKOUT↓		¼$t_{c(C)}$ − 10			ns
$t_{h(A\text{-}WMD)}$	Address hold time after $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑ (see Note 5)		−10†			ns
$t_{su(A\text{-}MD)}$	Address bus setup time prior to $\overline{MEN}$↓ or $\overline{DEN}$↓		¼$t_{c(C)}$ − 45			ns

†Values derived from characterization data and not tested.
NOTE 5: For interfacing I/O devices, see Figure 6.

timing requirements over recommended operating conditions

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(D)}$	Setup time data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF, See Figure 5	50			ns
$t_{h(D)}$	Hold time data bus held valid after CLKOUT↓ (see Note 2)		0			ns

NOTE 2: Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓.

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RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time $\overline{DEN}$↑, $\overline{WE}$↑, and $\overline{MEN}$↑ from $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF, See Figure 5			½$t_{c(C)}$ + 50†	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				¼$t_{c(C)}$ + 50†	ns

†These values were derived from characterization data and not tested.

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 3)	50			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	5$t_{c(C)}$			ns

NOTE 3: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{INT}$) TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(INT)}$	Fall time $\overline{INT}$			15	ns
$t_{w(INT)}$	Pulse duration $\overline{INT}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time $\overline{INT}$↓ before CLKOUT↓	50			ns

I/O ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(IO)}$	Fall time $\overline{BIO}$			15	ns
$t_{w(IO)}$	Pulse duration $\overline{BIO}$	$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time $\overline{BIO}$↓ before CLKOUT↓	50			ns

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}‡ Supply current	TMS320C15	f = 20.5 MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C		45	55	mA
	TMS320C15-25	f = 25.6 MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C		50	65	
	TMS320E15	f = 20.5 MHz, V_{CC} = 5.25 V, T_A = −40°C to 85°C		55	75	
	TMS320E15-25	f = 25.6 MHz, V_{CC} = 5.25 V, T_A = 0°C to 70°C		65	85	

†All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependence on temperature, frequency, and loading, see Figure 9.

CLOCK CHARACTERISTICS AND TIMING

The TMS320C15/E15 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 4). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_x	TMS320C15	T_A = 0°C to 70°C	6.7		20.5	MHz
	TMS320E15	T_A = −40°C to 85°C	6.7		20.5	MHz
	TMS320C15-25/E15-25	T_A = 0°C to 70°C	6.7		25.6	MHz
C1, C2		T_A = 0°C to 70°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C15/E15			TMS320C15-25/E15-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(C)}$	CLKOUT cycle time†	R_L = 825 Ω, C_L = 100 pF, See Figure 5	195.12	200		156.25	160		ns
$t_{r(C)}$	CLKOUT rise time			10‡			10‡		ns
$t_{f(C)}$	CLKOUT fall time			8‡			8‡		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			92‡			72‡		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			90‡			70‡		ns
$t_{d(MCC)}$	Delay time CLKIN↑ to CLKOUT↓		25‡		60‡	25‡		50‡	ns

†$t_{c(C)}$ is the cycle time of CLKOUT, i.e., 4*$t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
‡Values derived from characterization data and not tested.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

timing requirements over recommended operating conditions

		TMS320C15/E15			TMS320C15-25/E15-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(MC)}$	Master clock cycle time	48.78	50	150	39.06	40	150	ns
$t_{r(MC)}$	Rise time master clock input		5†	10†		5†	10†	ns
$t_{f(MC)}$	Fall time master clock input		5†	10†		5†	10†	ns
$t_{w(MCP)}$	Pulse duration master clock	$0.4t_{c(MC)}$†		$0.6t_{c(MC)}$†	$0.45t_{c(MC)}$†		$0.55t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration master clock low		20†			15†		ns
$t_{w(MCH)}$	Pulse duration master clock high		20†			15†		ns

†Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C15/E15			TMS320C15-25/E15-25			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{d1}	Delay time CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF, See Figure 5	10†		50	10†		40	ns
t_{d2}	Delay time CLKOUT↓ to $\overline{MEN}$↓		$¼t_{c(C)}-5$†		$¼t_{c(C)}+15$	$¼t_{c(C)}-5$†		$¼t_{c(C)}+12$	ns
t_{d3}	Delay time CLKOUT↓ to $\overline{MEN}$↑		−10†		15	−10†		12	ns
t_{d4}	Delay time CLKOUT↓ to $\overline{DEN}$↓		$¼t_{c(C)}-5$†		$¼t_{c(C)}+15$	$¼t_{c(C)}-5$†		$¼t_{c(C)}+12$	ns
t_{d5}	Delay time CLKOUT↓ to $\overline{DEN}$↑		−10†		15	−10†		12	ns
t_{d6}	Delay time CLKOUT↓ to $\overline{WE}$↓		$½t_{c(C)}-5$†		$½t_{c(C)}+15$	$½t_{c(C)}-5$†		$½t_{c(C)}+12$	ns
t_{d7}	Delay time CLKOUT↓ to $\overline{WE}$↑		−10†		15	−10†		12	ns
t_{d8}	Delay time CLKOUT↓ to data bus OUT valid				$¼t_{c(C)}+65$			$¼t_{c(C)}+52$	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		$¼t_{c(C)}-5$†			$¼t_{c(C)}-5$†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven (TMS320C15/C15-25 only)				$¼t_{c(C)}+40$†			$¼t_{c(C)}+40$†	ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven (TMS320E15/E15-25 only)				$¼t_{c(C)}+70$†			$¼t_{c(C)}+70$†	ns
t_v	Data bus OUT valid after CLKOUT↓		$¼t_{c(C)}-10$			$¼t_{c(C)}-10$			ns
$t_{h(A-WMD)}$	Address hold time after $\overline{WE}$↑, $\overline{MEN}$↑, or $\overline{DEN}$↑ (see Note 1)		0†		2†	0†		2†	ns
$t_{su(A-MD)}$	Address bus setup time prior to $\overline{DEN}$↓		$¼t_{c(C)}-45$			$¼t_{c(C)}-35$			ns

†Values derived from characterization data and not tested.
NOTE 1: Address bus will be valid upon $\overline{WE}$↑, $\overline{DEN}$↑, or $\overline{MEN}$↑.

timing requirements over recommended operating conditions

		TEST CONDITIONS	TMS320C15/E15			TMS320C15-25/E15-25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{su(D)}$	Setup time data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF, See Figure 5	50			40			ns
$t_{h(D)}$	Hold time data bus held valid after CLKOUT↓ (see Note 2)		0			0			ns

NOTE 2: Data may be removed from the data bus upon $\overline{MEM}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓.

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time $\overline{DEN}$↑, $\overline{WE}$↑, and $\overline{MEN}$↑ from $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF, See Figure 5			½$t_{c(C)}$ + 50†	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				¼$t_{c(C)}$ + 50†	ns

†Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS320C15/E15			TMS320C15-25/E15-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 3)	50			40			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	5$t_{c(C)}$			5$t_{c(C)}$			ns

NOTE 3: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{INT}$) TIMING

timing requirements over recommended operating conditions

		TMS320C15/E15			TMS320C15-25/E15-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{f(INT)}$	Fall time $\overline{INT}$			15			15	ns
$t_{w(INT)}$	Pulse duration $\overline{INT}$	$t_{c(C)}$			$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time $\overline{INT}$↓ before CLKOUT↓	50			40			ns

I/O ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		TMS320C15/E15			TMS320C15-25/E15-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{f(IO)}$	Fall time $\overline{BIO}$			15			15	ns
$t_{w(IO)}$	Pulse duration $\overline{BIO}$	$t_{c(C)}$			$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time $\overline{BIO}$↓ before CLKOUT↓	50			40			ns

TEXAS INSTRUMENTS
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electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}‡ Supply current	TMS320C17	f = 20.5 MHz, V_{CC} = 5.5 V, T_A = 0°C to 70°C		50	65	mA
	TMS320E17	f = 20.5 MHz, V_{CC} = 5.25 V, T_A = −40°C to 85°C		55	75	

†All typical values are at T_A = 70°C and are used for thermal resistance calculations.
‡I_{CC} characteristics are inversely proportional to temperature. For I_{CC} dependance on temperature, frequency, and loading, see Figure 9.

CLOCK CHARACTERISTICS AND TIMING

The TMS320C17/E17 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 4). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, f_x	TMS320C17	T_A = 0°C to 70°C	6.7		20.5	MHz
	TMS320E17	T_A = −40°C to 85°C	6.7		20.5	MHz
C1, C2		T_A = 0°C to 70°C		10		pF

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C17/E17			UNIT
			MIN	NOM	MAX	
$t_{c(C)}$	CLKOUT cycle time†	R_L = 825 Ω, C_L = 100 pF, See Figure 5	195.12	200		ns
$t_{r(C)}$	CLKOUT rise time			10‡		ns
$t_{f(C)}$	CLKOUT fall time			8‡		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			92‡		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			90‡		ns
$t_{d(MCC)}$	Delay time CLKIN↑ to CLKOUT↓		25‡		60‡	ns

†$t_{c(C)}$ is the cycle time of CLKOUT, i.e., 4*$t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
‡Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS320C17/E17			UNIT
		MIN	NOM	MAX	
$t_{c(MC)}$	Master clock cycle time	48.78	50	150	ns
$t_{r(MC)}$	Rise time master clock input		5†	10†	ns
$t_{f(MC)}$	Fall time master clock input		5†	10†	ns
$t_{w(MCP)}$	Pulse duration master clock	$0.45t_{c(MC)}$†		$0.6t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration master clock low		20†		ns
$t_{w(MCH)}$	Pulse duration master clock high		20†		ns

†Values derived from characterization data and not tested.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS320C17/E17			UNIT
			MIN	NOM	MAX	
t_{d1}	Delay time CLKOUT↓ to address bus valid	R_L = 825 Ω, C_L = 100 pF, See Figure 5	10†		50	ns
t_{d4}	Delay time CLKOUT↓ to $\overline{DEN}$↓		$¼t_{c(C)}-5$†		$¼t_{c(C)}+15$	ns
t_{d5}	Delay time CLKOUT↓ to $\overline{DEN}$↑		−10†		15	ns
t_{d6}	Delay time CLKOUT↓ to $\overline{WE}$↓		$½t_{c(C)}-5$†		$½t_{c(C)}+15$	ns
t_{d7}	Delay time CLKOUT↓ to $\overline{WE}$↑		−10†		15	ns
t_{d8}	Delay time CLKOUT↓ to data bus OUT valid				$¼t_{c(C)}+65$	ns
t_{d9}	Time after CLKOUT↓ that data bus starts to be driven		$¼t_{c(C)}-5$†			ns
t_{d10}	Time after CLKOUT↓ that data bus stops being driven				$¼t_{c(C)}+70$†	ns
t_v	Data bus OUT valid after CLKOUT↓		$¼t_{c(C)}-10$			ns
$t_{h(A\text{-}WMD)}$	Address hold time after $\overline{WE}$↑ or $\overline{DEN}$↑ (see Note 1)		0†	2†		ns
$t_{su(A\text{-}MD)}$	Address bus setup time prior to $\overline{DEN}$↓		$¼t_{c(C)}-45$			ns

†Values derived from characterization data and not tested.
NOTE 1: Address bus will be valid upon $\overline{WE}$↑, $\overline{DEN}$↑, or $\overline{MEN}$↑.

timing requirements over recommended operating conditions

		TEST CONDITIONS	TMS320C17/E17			UNIT
			MIN	NOM	MAX	
$t_{su(D)}$	Setup time data bus valid prior to CLKOUT↓	R_L = 825 Ω, C_L = 100 pF, See Figure 5	50			ns
$t_{h(D)}$	Hold time data bus held valid after CLKOUT↓ (see Note 2)		0			ns

NOTE 2: Data may be removed from the data bus upon $\overline{DEN}$↑ preceding CLKOUT↓.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

RESET ($\overline{RS}$) TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d11}	Delay time $\overline{DEN}$↑ and $\overline{WE}$↑ from $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF, See Figure 5			$\frac{1}{2}t_{c(C)}+50$†	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				$\frac{1}{4}t_{c(C)}+50$†	ns
t_{d12}	Delay time from $\overline{RS}$↓ to high-impedance SCLK				200†	ns
t_{d13}	Delay time from $\overline{RS}$↓ to high-impedance DX1, DX0				200†	ns

†Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

		TMS320C17/E17			UNIT
		MIN	NOM	MAX	
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT (see Note 3)	50			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			ns

NOTE 3: RS can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

INTERRUPT ($\overline{EXINT}$) TIMING

timing requirements over recommended operating conditions

		TMS320C17/E17			UNIT
		MIN	NOM	MAX	
$t_{f(INT)}$	Fall time $\overline{EXINT}$			15	ns
$t_{w(INT)}$	Pulse duration $\overline{EXINT}$	$t_{c(C)}$			ns
$t_{su(INT)}$	Setup time $\overline{EXINT}$↓ before CLKOUT↓	50			ns

I/O ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		TMS320C17/E17			UNIT
		MIN	NOM	MAX	
$t_{f(IO)}$	Fall time $\overline{BIO}$			15	ns
$t_{w(IO)}$	Pulse duration $\overline{BIO}$	$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time $\overline{BIO}$↓ before CLKOUT↓	50			ns

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(XF)}$	Delay time CLKOUT↓ to valid XF	R_L = 825 Ω, C_L = 100 pF, See Figure 5	5†		115	ns

†Values derived from characterization data and not tested.

SERIAL PORT TIMING

switching characteristics over recommended operating conditions

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CH-FR)}$	Internal framing (FR) delay from SCLK rising edge			70	ns
$t_{d(DX1-CL)}$	DX bit 1 valid before SCLK falling edge	20			ns
$t_{d(DX2-CL)}$	DX bit 2 valid before SCLK falling edge	20			ns
$t_{h(DX)}$	DX hold time after SCLK falling edge	$t_{c(SCLK)}/2$			ns

timing requirements over recommended operating conditions, f = 25 MHz

		MIN	NOM	MAX	UNIT
$t_{c(SCLK)}$	Serial port clock (SCLK) cycle time (see Note 6)	390		4770	ns
$t_{f(SCLK)}$	Serial port clock (SCLK) fall time			30†	ns
$t_{r(SCLK)}$	Serial port clock (SCLK) rise time			30†	ns
$t_{w(SCLKL)}$	Serial port clock (SCLK) low-pulse duration (see Note 7)	185		2500	ns
$t_{w(SCLKH)}$	Serial port clock (SCLK) high-pulse duration (see Note 7)	185		2500	
$t_{su(FS)}$	$\overline{FSX}/\overline{FSR}$ setup time before SCLK falling edge	100			ns
$t_{su(DR)}$	DR setup time before SCLK falling edge	20			ns
$t_{h(DR)}$	DR hold time after SCLK falling edge	20			ns

†Values derived from characterization data and not tested.

NOTES: 6. Minimum cycle time is $2t_{c(C)}$ where $t_{c(C)}$ is CLKOUT cycle time.
7. The duty cycle of the serial port clock must be within 45 to 55 percent.

COPROCESSOR INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
$t_{d(R-A)}$	$\overline{RD}$ low to $\overline{TBLF}$ high			75	ns
$t_{d(W-A)}$	$\overline{WR}$ low to $\overline{RBLE}$ high			75	ns
$t_{a(RD)}$	$\overline{RD}$ low to data valid			80	ns
$t_{h(RD)}$	Data hold time after $\overline{RD}$ high	25			ns

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{h(HL)}$	HI/$\overline{LO}$ hold time after $\overline{WR}$ or $\overline{RD}$ high	25			ns
$t_{su(HL)}$	HI/$\overline{LO}$ setup time prior to $\overline{WR}$ or $\overline{RD}$ low	40			ns
$t_{su(WR)}$	Data setup time prior to $\overline{WR}$ high	30			ns
$t_{h(WR)}$	Data hold time after $\overline{WR}$ high	25			ns
$t_{w(RDL)}$	$\overline{RD}$ low-pulse duration	80			ns
$t_{w(WRL)}$	$\overline{WR}$ low-pulse duration	60			ns

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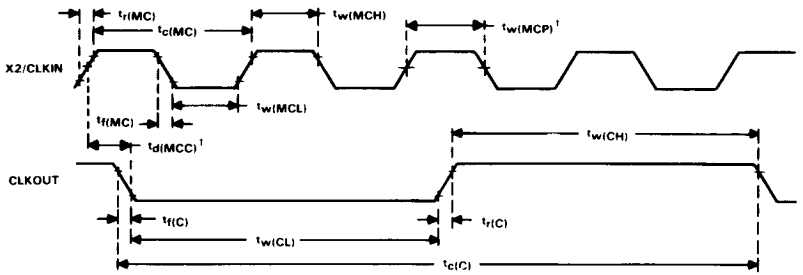
TIMING DIAGRAMS

This section contains all the timing diagrams for the TMS320 first-generation devices. For a specific device, refer to the top corner of pages 46-51.

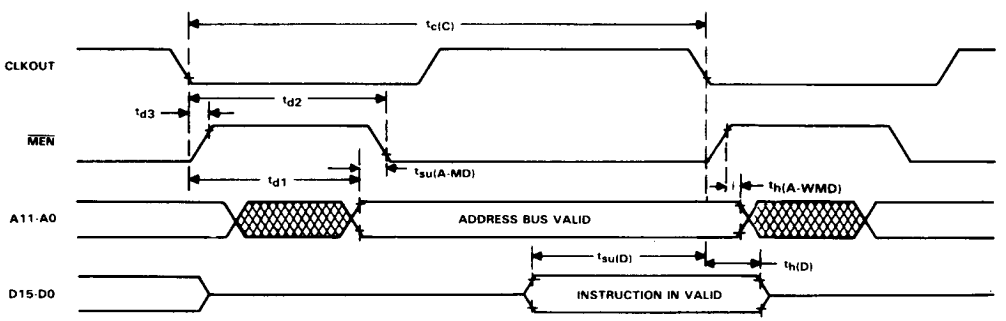
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

clock timing

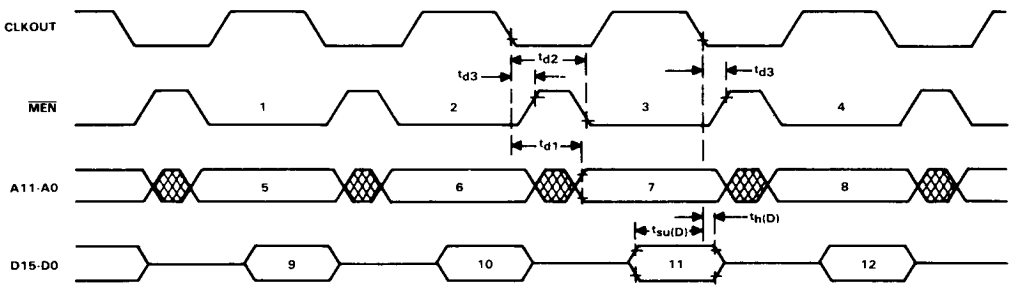


†$t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 volts on the CLKIN waveform.

memory read timing



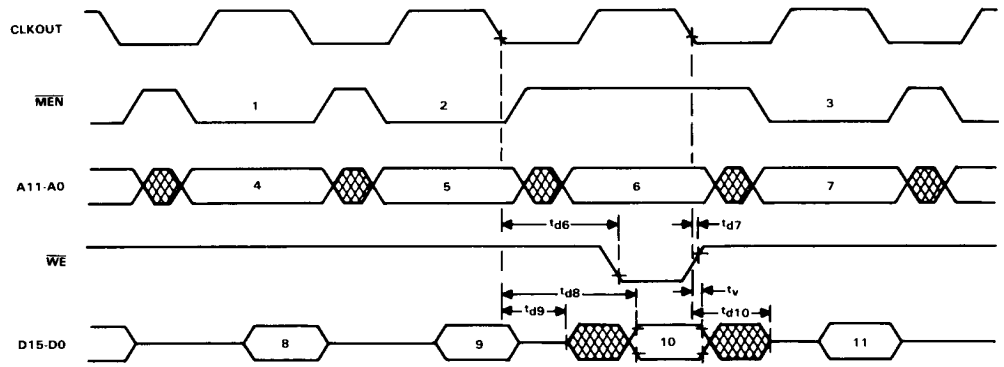
TBLR instruction timing



LEGEND:

1. TBLR INSTRUCTION PREFETCH
2. DUMMY PREFETCH
3. DATA FETCH
4. NEXT INSTRUCTION PREFETCH
5. ADDRESS BUS VALID
6. ADDRESS BUS VALID
7. ADDRESS BUS VALID
8. ADDRESS BUS VALID
9. INSTRUCTION VALID
10. INSTRUCTION VALID
11. DATA INPUT VALID
12. INSTRUCTION VALID

TBLW instruction timing



LEGEND:

1. TBLW INSTRUCTION PREFETCH
2. DUMMY PREFETCH
3. NEXT INSTRUCTION PREFETCH
4. ADDRESS BUS VALID
5. ADDRESS BUS VALID
6. ADDRESS BUS VALID
7. ADDRESS BUS VALID
8. INSTRUCTION VALID
9. INSTRUCTION VALID
10. DATA OUTPUT VALID
11. INSTRUCTION VALID

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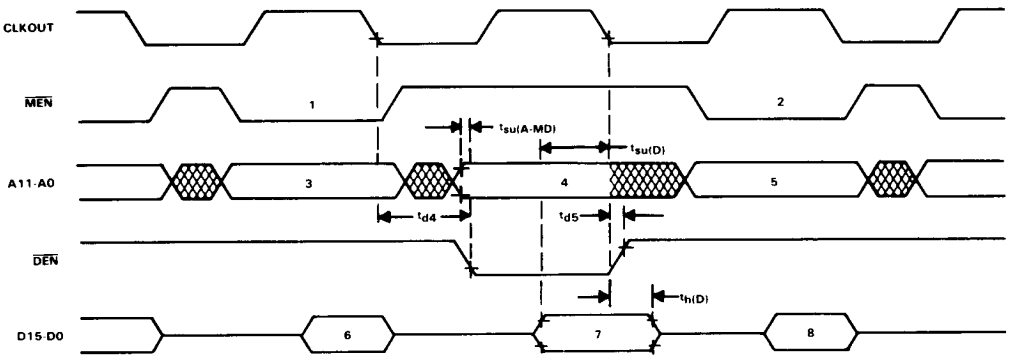
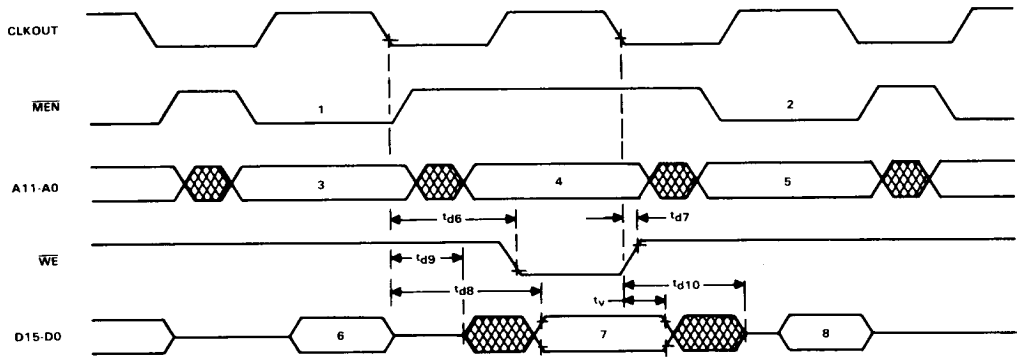
IN instruction timing



LEGEND:

1. IN INSTRUCTION PREFETCH
2. NEXT INSTRUCTION PREFETCH
3. ADDRESS BUS VALID
4. PERIPHERAL ADDRESS VALID
5. ADDRESS BUS VALID
6. INSTRUCTION VALID
7. DATA INPUT VALID
8. INSTRUCTION VALID

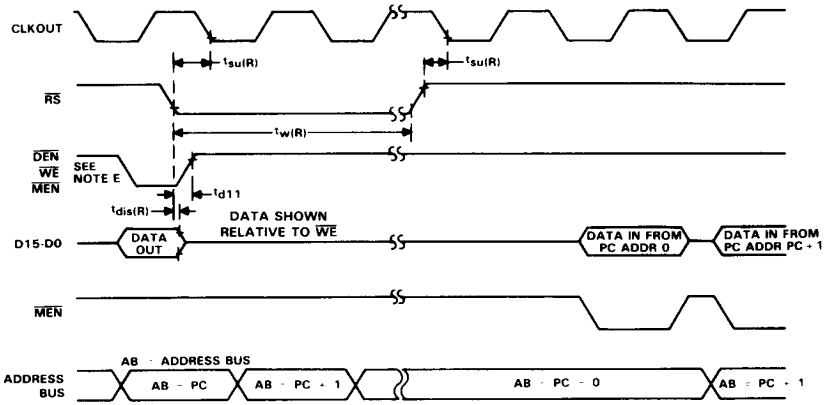
OUT instruction timing



LEGEND:

1. OUT INSTRUCTION PREFETCH
2. NEXT INSTRUCTION PREFETCH
3. ADDRESS BUS VALID
4. PERIPHERAL ADDRESS VALID
5. ADDRESS BUS VALID
6. INSTRUCTION VALID
7. DATA OUTPUT VALID
8. INSTRUCTION VALID

reset timing



NOTES: A. $\overline{RS}$ forces $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ high and places data bus D0 through D15 in a high-impedance state. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from $\overline{RS}\downarrow$.

B. $\overline{RS}$ must be maintained for a minimum of five clock cycles.

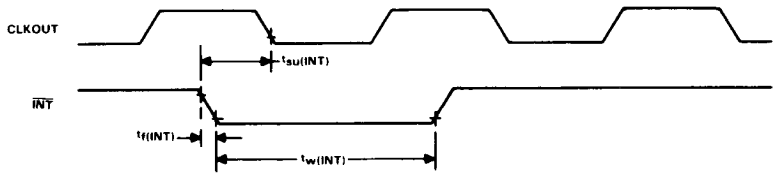
C. Resumption of normal program will commence after one complete CLK cycle from $\overline{RS}\uparrow$.

D. Due to the synchronizing action on $\overline{RS}$, time to execute the function can vary dependent upon when $\overline{RS}\uparrow$ or $\overline{RS}\downarrow$ occur in the CLK cycle.

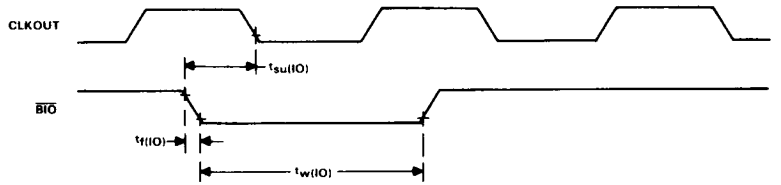
E. Diagram shown is for definition purpose only. $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ are mutually exclusive.

F. During a write cycle, $\overline{RS}$ may produce an invalid write address.

interrupt timing

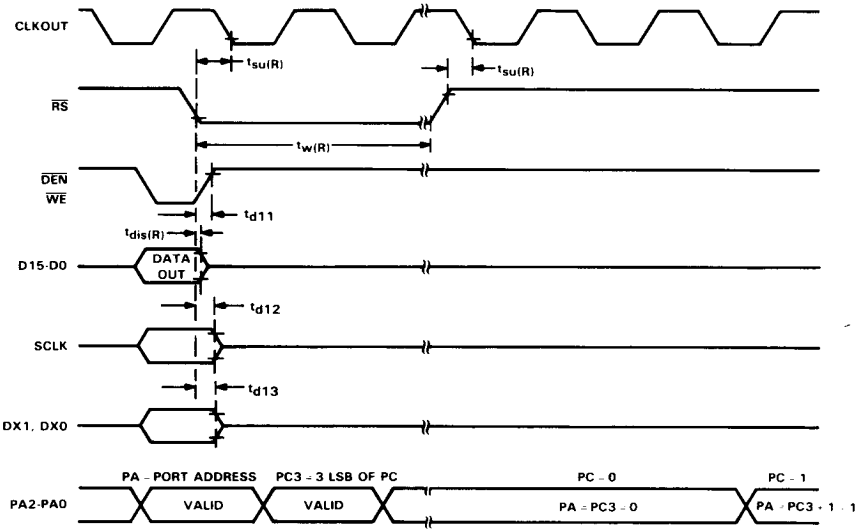


$\overline{BIO}$ timing

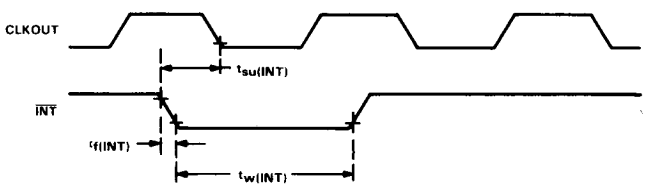


TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

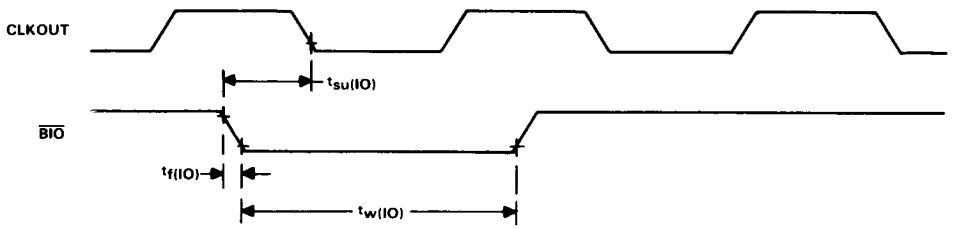
reset timing



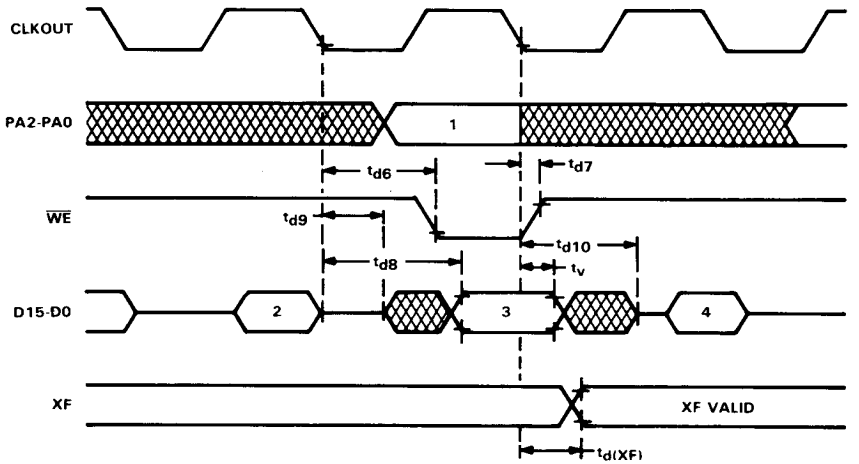
interrupt timing



$\overline{\text{BIO}}$ timing



XF timing



LEGEND:

1. PORT ADDRESS VALID
2. OUT OPCODE VALID
3. PORT DATA VALID
4. NEXT INSTRUCTION OPCODE VALID

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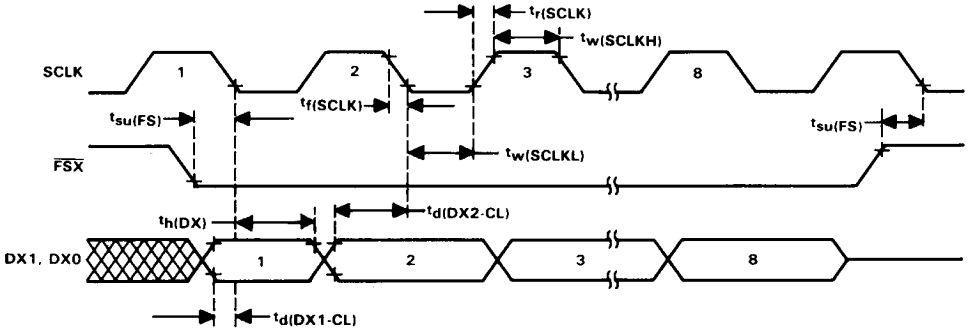
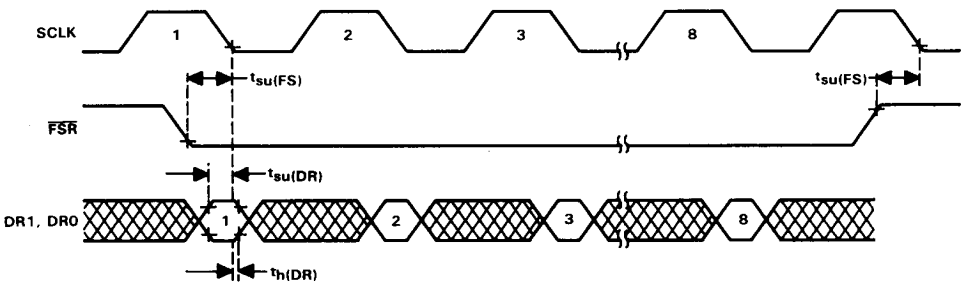
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

external framing: transmit timing



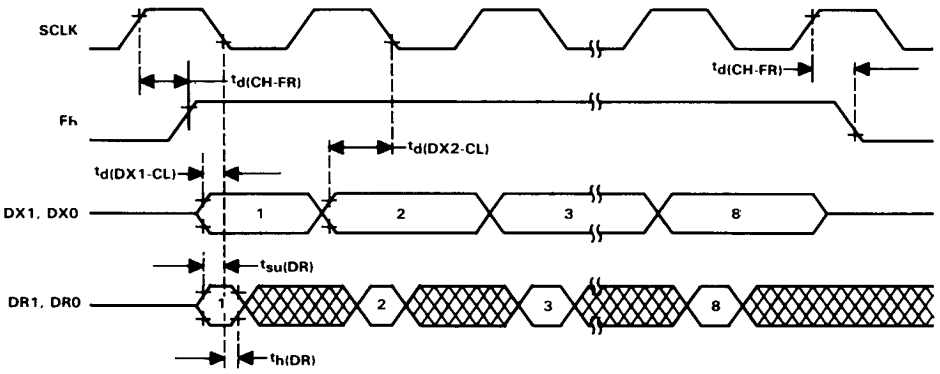
NOTES: G. Data valid on transmit outputs until SCLK rises.
H. The most significant bit is shifted first.

external framing: receive timing



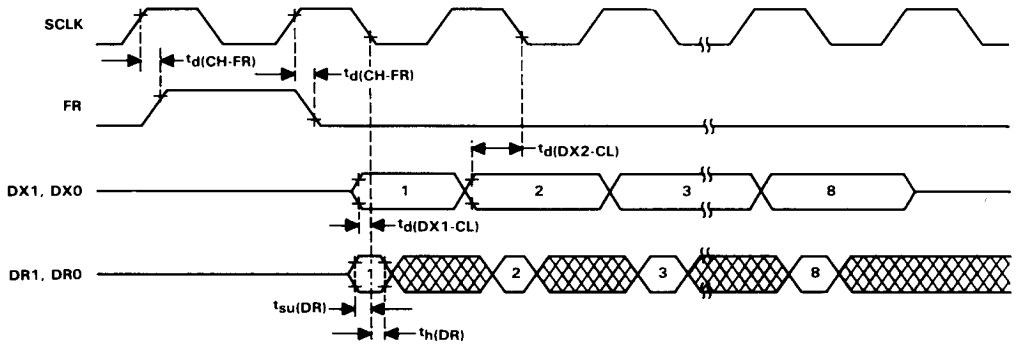
NOTE H: The most significant bit is shifted first.

internal framing: variable-data rate



NOTE H: The most significant bit is shifted first.

internal framing: fixed-data rate



NOTE H: The most significant bit is shifted first.

TEXAS INSTRUMENTS
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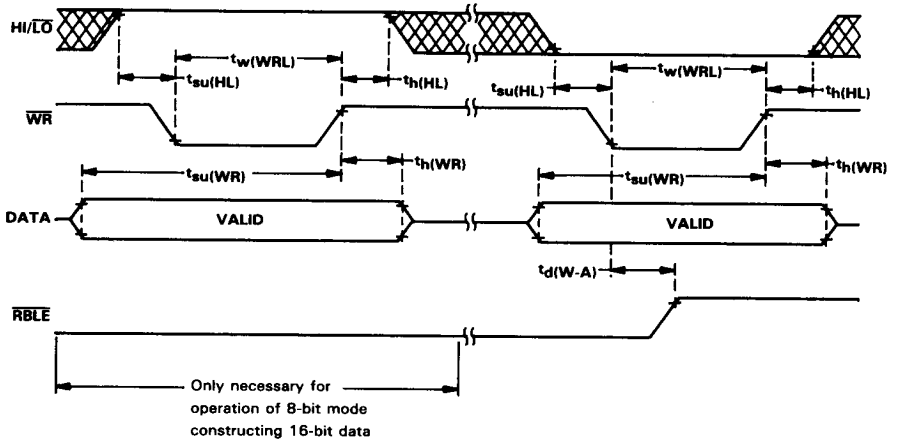
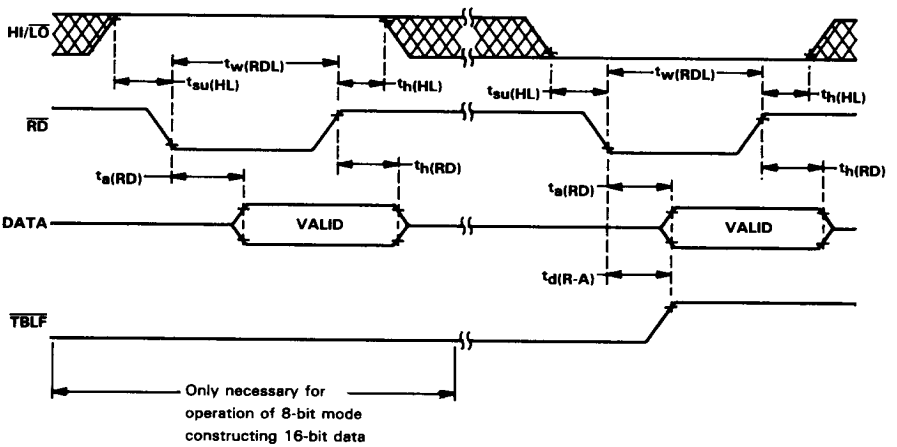
coprocessor timing: external write to coprocessor port



coprocessor timing: external read from coprocessor port



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TEXAS INSTRUMENTS
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EPROM PROGRAMMING

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{PP} (see Note 1) . . . . . −0.6 V to 14 V

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1. All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{PP} Supply voltage (see Note 2)		12.5	12.75	V

NOTE 2: V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.25 V).

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{PP1}	V_{PP} supply current	$V_{PP} = V_{CC} = 5.5$ V			100	μA
I_{PP2}	V_{PP} supply current (during program pulse)	$V_{PP} = 12.5$ V		30	50	mA

†All typical values except for I_{CC} are at $V_{CC} = 5$ V, $T_A = 25°C$.

recommended timing requirements for programming, $T_A = 25°C$, $V_{CC} = 6$ V, $V_{PP} = 12.5$ V (see Note 3)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	3.8		63	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130†	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150†	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	VCC setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

†Values derived from characterization data and not tested.

NOTES: 3. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and $V_{PP} = 12.5$ V ± 0.25 V during programming.

4. Common test conditions apply for $t_{dis(G)}$ except during programming.

PROGRAMMING THE TMS320E15/E17 EPROM CELL

Each TMS320E15/E17 device includes a 4K x 16-bit industry-standard EPROM cell for prototyping, early field testing, and low-volume production. In conjunction with this EPROM, the TMS320C15/C17 with a 4K-word masked ROM, then, provides more migration paths for cost-effective production.

EPROM adaptor sockets are available that provide pin-to-pin conversions for programming any TMS320E15/E17 device. One adaptor socket (part number RTC/PGM320A-06), shown in Figure 7, converts a 40-pin DIP device into an equivalent 28-pin device. Another socket (part number RTC/PGM320C-06), not shown, permits 44- to 28-pin conversion.

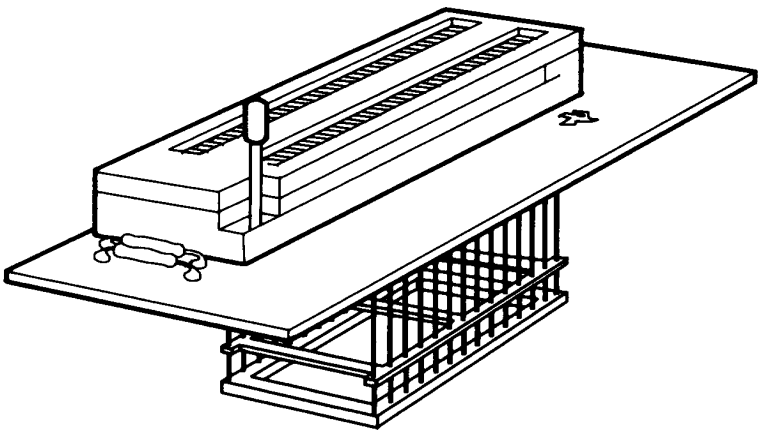


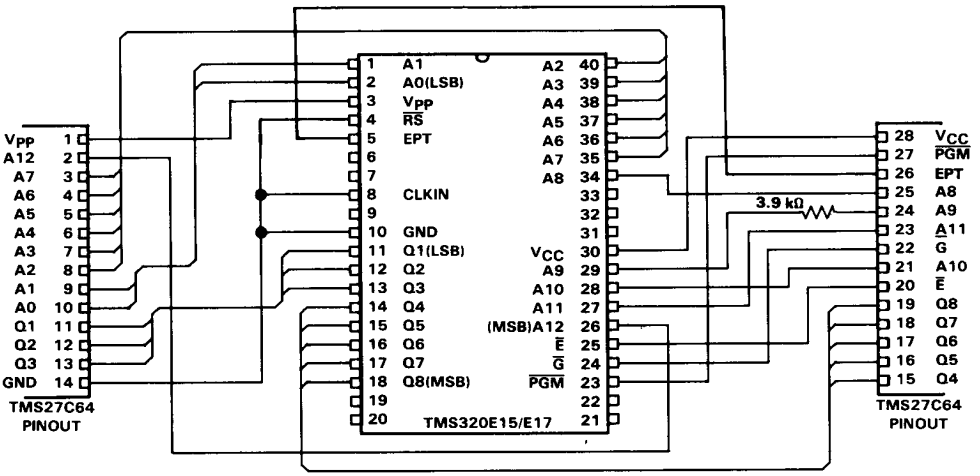
FIGURE 7. EPROM ADAPTOR SOCKET (40-pin to 28-pin DIP Conversion)

Key features of the EPROM cell include the normal programming operation as well as verification. The EPROM cell also includes a code protection feature that allows code to be protected against copyright violations.

The TMS320E15/E17 EPROM cell is programmed using the same family and device codes as the TMS27C64 8K x 8-bit EPROM. The TMS27C64 EPROM series are ultraviolet-light erasable, electrically programmable, read-only memories, fabricated using HVCMOS technology. They are pin-compatible with existing 28-pin ROMs and EPROMs. These EPROMs operate from a single 5-V supply in the read mode; however, a 12.5-V supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

Figure 8 shows the wiring conversion to program the TMS320E15/E17 using the 28-pin pinout of the TMS27C64. The table of pin nomenclature provides a description of the TMS27C64 pins. The code to be programmed into the device should be in serial mode. The TMS320E15/E17 uses 13 address lines to address the 4K-word memory in byte format.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001



CAUTION

Although acceptable by some EPROM programmers, the signature mode cannot be used on any TMS320E1x device. The signagure mode will input a high-level voltage (12.5 Vdc) onto pin A9. Since this pin is not designed for high voltage, the cell will be damaged. To prevent an accidental application of voltage, Texas Instruments has inserted a 3.9 kΩ resistor between pin A9 of the TI programmer socket and the programmer itself.

PIN NOMENCLATURE (TMS320E15/TMS320E17)

NAME	I/O	DEFINITION
A0-A12	I	On-chip EPROM programming address lines
CLKIN	I	Clock oscillator input
$\overline{E}$	I	EPROM chip select
EPT	I	EPROM test mode select
$\overline{G}$	I	EPROM read/verify select
GND	I	Ground
$\overline{PGM}$	I	EPROM write/program select
Q1-Q8	I/O	Data lines for byte-wide programming of on-chip 8K bytes of EPROM
$\overline{RS}$	I	Reset for initializing the device
V_{CC}	I	5-V power supply
V_{PP}	I	12.5-V power supply

FIGURE 8. TMS320E15/E17 EPROM PROGRAMMING CONVERSION TO TMS27C64 EPROM PINOUT

Table 8 shows the programming levels required for programming, verifying, reading, and protecting the EPROM cell.

TABLE 8. TMS320E15/E17 PROGRAMMING MODE LEVELS

SIGNAL NAME	TMS320E15 PIN	TMS27C64 PIN	PROGRAM	VERIFY	READ	PROTECT VERIFY	EPROM PROTECT
$\overline{E}$	25	20	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$	24	22	V_{IH}	$\overline{PULSE}$	$\overline{PULSE}$	V_{IL}	V_{IH}
$\overline{PGM}$	23	27	$\overline{PULSE}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}
V_{PP}	3	1	V_{PP}	V_{PP}	V_{CC}	V_{CC} + 1	V_{PP}
V_{CC}	30	28	V_{CC}	V_{CC}	V_{CC}	V_{CC} + 1	V_{CC} + 1
V_{SS}	10	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
CLKIN	8	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
$\overline{RS}$	4	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
EPT	5	26	V_{SS}	V_{SS}	V_{SS}	V_{PP}	V_{PP}
Q1-Q8	11-18	11-13, 15-19	D_{IN}	Q_{OUT}	Q_{OUT}	Q8 = RBIT	Q8 = $\overline{PULSE}$
A0-A3	2,1,40,39	10-7	ADDR	ADDR	ADDR	X	X
A4	38	6	ADDR	ADDR	ADDR	X	V_{IH}
A5	37	5	ADDR	ADDR	ADDR	X	X
A6	36	4	ADDR	ADDR	ADDR	V_{IL}	X
A7-A9	35,34,29	3,25,24	ADDR	ADDR	ADDR	X	X
A10-A12	28-26	21,23,2	ADDR	ADDR	ADDR	X	X

LEGEND:
V_{IH} = TTL high level; V_{IL} = TTL low level; ADDR = byte address bit
V_{PP} = 12.5 V ± 0.25 V; V_{CC} = 5 V ± 0.25 V; X = don't care
$\overline{PULSE}$ = low-going TTL level pulse; D_{IN} = byte to be programmed at ADDR
Q_{OUT} = byte stored at ADDR; RBIT = ROM protect bit.

programming

Since every memory bit in the cell is a logic 1, the programming operation reprograms certain bits to 0. Once programmed, these bits can only be erased using ultraviolet light. The correct byte is placed on the data bus with Vpp set to the 12.5-V level. The $\overline{PGM}$ pin is then pulsed low to program in the zeroes.

erasure

Before programming, the device must be erased by exposing it to ultraviolet light. The recommended minimum exposure dose (UV-intensity X exposure-time) is 15 watt-seconds per square centimeter. A typical 12 milliwatt-seconds per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After exposure, all bits are in the high state.

verify/read

To verify correct programming, the EPROM cell can be read using either the verify or read line definitions shown in Table 8, assuming the inhibit bit has not been programmed.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

read

The EPROM contents may be read independent of the programming cycle, provided the RBIT (ROM protect bit) has not been programmed. The read is accomplished by setting $\overline{E}$ to zero and pulsing $\overline{G}$ low. The contents of the EPROM location selected by the value on the address inputs appear on Q8-Q1.

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POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

output disable

During the EPROM programming process, the EPROM data outputs may be disabled, if desired, by establishing the output disable state. This state is selected by setting $\overline{G}$ and $\overline{E}$ pins high. While output disable is selected, Q8-Q1 are placed in the high-impedance state.

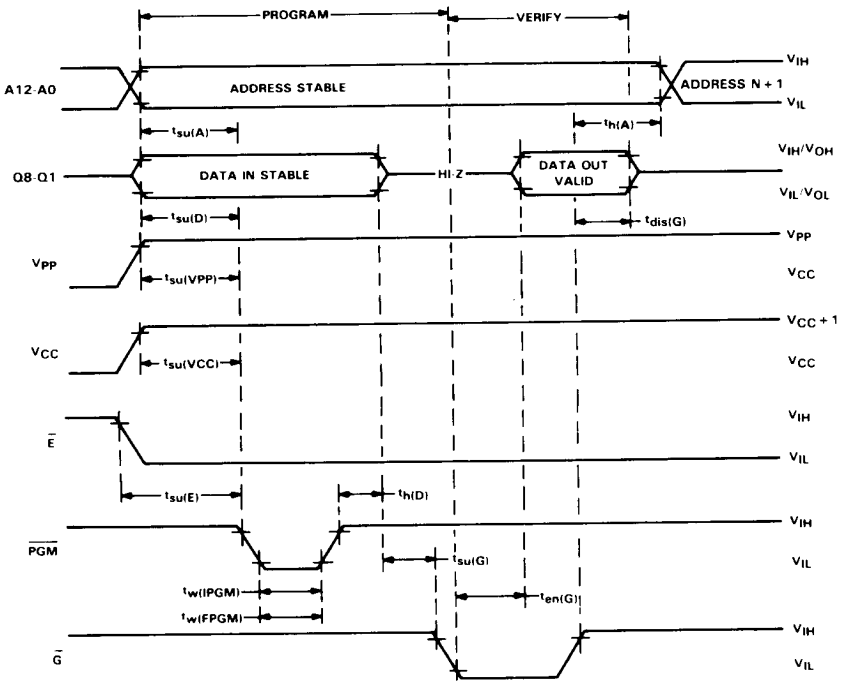
EPROM protection

To protect the proprietary algorithms existing in the code programmed on-chip, the ability to read or verify code from external accesses can be completely disabled. Programming the RBIT disables external access of the EPROM cell, making it impossible to access the code resident in the EPROM cell. The only way to remove this protection is to erase the entire EPROM cell, thus removing the proprietary information. The signal requirements for programming this bit are shown in Table 8. The cell can be determined as protected by verifying the programming of the RBIT shown in the table.

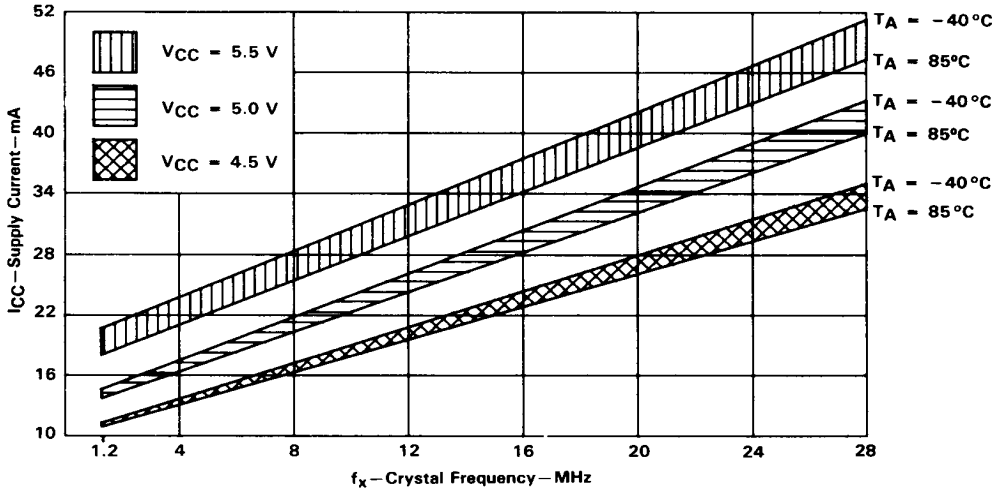
standard programming procedure

Before programming, the device must first be completely erased. Then the device can be programmed with the correct code. It is advisable to program unused sections with zeroes as a further security measure. After the programming is complete, the code programmed into the cell should be verified. If the cell passes verification, the next step is to program the ROM protect bit (RBIT). Once the RBIT programming is verified, an opaque label should be placed over the window to protect the EPROM cell from inadvertent erasure by ambient light. At this point, the programming is complete, and the device is ready to be placed into its destination circuit.

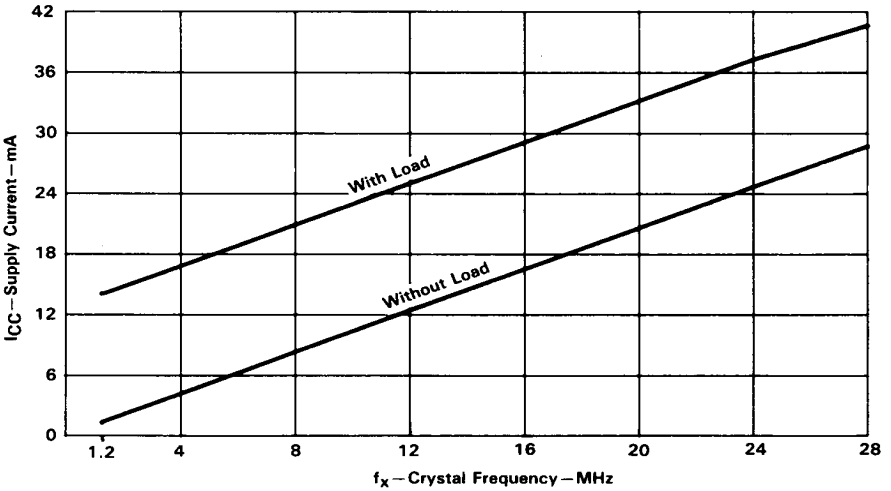
program cycle timing



TYPICAL POWER VS. FREQUENCY GRAPHS



(a) – 40°C TO 85°C TEMPERATURE RANGE



(b) VOLTAGE = 5 V; TEMPERATURE = 25°C

FIGURE 9. TYPICAL CMOS I_{CC} VS. FREQUENCY

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POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PACKAGE TYPES

PACKAGE TYPE	SUFFIX	FAMILY MEMBERS
40-pin plastic DIP (100-mil pin spacing)	N	NMOS: TMS32010 CMOS: TMS320C10, TMS320C10-14, TMS320C10-25, TMS320C15, TMS320C15-25, TMS320C17
40-pin windowed ceramic DIP (100-mil pin spacing)	JD	CMOS: TMS320E15, TMS320E15-25, TMS320E17
44-lead PLCC (50-mil pin spacing)	FN	CMOS: TMS320C10, TMS320C10-25, TMS320C15, TMS320C15-25, TMS320C17
44-lead windowed CER-QUAD (50-mil pin spacing)	FZ	CMOS: TMS320E15, TMS320E15-25, TMS320E17

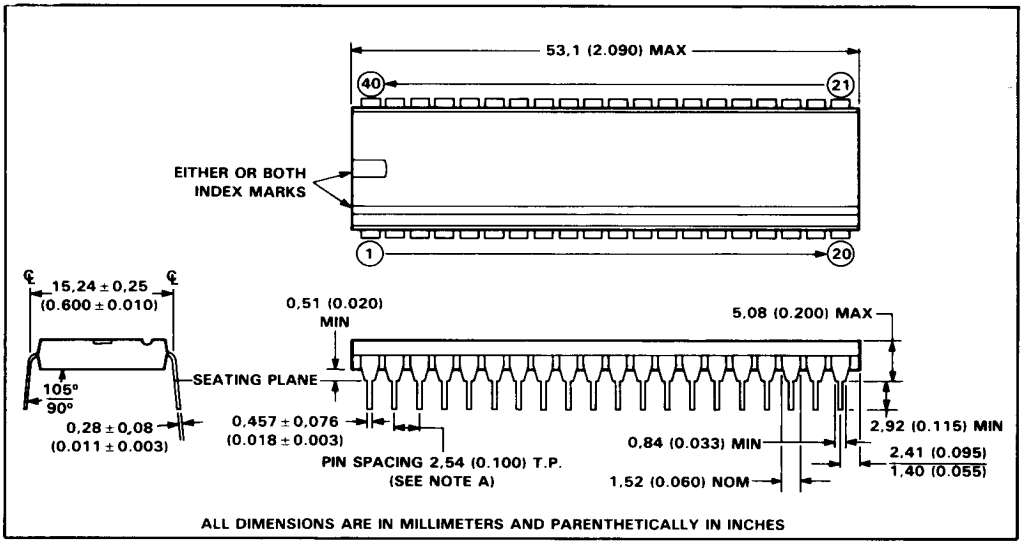
THERMAL DATA

thermal resistance characteristics

PACKAGE	$R_{\theta JA}$ °C/W)	$R_{\theta JC}$ (°C/W)
40-pin plastic dual-in-line package (NMOS)	51.6	16.6
40-pin plastic dual-in-line package (CMOS)	84	26
40-pin windowed ceramic dual-in-line package (CMOS)	40	8
44-lead plastic chip carrier package (CMOS)	60	17
44-lead CER-QUAD chip carrier package (CMOS)	63.8	7.8

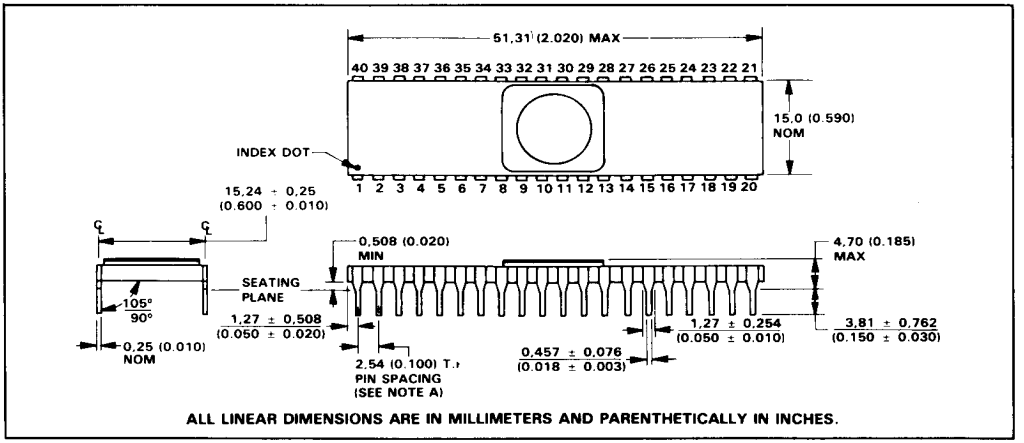
MECHANICAL DATA

40-pin plastic dual-in-line package



NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.

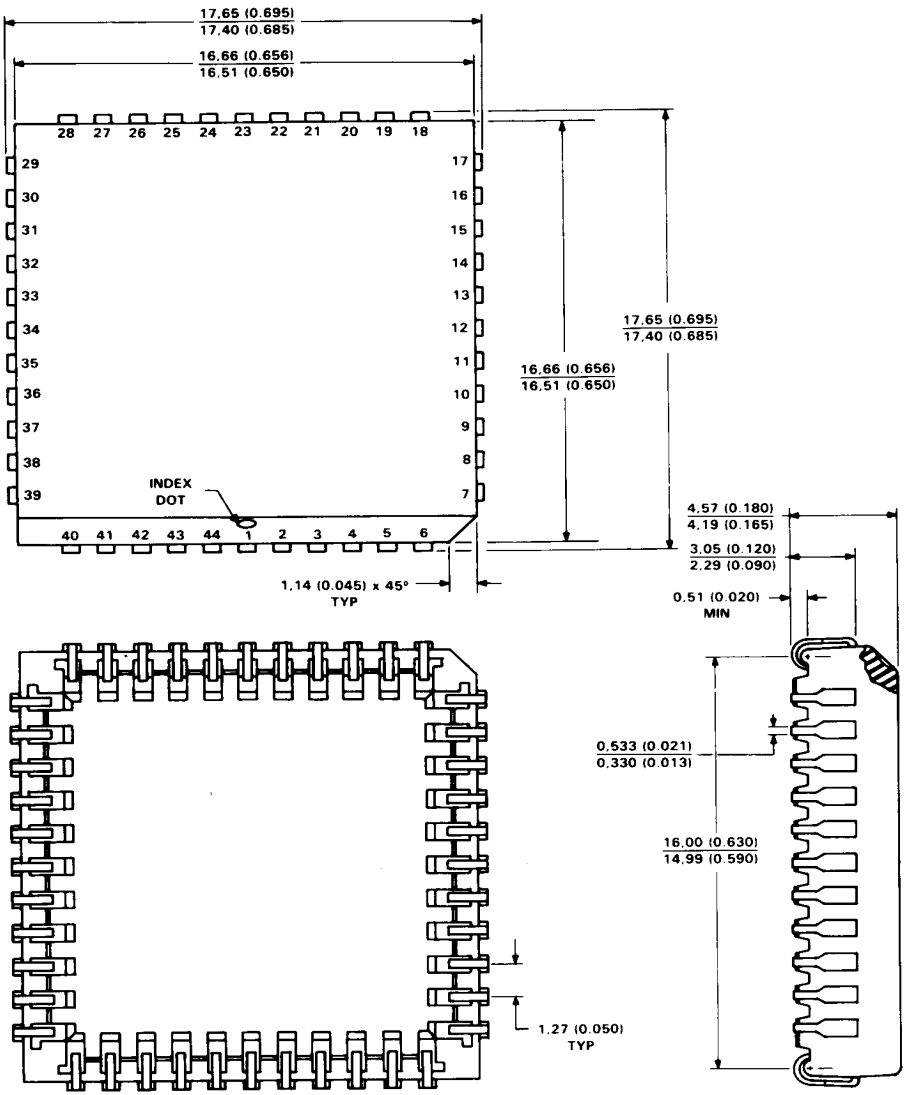
40-pin windowed ceramic dual-in-line package



NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.

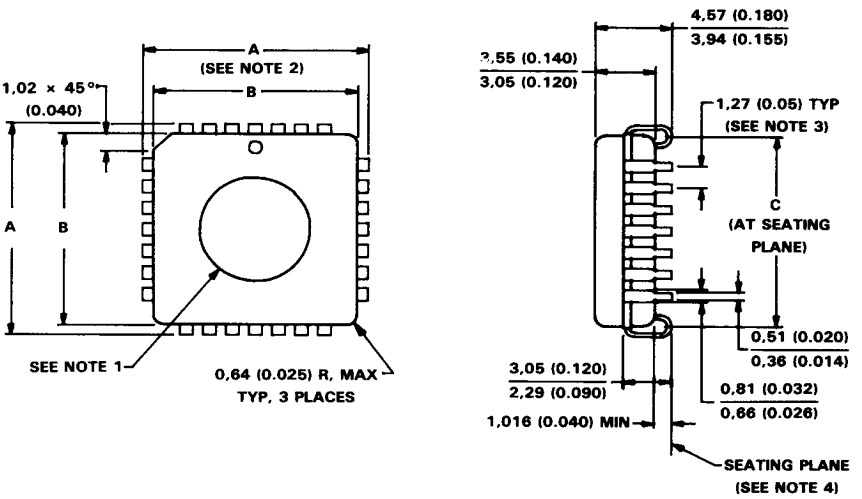
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

44-lead plastic chip package



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

44-lead FZ CER-QUAD chip carrier package



JEDEC OUTLINE	NO. OF TERMINALS	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO-087AA	28	12,32 (0.485)	12,57 (0.495)	10,92 (0.430)	11,56 (0.455)	10,41 (0.410)	10,92 (0.430)
MO-087AB	44	17,40 (0.685)	17,65 (0.695)	16,00 (0.630)	16,64 (0.655)	15,49 (0.610)	16,00 (0.630)
— —	68	25,02 (0.985)	25,27 (0.995)	23,62 (0.930)	24,26 (0.955)	23,11 (0.910)	23,62 (0.930)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: 1. Glass is optional, and the diameter is dependent on device application.
2. Centerline of center pin, each side, is within 0,10 (0.004) of package centerline as determined by dimension B.
3. Location of each pin is within 0,127 (0.005) of its true position with respect to center pin on each side.
4. The lead contact points are planar and within 0,15 (0.006).

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

INDEX