

RQJ0303PGDQA

Silicon P Channel MOS FET
Power Switching

REJ03G1272-0400

Rev.4.00

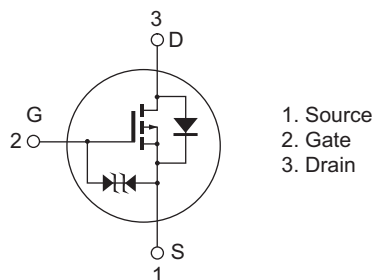
May 26, 2006

Features

- Low on-resistance
 $R_{DS(on)} = 54 \text{ m}\Omega$ typ ($V_{GS} = -10 \text{ V}$, $I_D = -1.6 \text{ A}$)
- Low drive current
- High speed switching
- 4.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



Note: Marking is "PG".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	+10 / -20	V
Drain current	I_D	-3.3	A
Drain peak current	$I_{D(Pulse)}$ ^{Note1}	-5	A
Body - drain diode reverse drain current	I_{DR}	-3.3	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4: $40 \times 40 \times 1 \text{ mm}$)

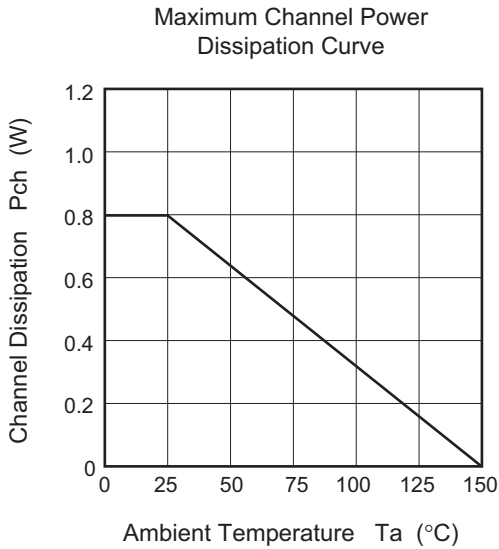
Electrical Characteristics

(Ta = 25°C)

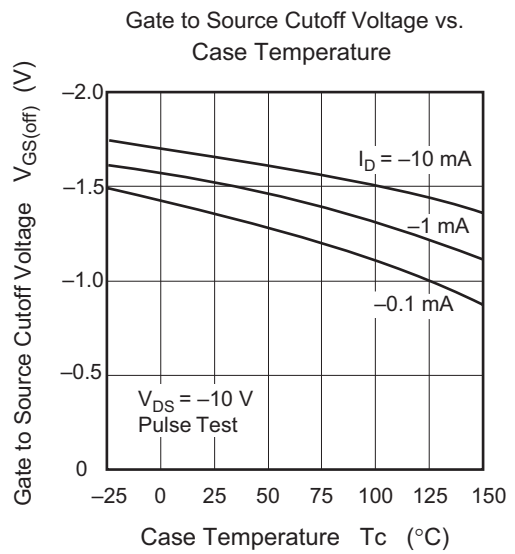
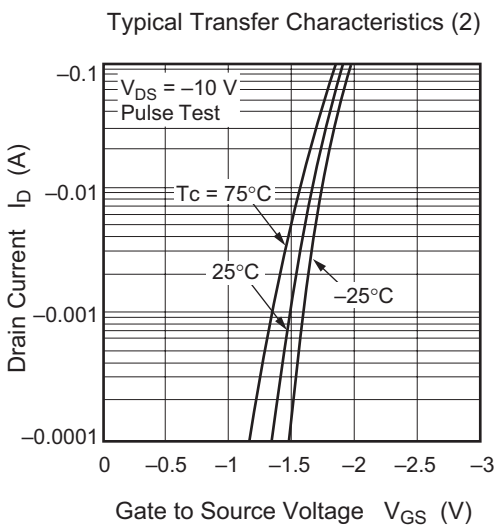
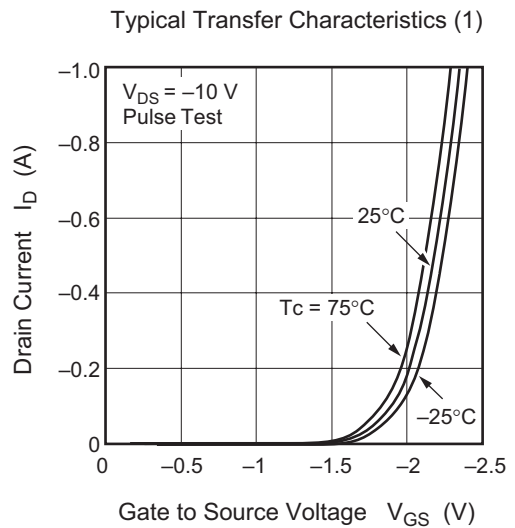
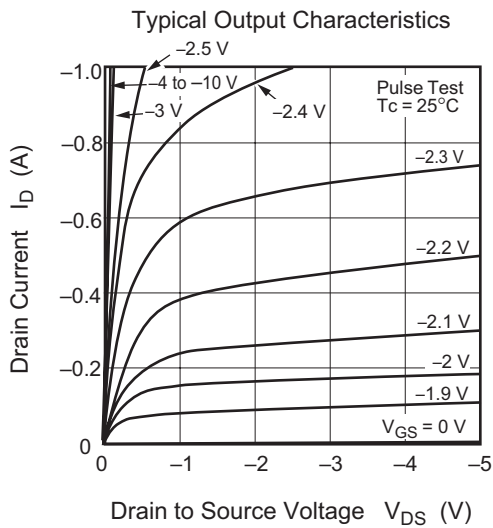
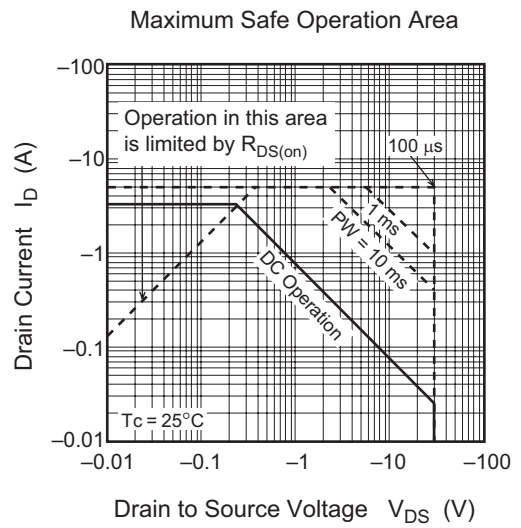
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+10	—	—	V	$I_G = +100 \mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-20	—	—	V	$I_G = -100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +8 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -16 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	54	68	$\text{m}\Omega$	$I_D = -1.6 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	76	107	$\text{m}\Omega$	$I_D = -1.6 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	2.5	4.2	—	S	$I_D = -1.6 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	625	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	111	—	pF	
Reverse transfer capacitance	C_{rss}	—	83	—	pF	
Turn - on delay time	$t_{d(on)}$	—	18	—	ns	$I_D = -1 \text{ A}$, $V_{GS} = -10 \text{ V}$, $R_L = 6.6 \Omega$, $R_g = 4.7 \Omega$
Rise time	t_r	—	29	—	ns	
Turn - off delay time	$t_{d(off)}$	—	47	—	ns	
Fall time	t_f	—	5.7	—	ns	
Total gate charge	Q_g	—	12	—	nC	$V_{DD} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -3.3 \text{ A}$
Gate to source charge	Q_{gs}	—	1.5	—	nC	
Gate to drain charge	Q_{gd}	—	2.9	—	nC	
Body - drain diode forward voltage	V_{DF}	—	-0.9	—	V	$I_F = -1.5 \text{ A}$, $V_{GS} = 0$ ^{Note3}

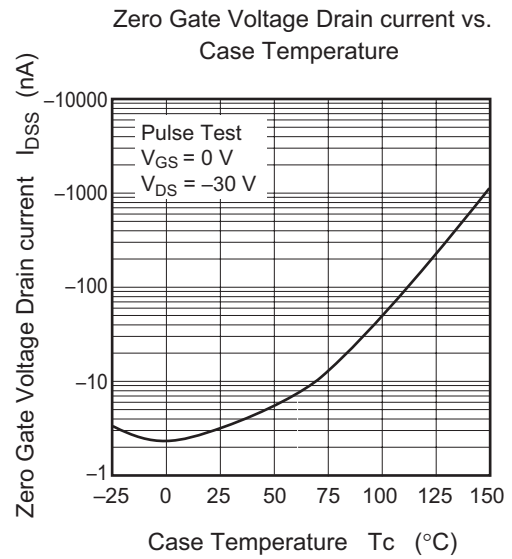
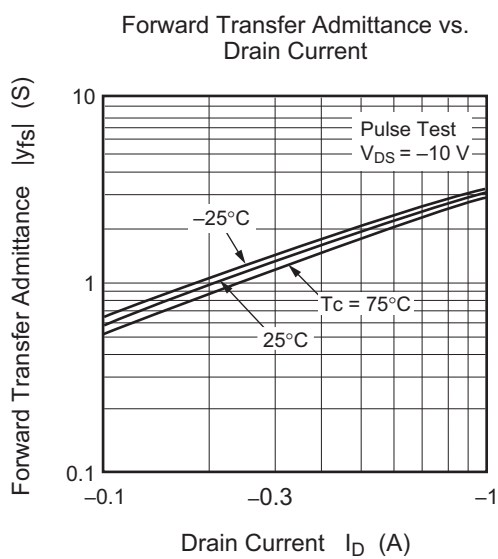
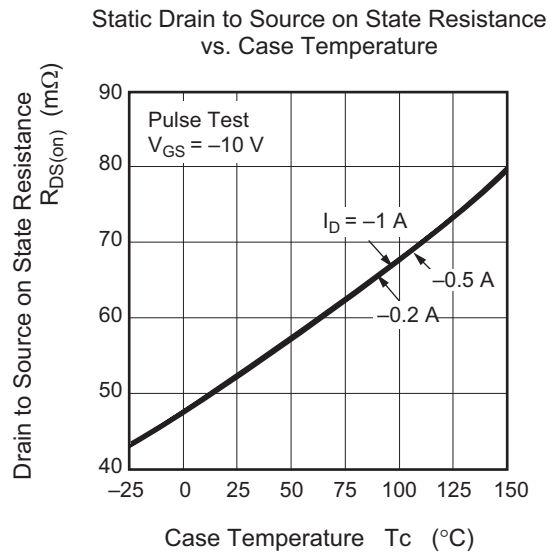
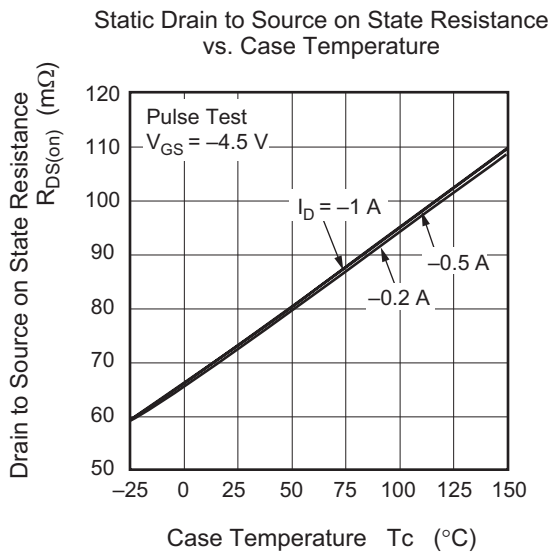
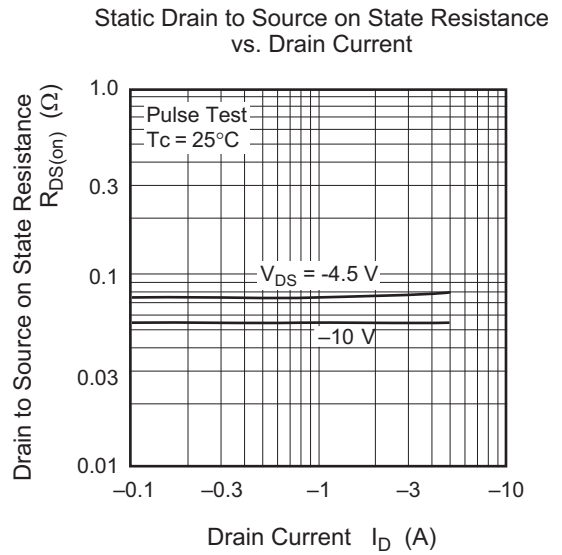
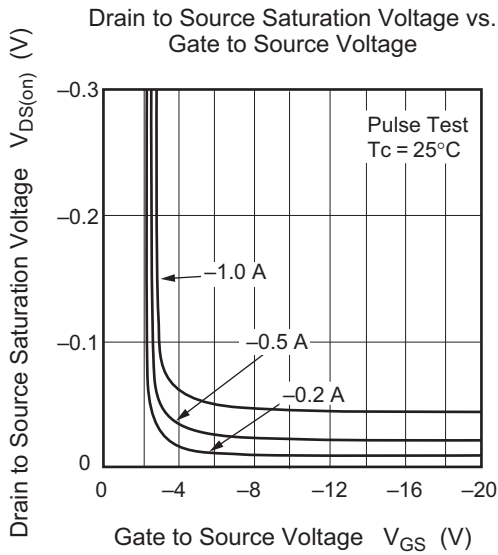
Notes: 3. Pulse test

Main Characteristics

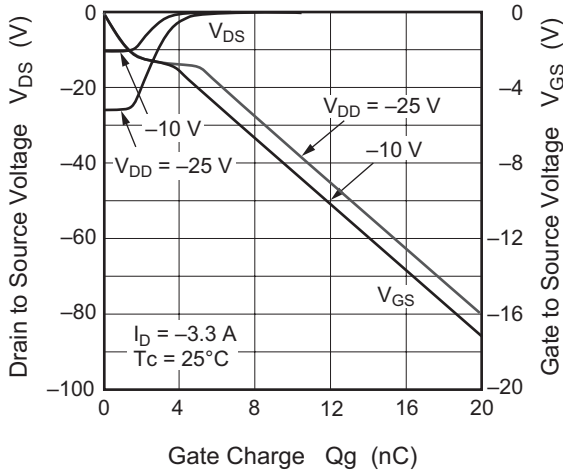


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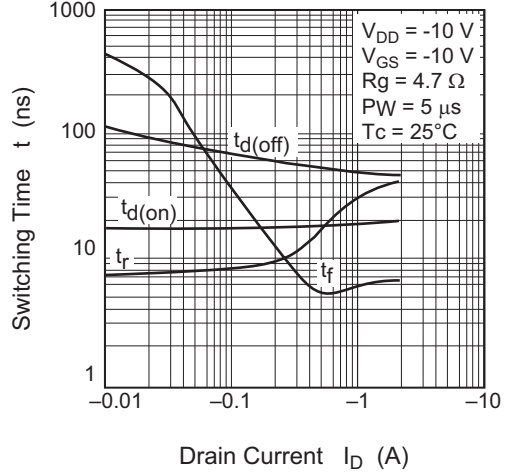




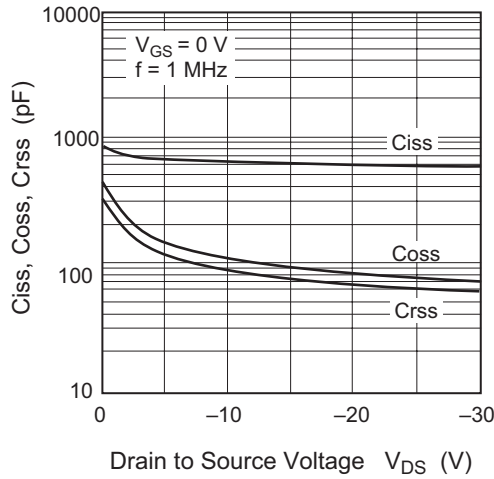
Dynamic Input Characteristics



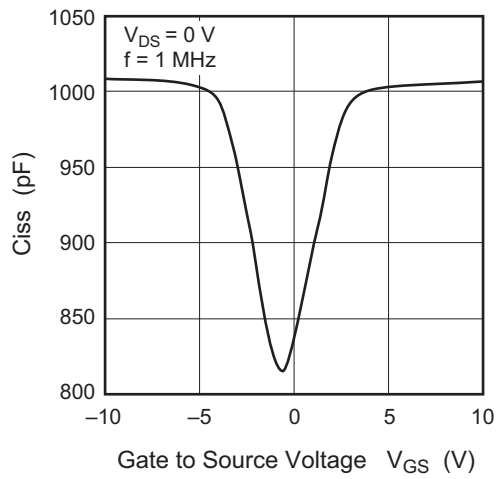
Switching Characteristics



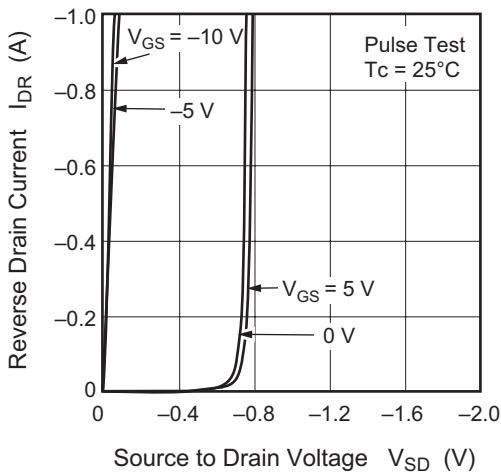
Typical Capacitance vs. Drain to Source Voltage



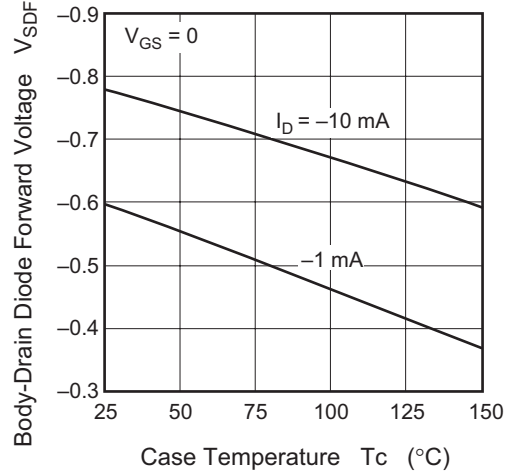
Input Capacitance vs. Gate to Source Voltage



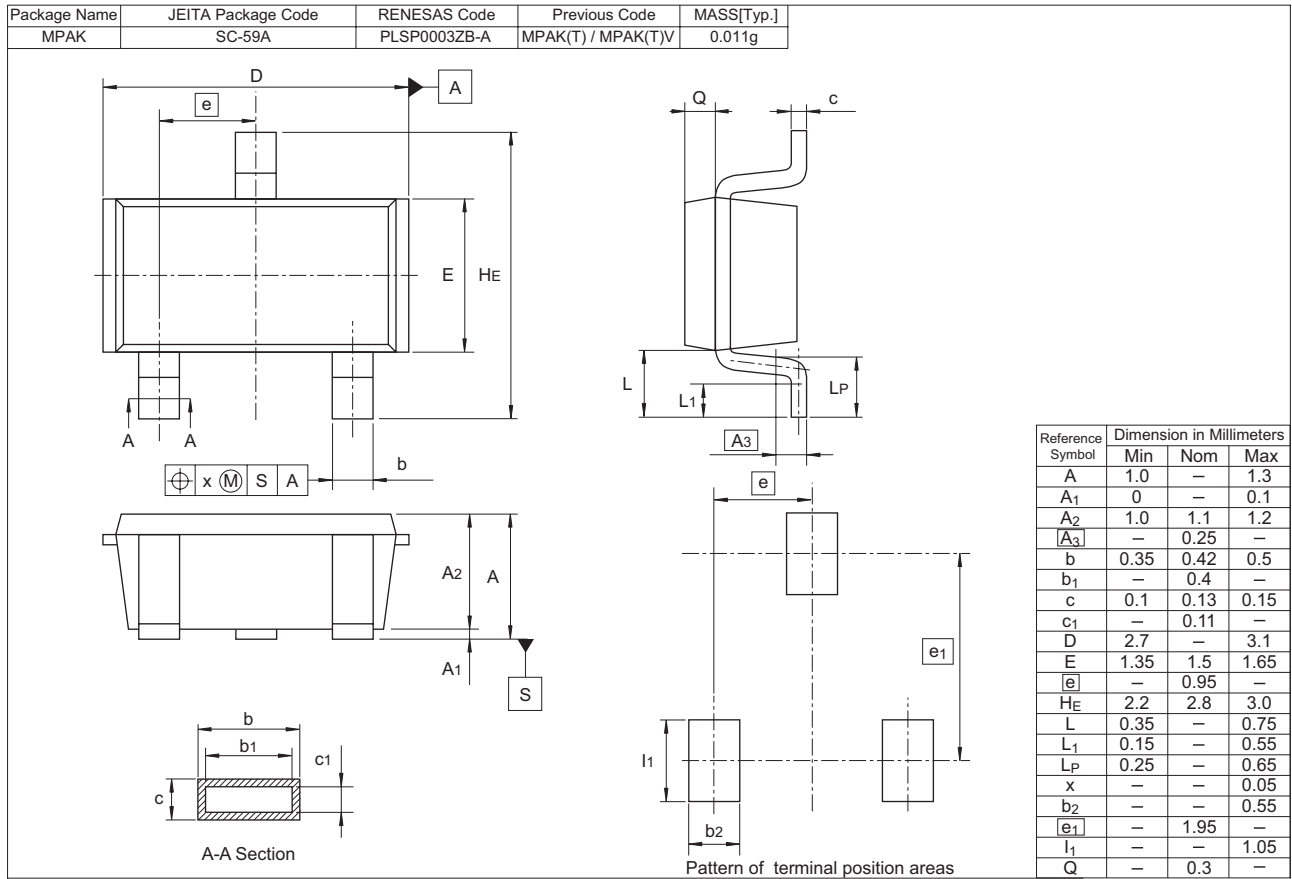
Reverse Drain Current vs. Source to Drain Voltage



Body-Drain Diode Forward Voltage vs. Case Temperature



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
RQJ0303PGDQATL-E	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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