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# R1LV0416C-I Series

Wide Temperature Range Version  
4 M SRAM (256-kword  $\times$  16-bit)

REJ03C0105-0100Z

Rev. 1.00

Aug.05.2003

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## Description

The R1LV0416C-I is a 4-Mbit static RAM organized 256-kword  $\times$  16-bit. R1LV0416C-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The R1LV0416C-I Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 44-pin TSOP II.

## Features

- Single 2.5 V and 3.0 V supply: 2.2 V to 3.6 V
- Fast access time: 55/70 ns (max)
- Power dissipation:
  - Active: 5.0 mW/MHz (typ) ( $V_{cc} = 2.5$  V)  
: 6.0 mW/MHz (typ) ( $V_{cc} = 3.0$  V)
  - Standby: 1.25  $\mu$ W (typ) ( $V_{cc} = 2.5$  V)  
: 1.5  $\mu$ W (typ) ( $V_{cc} = 3.0$  V)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range:  $-40$  to  $+85^{\circ}\text{C}$

## R1LV0416C-I Series

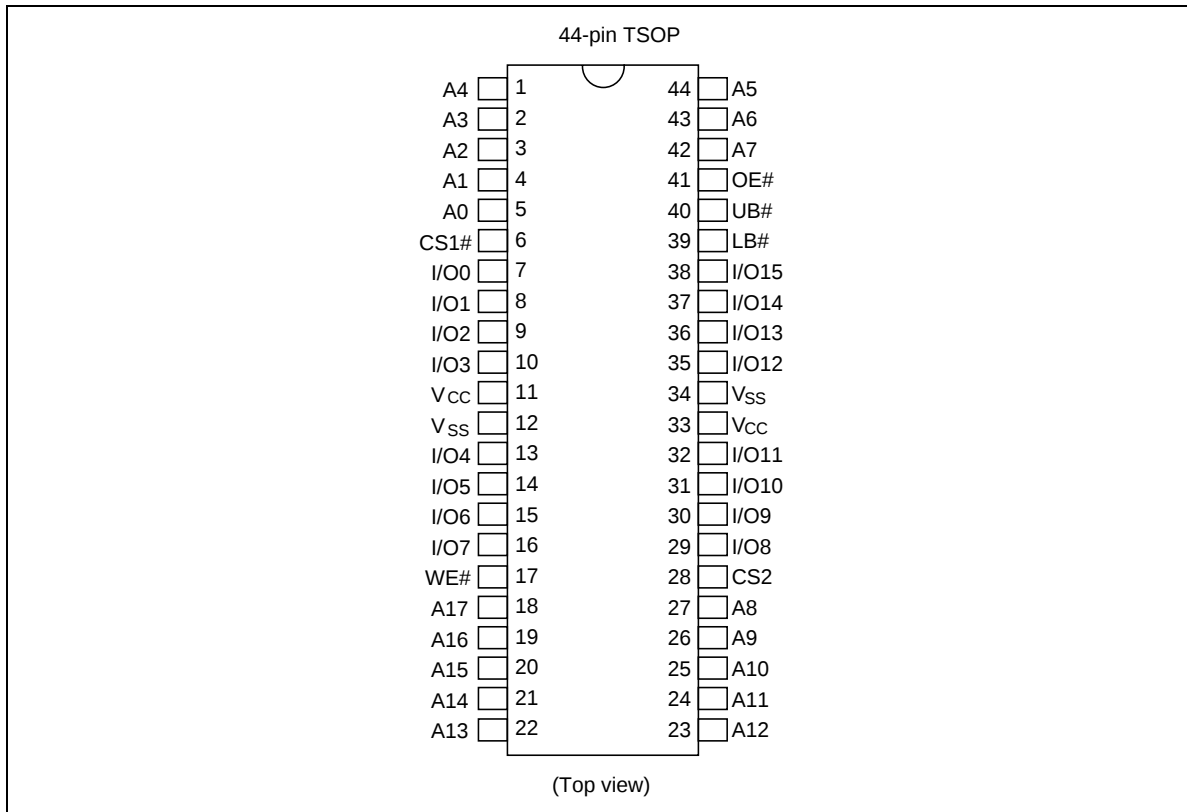
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### Ordering Information

| Type No.        | Access time | Package                                  |
|-----------------|-------------|------------------------------------------|
| R1LV0416CSB-5SI | 55 ns       | 400-mil 44-pin plastic TSOP II (44P3W-H) |
| R1LV0416CSB-7LI | 70 ns       |                                          |

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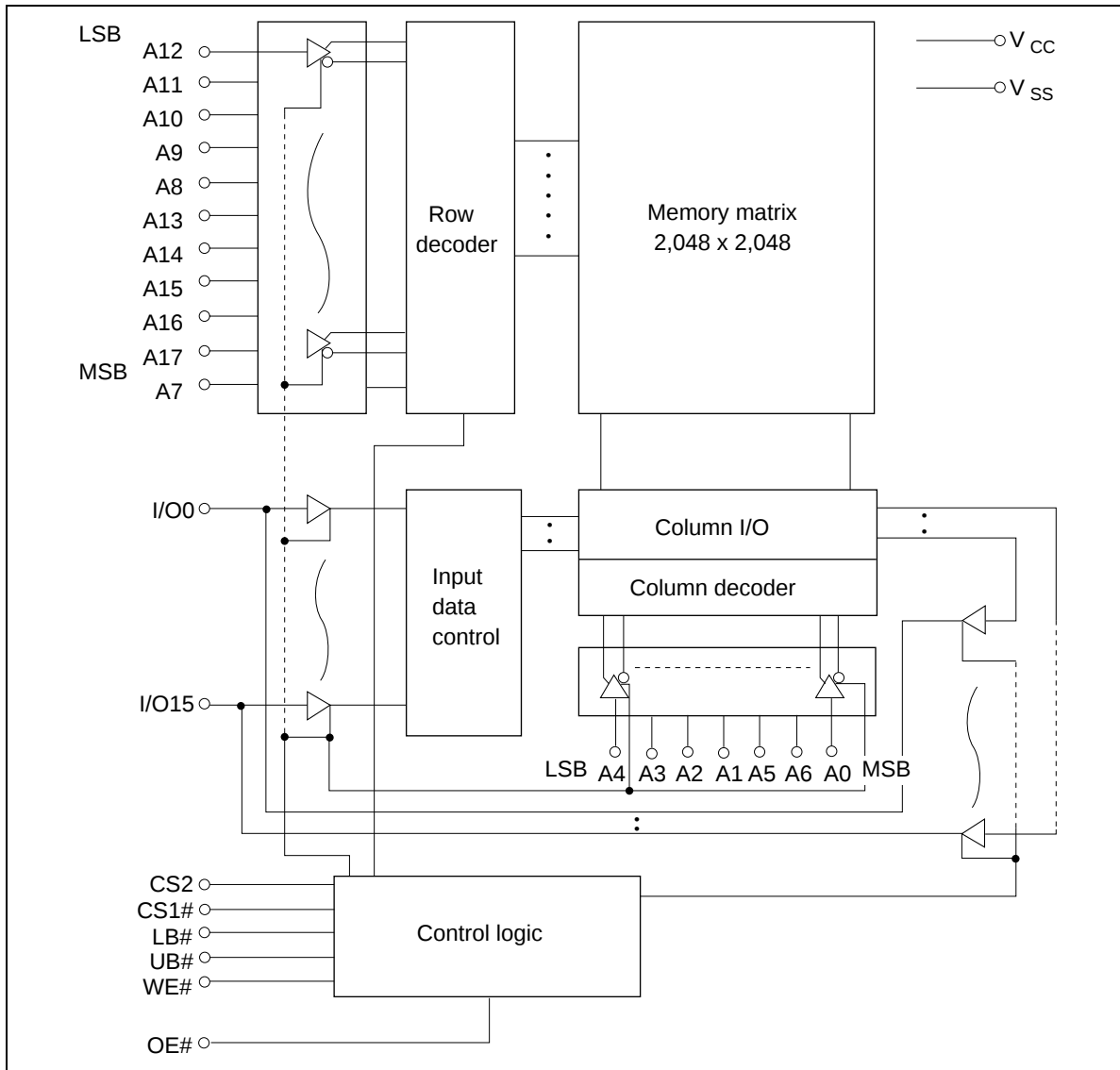
## Pin Arrangement



## Pin Description

| Pin name                         | Function          |
|----------------------------------|-------------------|
| A0 to A17                        | Address input     |
| I/O0 to I/O15                    | Data input/output |
| CS1# ( $\overline{\text{CS1}}$ ) | Chip select 1     |
| CS2                              | Chip select 2     |
| OE# ( $\overline{\text{OE}}$ )   | Output enable     |
| WE# ( $\overline{\text{WE}}$ )   | Write enable      |
| LB# ( $\overline{\text{LB}}$ )   | Lower byte select |
| UB# ( $\overline{\text{UB}}$ )   | Upper byte select |
| V <sub>CC</sub>                  | Power supply      |
| V <sub>SS</sub>                  | Ground            |

## Block Diagram



## R1LV0416C-I Series

### Operation Table

| CS1# | CS2 | WE# | OE# | UB# | LB# | I/O0 to I/O7 | I/O8 to I/O15 | Operation        |
|------|-----|-----|-----|-----|-----|--------------|---------------|------------------|
| H    | ×   | ×   | ×   | ×   | ×   | High-Z       | High-Z        | Standby          |
| ×    | L   | ×   | ×   | ×   | ×   | High-Z       | High-Z        | Standby          |
| ×    | ×   | ×   | ×   | H   | H   | High-Z       | High-Z        | Standby          |
| L    | H   | H   | L   | L   | L   | Dout         | Dout          | Read             |
| L    | H   | H   | L   | H   | L   | Dout         | High-Z        | Lower byte read  |
| L    | H   | H   | L   | L   | H   | High-Z       | Dout          | Upper byte read  |
| L    | H   | L   | ×   | L   | L   | Din          | Din           | Write            |
| L    | H   | L   | ×   | H   | L   | Din          | High-Z        | Lower byte write |
| L    | H   | L   | ×   | L   | H   | High-Z       | Din           | Upper byte write |
| L    | H   | H   | H   | ×   | ×   | High-Z       | High-Z        | Output disable   |

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

### Absolute Maximum Ratings

| Parameter                                        | Symbol     | Value                                              | Unit |
|--------------------------------------------------|------------|----------------------------------------------------|------|
| Power supply voltage relative to $V_{SS}$        | $V_{CC}$   | -0.5 to +4.6                                       | V    |
| Terminal voltage on any pin relative to $V_{SS}$ | $V_T$      | -0.5 <sup>*1</sup> to $V_{CC} + 0.3$ <sup>*2</sup> | V    |
| Power dissipation                                | $P_T$      | 0.7                                                | W    |
| Operating temperature                            | $T_{opr}$  | -40 to +85                                         | °C   |
| Storage temperature range                        | $T_{stg}$  | -65 to +150                                        | °C   |
| Storage temperature range under bias             | $T_{bias}$ | -40 to +85                                         | °C   |

Notes: 1.  $V_T$  min: -3.0 V for pulse half-width ≤ 30 ns.  
2. Maximum voltage is +7.0 V.

### DC Operating Conditions

( $T_a = -40$  to +85°C)

| Parameter          |                           | Symbol   | Min  | Typ     | Max            | Unit | Note |
|--------------------|---------------------------|----------|------|---------|----------------|------|------|
| Supply voltage     |                           | $V_{CC}$ | 2.2  | 2.5/3.0 | 3.6            | V    |      |
|                    |                           | $V_{SS}$ | 0    | 0       | 0              | V    |      |
| Input high voltage | $V_{CC} = 2.2$ V to 2.7 V | $V_{IH}$ | 2.0  | —       | $V_{CC} + 0.3$ | V    |      |
|                    | $V_{CC} = 2.7$ V to 3.6 V | $V_{IH}$ | 2.2  | —       | $V_{CC} + 0.3$ | V    |      |
| Input low voltage  | $V_{CC} = 2.2$ V to 2.7 V | $V_{IL}$ | -0.2 | —       | 0.4            | V    | 1    |
|                    | $V_{CC} = 2.7$ V to 3.6 V | $V_{IL}$ | -0.3 | —       | 0.6            | V    | 1    |

Note: 1.  $V_{IL}$  min: -3.0 V for pulse half-width ≤ 30 ns.

## DC Characteristics

| Parameter                 | Symbol                                      | Min       | Typ <sup>*1</sup> | Max               | Unit             | Test conditions                                                                                                                                                           |
|---------------------------|---------------------------------------------|-----------|-------------------|-------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Input leakage current     | $ I_{LI} $                                  | —         | —                 | 1                 | $\mu\text{A}$    | $V_{in} = V_{SS}$ to $V_{CC}$                                                                                                                                             |
| Output leakage current    | $ I_{LO} $                                  | —         | —                 | 1                 | $\mu\text{A}$    | CS1# = $V_{IH}$ or CS2 = $V_{IL}$ or<br>OE# = $V_{IH}$ or WE# = $V_{IL}$ or<br>LB# = UB# = $V_{IH}$ ,<br>$V_{I/O} = V_{SS}$ to $V_{CC}$                                   |
| Operating current         | $I_{CC}$                                    | —         | 5                 | 20                | mA               | CS1# = $V_{IL}$ , CS2 = $V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0$ mA                                                                                         |
| Average operating current | $I_{CC1}$                                   | —         | 8                 | 25                | mA               | Min. cycle, duty = 100%,<br>$I_{I/O} = 0$ mA, CS1# = $V_{IL}$ ,<br>CS2 = $V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$                                                           |
|                           | $I_{CC2}$                                   | —         | 2                 | 5                 | mA               | Cycle time = 1 $\mu\text{s}$ ,<br>duty = 100%,<br>$I_{I/O} = 0$ mA, CS1# $\leq 0.2$ V,<br>CS2 $\geq V_{CC} - 0.2$ V,<br>$V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V |
| Standby current           | $I_{SB}$                                    | —         | 0.1               | 0.3               | mA               | CS2 = $V_{IL}$                                                                                                                                                            |
| Standby current           | to +85°C                                    | $I_{SB1}$ | —                 | —                 | 20 <sup>*2</sup> | $\mu\text{A}$ Vin $\geq 0$ V                                                                                                                                              |
|                           |                                             |           | —                 | —                 | 10 <sup>*3</sup> | $\mu\text{A}$ (1) $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ or                                                                                                     |
|                           | to +70°C                                    | $I_{SB1}$ | —                 | —                 | 20 <sup>*2</sup> | $\mu\text{A}$ (2) CS1# $\geq V_{CC} - 0.2 \text{ V}$ ,                                                                                                                    |
|                           |                                             |           | —                 | —                 | 10 <sup>*3</sup> | $\mu\text{A}$ CS2 $\geq V_{CC} - 0.2 \text{ V}$ or                                                                                                                        |
|                           | to +40°C                                    | $I_{SB1}$ | —                 | 0.7 <sup>*2</sup> | 10 <sup>*2</sup> | $\mu\text{A}$ (3) LB# = UB# $\geq V_{CC} - 0.2 \text{ V}$ ,                                                                                                               |
|                           |                                             |           | —                 | 0.7 <sup>*3</sup> | 3 <sup>*3</sup>  | $\mu\text{A}$ CS2 $\geq V_{CC} - 0.2 \text{ V}$ ,                                                                                                                         |
|                           | -40°C to +25°C                              | $I_{SB1}$ | —                 | 0.5 <sup>*2</sup> | 10 <sup>*2</sup> | $\mu\text{A}$ CS1# $\leq 0.2 \text{ V}$                                                                                                                                   |
|                           |                                             |           | —                 | 0.5 <sup>*3</sup> | 3 <sup>*3</sup>  | $\mu\text{A}$                                                                                                                                                             |
| Output high voltage       | $V_{CC} = 2.2 \text{ V}$ to $2.7 \text{ V}$ | $V_{OH}$  | 2.0               | —                 | —                | V $I_{OH} = -0.5 \text{ mA}$                                                                                                                                              |
|                           | $V_{CC} = 2.7 \text{ V}$ to $3.6 \text{ V}$ | $V_{OH}$  | 2.4               | —                 | —                | V $I_{OH} = -1 \text{ mA}$                                                                                                                                                |
|                           | $V_{CC} = 2.2 \text{ V}$ to $3.6 \text{ V}$ | $V_{OH2}$ | $V_{CC} - 0.2$    | —                 | —                | V $I_{OH} = -100 \mu\text{A}$                                                                                                                                             |
| Output low voltage        | $V_{CC} = 2.2 \text{ V}$ to $2.7 \text{ V}$ | $V_{OL}$  | —                 | —                 | 0.4              | V $I_{OL} = 0.5 \text{ mA}$                                                                                                                                               |
|                           | $V_{CC} = 2.7 \text{ V}$ to $3.6 \text{ V}$ | $V_{OL}$  | —                 | —                 | 0.4              | V $I_{OL} = 2 \text{ mA}$                                                                                                                                                 |
|                           | $V_{CC} = 2.2 \text{ V}$ to $3.6 \text{ V}$ | $V_{OL2}$ | —                 | —                 | 0.2              | V $I_{OL} = 100 \mu\text{A}$                                                                                                                                              |

Notes: 1. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.

2. L version. (-7LI)

3. SL version. (-5SI)

## R1LV0416C-I Series

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### Capacitance

(Ta = +25°C, f = 1.0 MHz)

| Parameter                | Symbol           | Min | Typ | Max | Unit | Test conditions        | Note |
|--------------------------|------------------|-----|-----|-----|------|------------------------|------|
| Input capacitance        | C <sub>in</sub>  | —   | —   | 8   | pF   | V <sub>in</sub> = 0 V  | 1    |
| Input/output capacitance | C <sub>I/O</sub> | —   | —   | 10  | pF   | V <sub>I/O</sub> = 0 V | 1    |

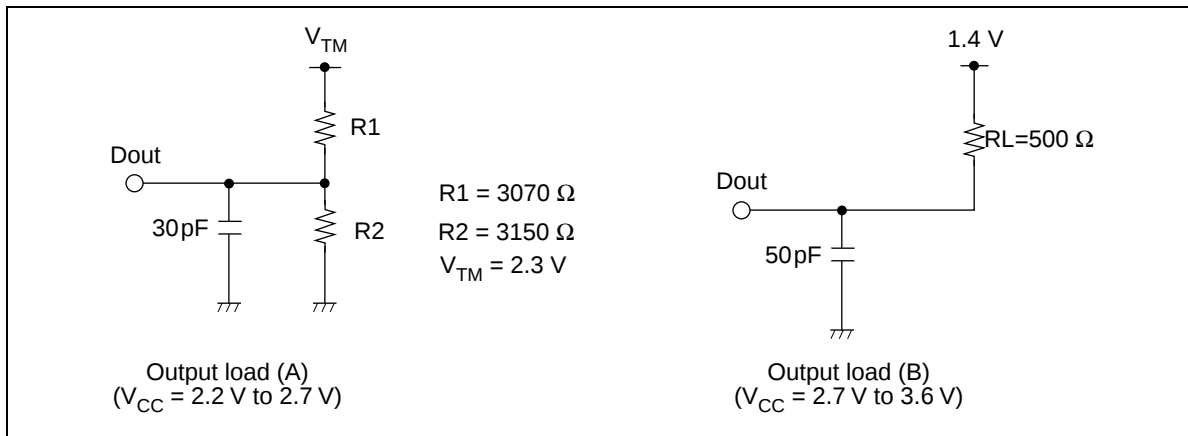
Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.2$  V to  $3.6$  V, unless otherwise noted.)

### Test Conditions

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.2$  V ( $V_{CC} = 2.2$  V to  $2.7$  V)  
:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.4$  V ( $V_{CC} = 2.7$  V to  $3.6$  V)
- Input rise and fall time: 5 ns
- Input/output timing reference levels: 1.1 V ( $V_{CC} = 2.2$  V to  $2.7$  V)  
: 1.4 V ( $V_{CC} = 2.7$  V to  $3.6$  V)
- Output load: See figures (Including scope and jig)



## R1LV0416C-I Series

### Read Cycle

|                                    |                   | R1LV0416C-I |     |     |     |      |       |
|------------------------------------|-------------------|-------------|-----|-----|-----|------|-------|
|                                    |                   | -5          |     | -7  |     |      |       |
| Parameter                          | Symbol            | Min         | Max | Min | Max | Unit | Notes |
| Read cycle time                    | t <sub>RC</sub>   | 55          | —   | 70  | —   | ns   |       |
| Address access time                | t <sub>AA</sub>   | —           | 55  | —   | 70  | ns   |       |
| Chip select access time            | t <sub>ASC1</sub> | —           | 55  | —   | 70  | ns   |       |
|                                    | t <sub>ASC2</sub> | —           | 55  | —   | 70  | ns   |       |
| Output enable to output valid      | t <sub>OE</sub>   | —           | 35  | —   | 40  | ns   |       |
| Output hold from address change    | t <sub>OH</sub>   | 10          | —   | 10  | —   | ns   |       |
| LB#, UB# access time               | t <sub>BA</sub>   | —           | 55  | —   | 70  | ns   |       |
| Chip select to output in low-Z     | t <sub>CLZ1</sub> | 10          | —   | 10  | —   | ns   |       |
|                                    | t <sub>CLZ2</sub> | 10          | —   | 10  | —   | ns   |       |
| LB#, UB# disable to low-Z          | t <sub>BLZ</sub>  | 5           | —   | 5   | —   | ns   |       |
| Output enable to output in low-Z   | t <sub>OLZ</sub>  | 5           | —   | 5   | —   | ns   | 2     |
| Chip deselect to output in high-Z  | t <sub>CHZ1</sub> | 0           | 20  | 0   | 25  | ns   |       |
|                                    | t <sub>CHZ2</sub> | 0           | 20  | 0   | 25  | ns   |       |
| LB#, UB# disable to high-Z         | t <sub>BHZ</sub>  | 0           | 20  | 0   | 25  | ns   |       |
| Output disable to output in high-Z | t <sub>OHZ</sub>  | 0           | 20  | 0   | 25  | ns   | 1, 2  |

## R1LV0416C-I Series

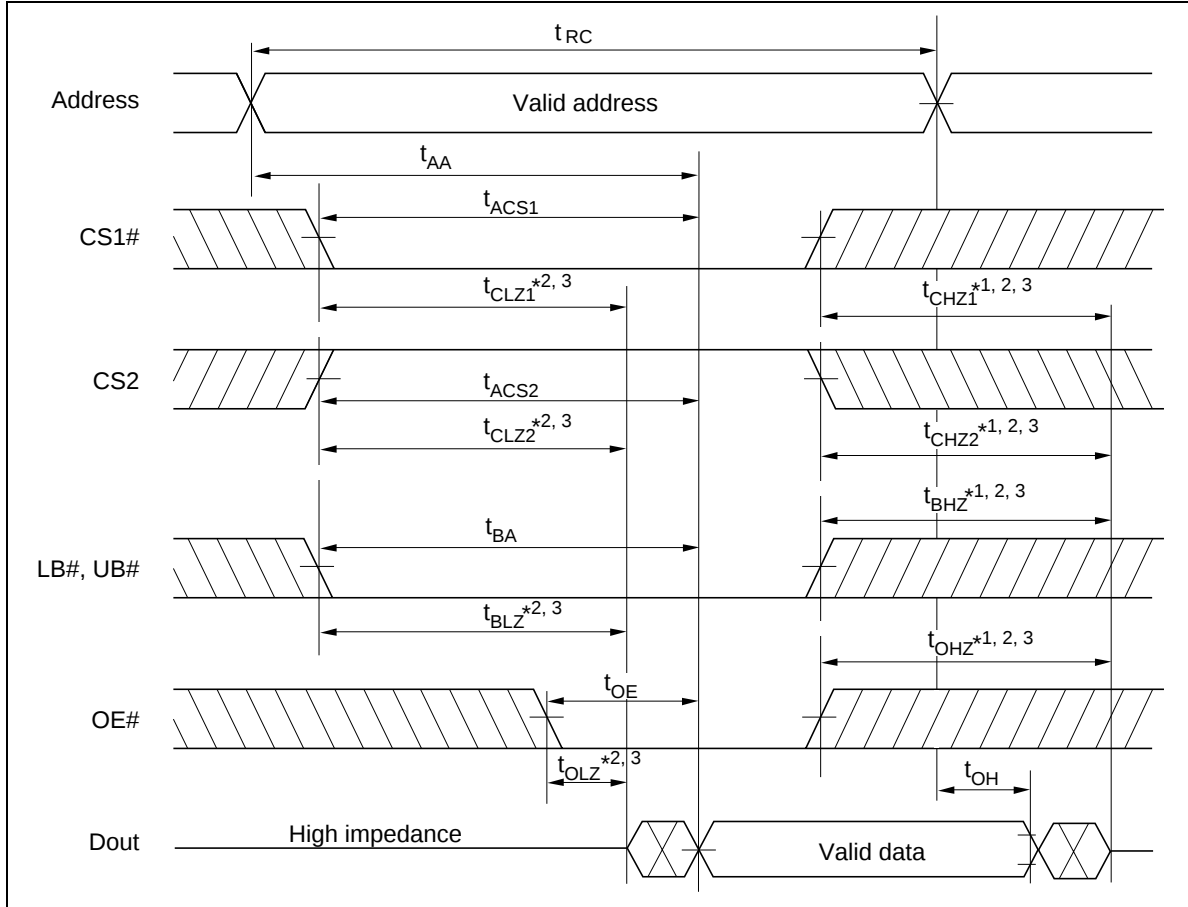
### Write Cycle

|                                    |                  | R1LV0416C-I |     |     |     |      |       |
|------------------------------------|------------------|-------------|-----|-----|-----|------|-------|
|                                    |                  | -5          |     | -7  |     |      |       |
| Parameter                          | Symbol           | Min         | Max | Min | Max | Unit | Notes |
| Write cycle time                   | t <sub>WC</sub>  | 55          | —   | 70  | —   | ns   |       |
| Address valid to end of write      | t <sub>AW</sub>  | 50          | —   | 60  | —   | ns   |       |
| Chip selection to end of write     | t <sub>CW</sub>  | 50          | —   | 60  | —   | ns   | 5     |
| Write pulse width                  | t <sub>WP</sub>  | 40          | —   | 50  | —   | ns   | 4     |
| LB#, UB# valid to end of write     | t <sub>BW</sub>  | 50          | —   | 55  | —   | ns   |       |
| Address setup time                 | t <sub>AS</sub>  | 0           | —   | 0   | —   | ns   | 6     |
| Write recovery time                | t <sub>WR</sub>  | 0           | —   | 0   | —   | ns   | 7     |
| Data to write time overlap         | t <sub>DW</sub>  | 25          | —   | 30  | —   | ns   |       |
| Data hold from write time          | t <sub>DH</sub>  | 0           | —   | 0   | —   | ns   |       |
| Output active from end of write    | t <sub>OW</sub>  | 5           | —   | 5   | —   | ns   | 2     |
| Output disable to output in high-Z | t <sub>OHZ</sub> | 0           | 20  | 0   | 25  | ns   | 1, 2  |
| Write to output in high-Z          | t <sub>WHZ</sub> | 0           | 20  | 0   | 25  | ns   | 1, 2  |

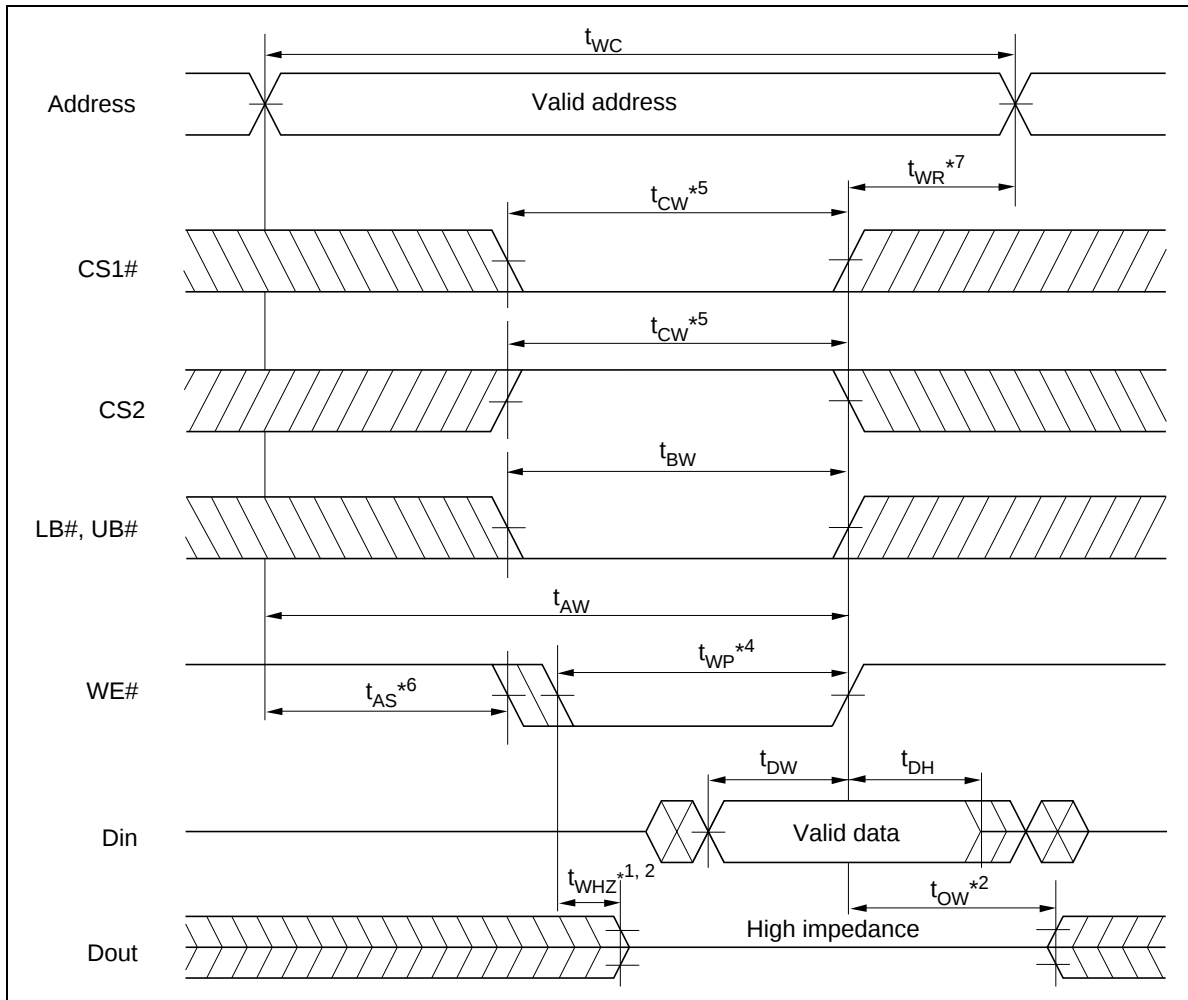
- Notes: 1.  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition,  $t_{LZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
5.  $t_{CW}$  is measured from the later of CS1# going low or CS2 going high to the end of write.
6.  $t_{AS}$  is measured from the address valid to the beginning of write.
7.  $t_{WR}$  is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

## Timing Waveform

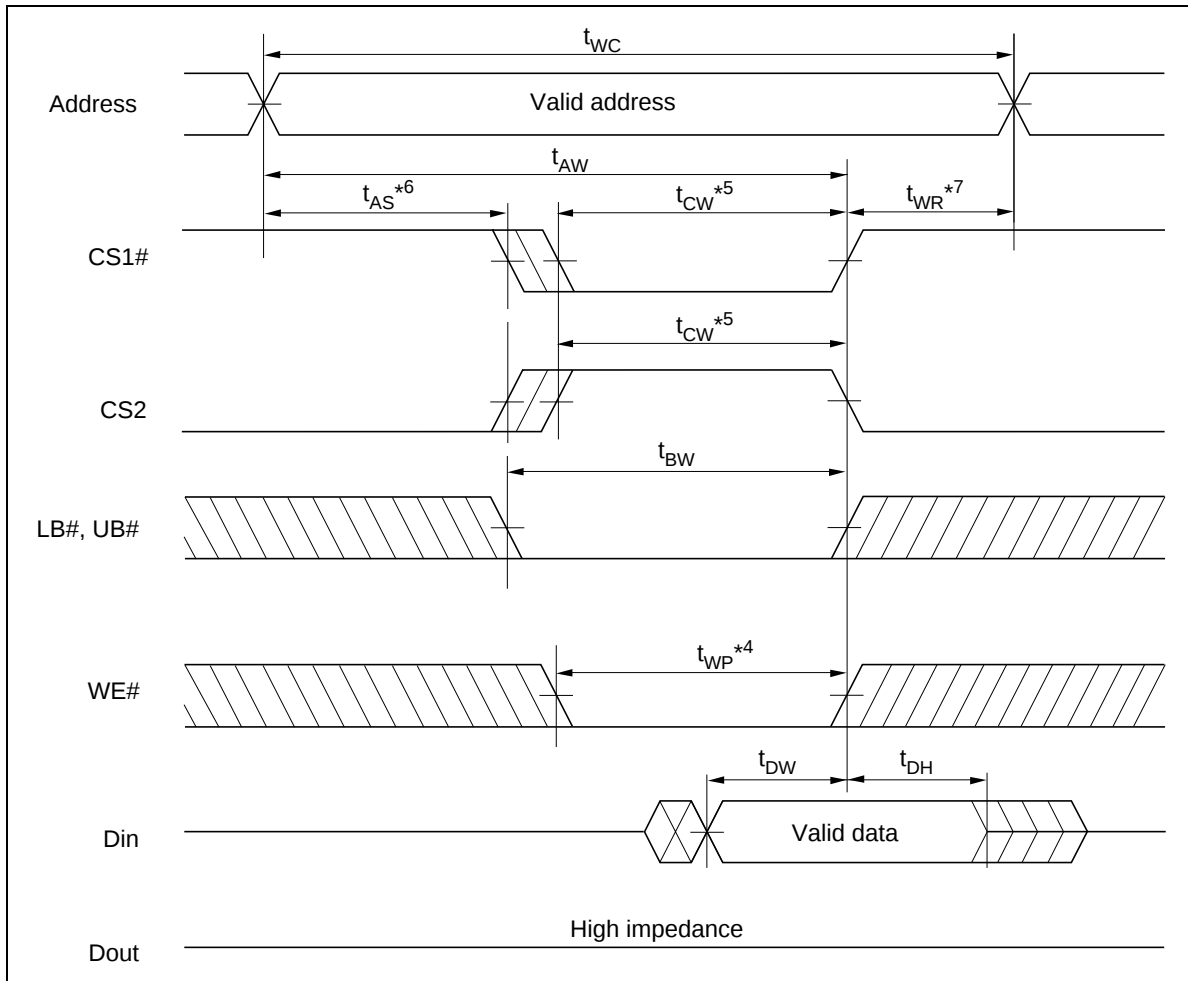
Read Timing Waveform ( $WE\# = V_{IH}$ )



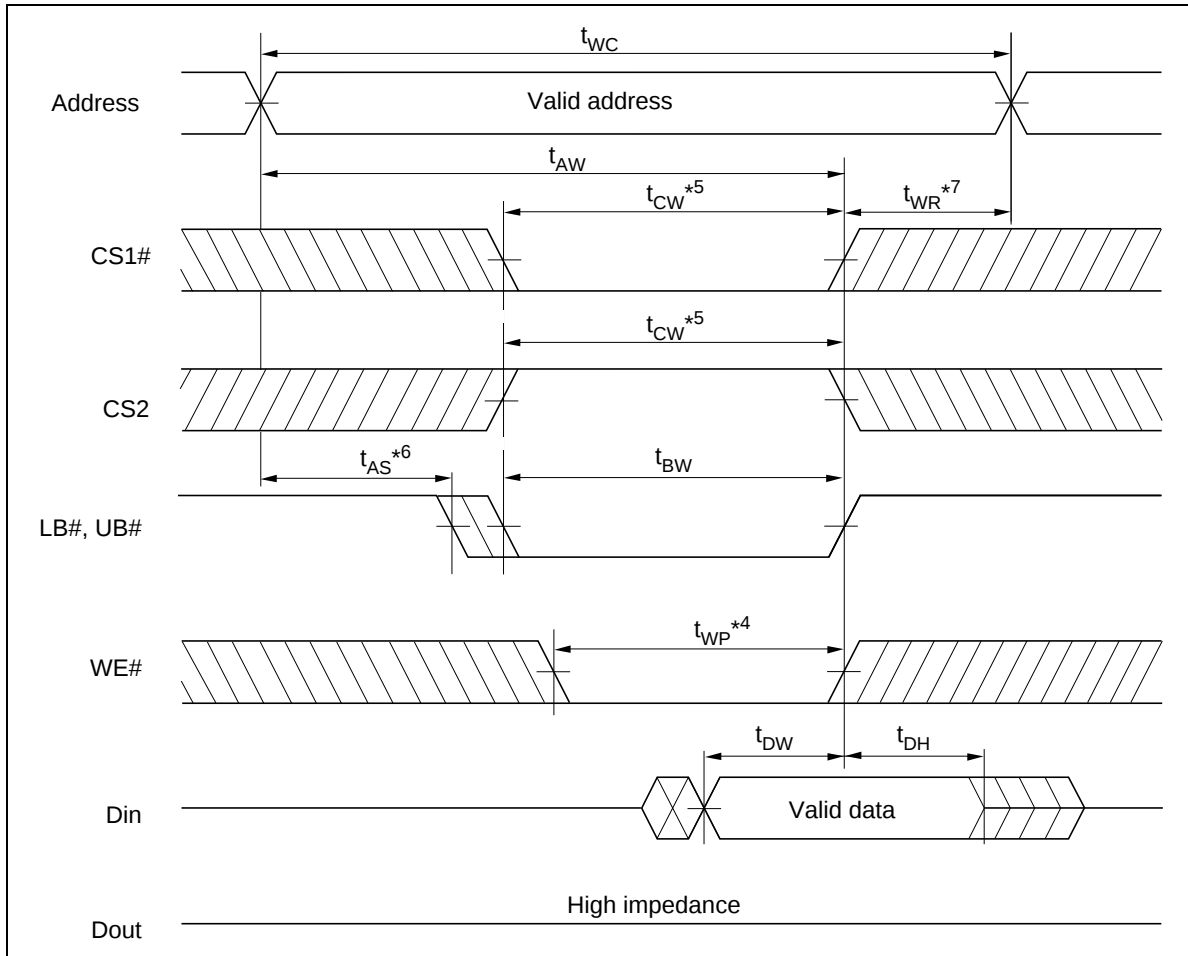
Write Timing Waveform (1) (WE# Clock)



Write Timing Waveform (2) (CS# Clock, OE# = V<sub>ih</sub>)



**Write Timing Waveform (3)** (LB#, UB# Clock, OE# = V<sub>ih</sub>)



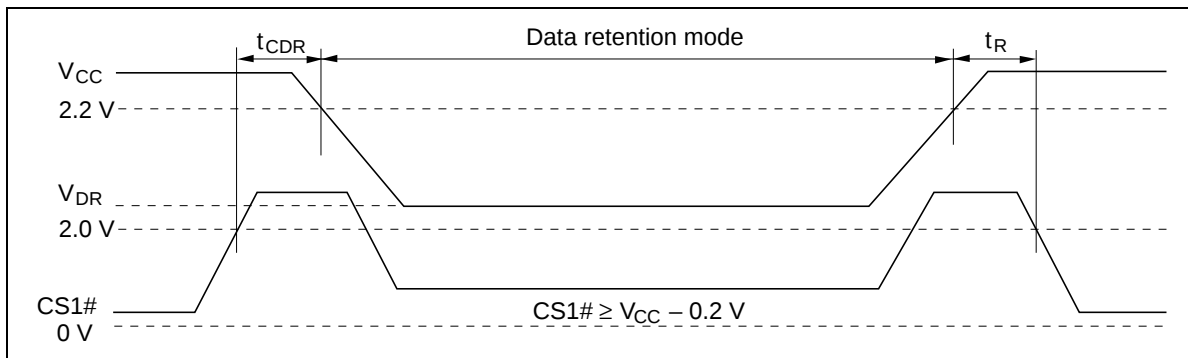
## Low $V_{CC}$ Data Retention Characteristics

( $T_a = -40$  to  $+85^\circ\text{C}$ )

| Parameter                            | Symbol                                     | Min             | Typ <sup>*4</sup> | Max | Unit | Test conditions <sup>*3</sup>                                                                                                                                                                                                                                                                                               |
|--------------------------------------|--------------------------------------------|-----------------|-------------------|-----|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{CC}$ for data retention          | $V_{DR}$                                   | 2               | —                 | —   | V    | $V_{in} \geq 0\text{V}$<br>(1) $0\text{V} \leq \text{CS2} \leq 0.2\text{V}$ or<br>(2) $\text{CS2} \geq V_{CC} - 0.2\text{V}$ ,<br>$\text{CS1\#} \geq V_{CC} - 0.2\text{V}$ or<br>(3) $\text{LB\#} = \text{UB\#} \geq V_{CC} - 0.2\text{V}$ ,<br>$\text{CS2} \geq V_{CC} - 0.2\text{V}$ ,<br>$\text{CS1\#} \leq 0.2\text{V}$ |
| Data retention current               | to $+85^\circ\text{C}$                     | $I_{CCDR}^{*1}$ | —                 | —   | 20   | $\mu\text{A}$ $V_{CC} = 3.0\text{V}$ , $V_{in} \geq 0\text{V}$                                                                                                                                                                                                                                                              |
|                                      |                                            | $I_{CCDR}^{*2}$ | —                 | —   | 10   | (1) $0\text{V} \leq \text{CS2} \leq 0.2\text{V}$ or<br>(2) $\text{CS2} \geq V_{CC} - 0.2\text{V}$ ,<br>$\text{CS1\#} \geq V_{CC} - 0.2\text{V}$ or<br>(3) $\text{LB\#} = \text{UB\#} \geq V_{CC} - 0.2\text{V}$ ,<br>$\text{CS2} \geq V_{CC} - 0.2\text{V}$ ,<br>$\text{CS1\#} \leq 0.2\text{V}$                            |
|                                      | to $+70^\circ\text{C}$                     | $I_{CCDR}^{*1}$ | —                 | —   | 20   | $\mu\text{A}$                                                                                                                                                                                                                                                                                                               |
|                                      |                                            | $I_{CCDR}^{*2}$ | —                 | —   | 10   |                                                                                                                                                                                                                                                                                                                             |
|                                      | to $+40^\circ\text{C}$                     | $I_{CCDR}^{*1}$ | —                 | 0.7 | 10   | $\mu\text{A}$                                                                                                                                                                                                                                                                                                               |
|                                      |                                            | $I_{CCDR}^{*2}$ | —                 | 0.7 | 3    |                                                                                                                                                                                                                                                                                                                             |
|                                      | $-40^\circ\text{C}$ to $+25^\circ\text{C}$ | $I_{CCDR}^{*1}$ | —                 | 0.5 | 10   | $\mu\text{A}$                                                                                                                                                                                                                                                                                                               |
|                                      |                                            | $I_{CCDR}^{*2}$ | —                 | 0.5 | 3    |                                                                                                                                                                                                                                                                                                                             |
| Chip deselect to data retention time | $t_{CDR}$                                  | 0               | —                 | —   | ns   | See retention waveform                                                                                                                                                                                                                                                                                                      |
| Operation recovery time              | $t_R$                                      | $t_{RC}^{*5}$   | —                 | —   | ns   |                                                                                                                                                                                                                                                                                                                             |

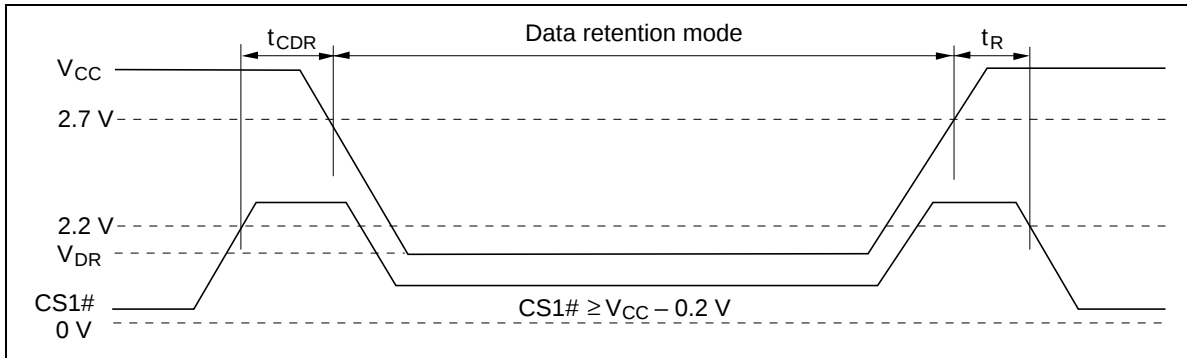
- Notes:
1. This characteristic is guaranteed only for L version.
  2. This characteristic is guaranteed only for SL version.
  3. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be  $\text{CS2} \geq V_{CC} - 0.2\text{V}$  or  $0\text{V} \leq \text{CS2} \leq 0.2\text{V}$ . The other input levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.
  4. Typical values are at  $V_{CC} = 3.0\text{V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.
  5.  $t_{RC}$  = read cycle time.

### Low $V_{CC}$ Data Retention Timing Waveform (1) (CS1# Controlled) ( $V_{CC} = 2.2\text{V}$ to $2.7\text{V}$ )

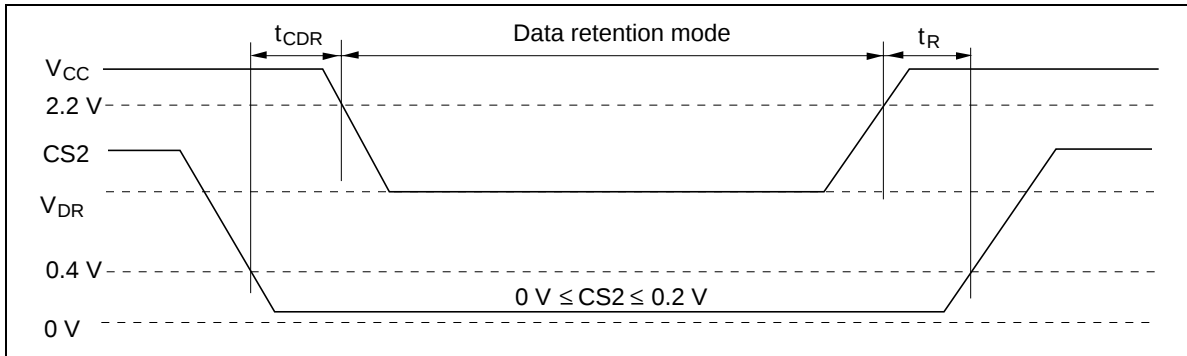


## R1LV0416C-I Series

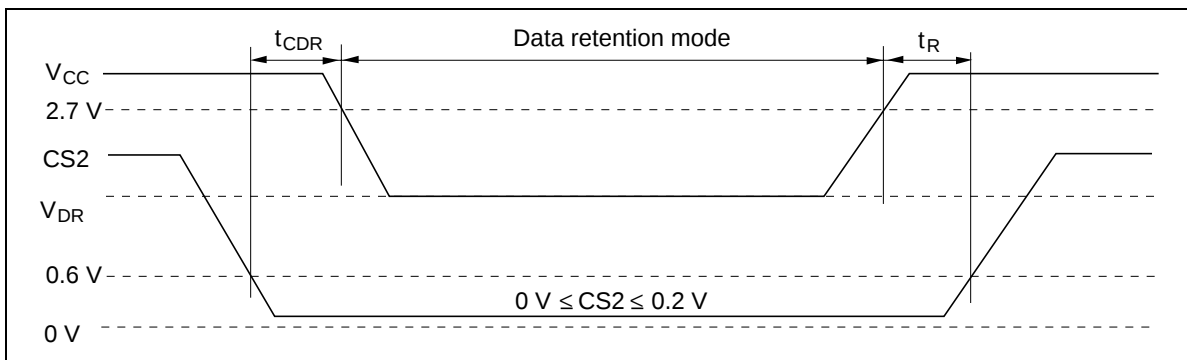
**Low  $V_{CC}$  Data Retention Timing Waveform (2) (CS1# Controlled) ( $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$ )**



**Low  $V_{CC}$  Data Retention Timing Waveform (3) (CS2 Controlled) ( $V_{CC} = 2.2\text{ V}$  to  $2.7\text{ V}$ )**

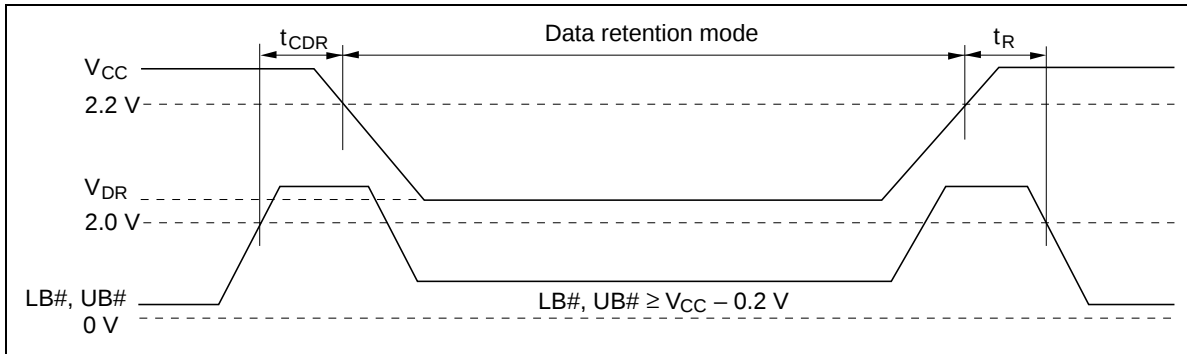


**Low  $V_{CC}$  Data Retention Timing Waveform (4) (CS2 Controlled) ( $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$ )**

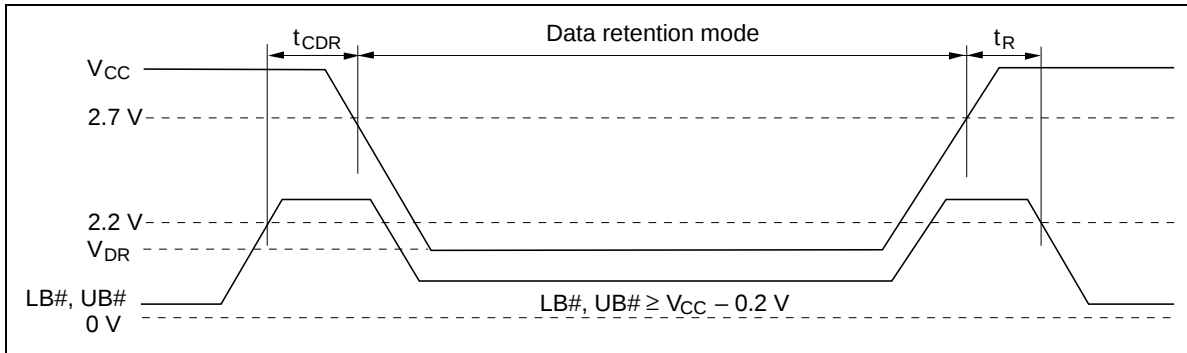


## R1LV0416C-I Series

### Low $V_{CC}$ Data Retention Timing Waveform (5) (LB#, UB# Controlled) ( $V_{CC} = 2.2\text{ V}$ to $2.7\text{ V}$ )



### Low $V_{CC}$ Data Retention Timing Waveform (6) (LB#, UB# Controlled) ( $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ )



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**Revision Record**

| <b>Rev.</b> | <b>Date</b>   | <b>Contents of Modification</b> | <b>Drawn by</b> | <b>Approved by</b> |
|-------------|---------------|---------------------------------|-----------------|--------------------|
| 1.00        | Aug. 05, 2003 | Initial issue                   |                 |                    |

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