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# R1LV0408C-I Series

Wide Temperature Range Version  
4 M SRAM (512-kword  $\times$  8-bit)

REJ03C0098-0100Z

Rev. 1.00

Jul.24.2003

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## Description

The R1LV0408C-I is a 4-Mbit static RAM organized 512-kword  $\times$  8-bit. R1LV0408C-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The R1LV0408C-I Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 32-pin SOP, 32-pin TSOP II and 32-pin STSOP.

## Features

- Single 3 V supply: 2.7 V to 3.6 V
- Access time: 55/70 ns (max)
- Power dissipation:
  - Active: 6 mW/MHz (typ)
  - Standby: 2.4  $\mu$ W (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Directly TTL compatible.
  - All inputs and outputs
- Battery backup operation.
- Operating temperature:  $-40$  to  $+85^{\circ}\text{C}$

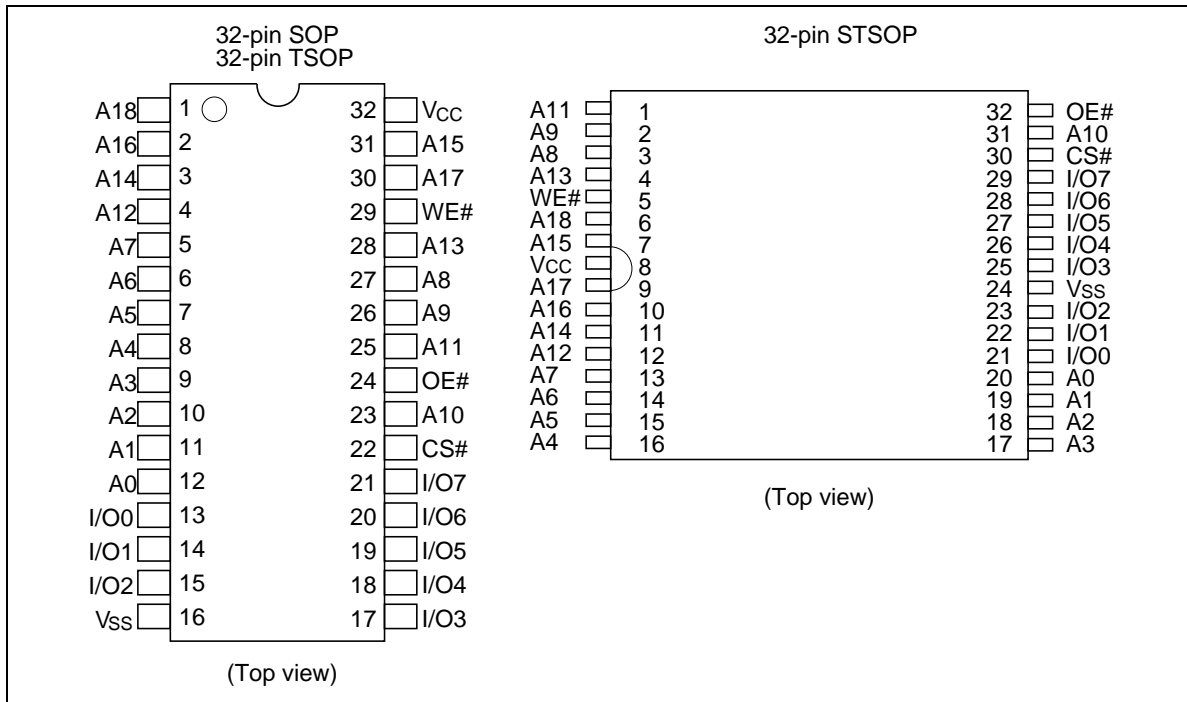
## R1LV0408C-I Series

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### Ordering Information

Type No.	Access time	Package
R1LV0408CSP-5SI	55 ns	525-mil 32-pin plastic SOP (32P2M-A)
R1LV0408CSP-7LI	70 ns	
R1LV0408CSB-5SI	55 ns	400-mil 32-pin plastic TSOP II (32P3Y-H)
R1LV0408CSB-7LI	70 ns	
R1LV0408CSA-5SI	55 ns	8mm × 13.4mm STSOP (32P3K-B)
R1LV0408CSA-7LI	70 ns	

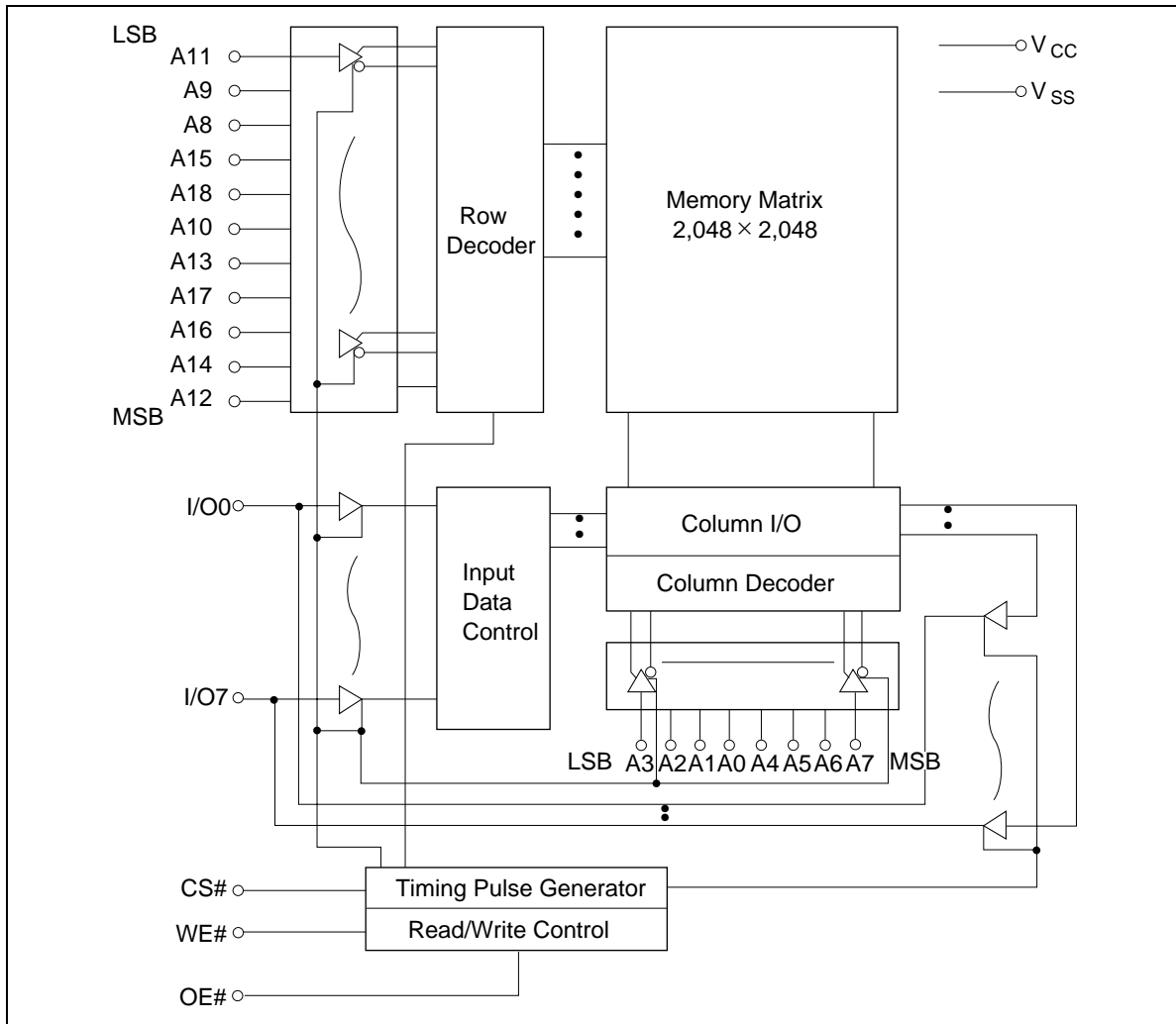
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS# ( $\overline{\text{CS}}$ )	Chip select
OE# ( $\overline{\text{OE}}$ )	Output enable
WE# ( $\overline{\text{WE}}$ )	Write enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground

## Block Diagram



## R1LV0408C-I Series

### Operation Table

WE#	CS#	OE#	Mode	V <sub>CC</sub> current	I/O0 to I/O7	Ref. cycle
×	H	×	Not selected	I <sub>SB1</sub> , I <sub>SB1</sub>	High-Z	—
H	L	H	Output disable	I <sub>CC</sub>	High-Z	—
H	L	L	Read	I <sub>CC</sub>	Dout	Read cycle
L	L	H	Write	I <sub>CC</sub>	Din	Write cycle (1)
L	L	L	Write	I <sub>CC</sub>	Din	Write cycle (2)

Note: H: V<sub>IH</sub>, L: V<sub>IL</sub>, ×: V<sub>IH</sub> or V<sub>IL</sub>

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V <sub>SS</sub>	V <sub>CC</sub>	−0.5 to +4.6	V
Terminal voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	−0.5* <sup>1</sup> to V <sub>CC</sub> + 0.5* <sup>2</sup>	V
Power dissipation	P <sub>T</sub>	0.7	W
Operating temperature	T <sub>opr</sub>	−40 to +85	°C
Storage temperature range	T <sub>stg</sub>	−65 to +150	°C
Storage temperature range under bias	T <sub>bias</sub>	−40 to +85	°C

Notes: 1. V<sub>T</sub> min: −3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is +7.0 V.

### DC Operating Conditions

(T<sub>a</sub> = −40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V
	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	−0.3* <sup>1</sup>	—	0.6	V

Note: 1. V<sub>IL</sub> min: −3.0 V for pulse half-width ≤ 30 ns.

## R1LV0408C-I Series

### DC Characteristics

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	$\mu A$	$V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	$\mu A$	$CS\# = V_{IH}$ or $OE\# = V_{IH}$ or $WE\# = V_{IL}$ or $V_{IO} = V_{SS}$ to $V_{CC}$
Operating current	$I_{CC}$	—	5	10	mA	$CS\# = V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA
Average operating current	$I_{CC1}$	—	8	25	mA	Min. cycle, duty = 100%, $CS\# = V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA
	$I_{CC2}$	—	2	5	mA	Cycle time = 1 $\mu s$ , duty = 100%, $I_{IO} = 0$ mA, $CS\# \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current	$I_{SB}$	—	0.1	0.3	mA	$CS\# = V_{IH}$
Standby current	to +85°C	$I_{SB1}$	—	20 <sup>*2</sup>	$\mu A$	$V_{in} \geq 0$ V, $CS\# \geq V_{CC} - 0.2$ V
			—	10 <sup>*3</sup>	$\mu A$	
	to +70°C	$I_{SB1}$	—	16 <sup>*2</sup>	$\mu A$	
			—	8 <sup>*3</sup>	$\mu A$	
	to +40°C	$I_{SB1}$	—	0.7 <sup>*2</sup>	10 <sup>*2</sup>	
			—	0.7 <sup>*3</sup>	3 <sup>*3</sup>	
	-40°C to +25°C	$I_{SB1}$	—	0.5 <sup>*2</sup>	10 <sup>*2</sup>	
			—	0.5 <sup>*3</sup>	3 <sup>*3</sup>	
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1$ mA
	$V_{OL2}$	—	—	0.2	V	$I_{OL} = 100$ $\mu A$
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1.0$ mA
	$V_{OH2}$	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -0.1$ mA

Notes: 1. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = +25^\circ C$  and specified loading, and not guaranteed.

2. L version. (-7LI)

3. SL version. (-5SI)

### Capacitance

( $T_a = +25^\circ C$ ,  $f = 1.0$  MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0$ V	1
Input/output capacitance	$C_{IO}$	—	—	10	pF	$V_{IO} = 0$ V	1

Note: 1. This parameter is sampled and not 100% tested.

## R1LV0408C-I Series

### AC Characteristics

(Ta = -40 to +85°C, V<sub>CC</sub> = 2.7 V to 3.6 V, unless otherwise noted.)

#### Test Conditions

- Input pulse levels: V<sub>IL</sub> = 0.4 V, V<sub>IH</sub> = 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C<sub>L</sub> (50 pF) (R1LV0408C-5I)  
1 TTL Gate + C<sub>L</sub> (100 pF) (R1LV0408C-7I)  
(Including scope and jig)

#### Read Cycle

Parameter	Symbol	R1LV0408C-I				Unit	Notes
		-5		-7			
		Min	Max	Min	Max		
Read cycle time	t <sub>RC</sub>	55	—	70	—	ns	
Address access time	t <sub>AA</sub>	—	55	—	70	ns	
Chip select access time	t <sub>CO</sub>	—	55	—	70	ns	
Output enable to output valid	t <sub>OE</sub>	—	30	—	35	ns	
Chip select to output in low-Z	t <sub>LZ</sub>	10	—	10	—	ns	2
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	ns	2
Chip deselect to output in high-Z	t <sub>HZ</sub>	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	ns	1, 2
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns	

## R1LV0408C-I Series

### Write Cycle

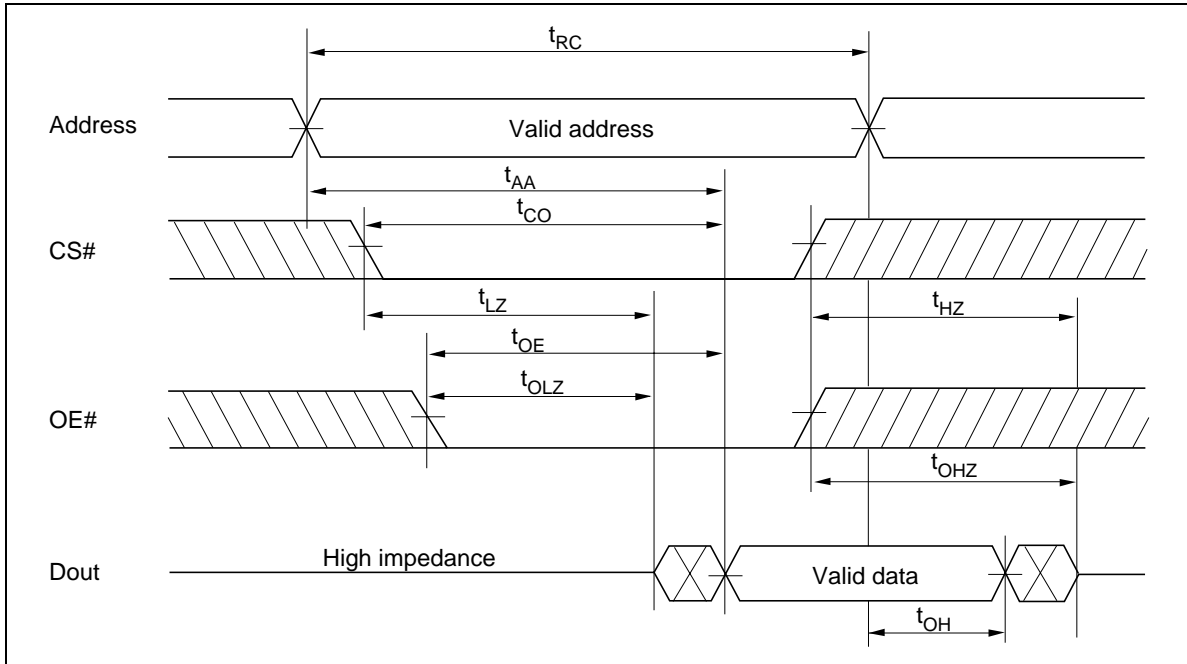
		R1LV0408C-I					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t <sub>WC</sub>	55	—	70	—	ns	
Chip selection to end of write	t <sub>CW</sub>	50	—	60	—	ns	4
Address setup time	t <sub>AS</sub>	0	—	0	—	ns	5
Address valid to end of write	t <sub>AW</sub>	50	—	60	—	ns	
Write pulse width	t <sub>WP</sub>	40	—	50	—	ns	3, 12
Write recovery time	t <sub>WR</sub>	0	—	0	—	ns	6
Write to output in high-Z	t <sub>WHZ</sub>	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t <sub>DW</sub>	25	—	30	—	ns	
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns	
Output active from end of write	t <sub>OW</sub>	5	—	5	—	ns	2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	ns	1, 2, 7

- Notes:
1.  $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. A write occurs during the overlap ( $t_{WP}$ ) of a low CS# and a low WE#. A write begins at the later transition of CS# going low or WE# going low. A write ends at the earlier transition of CS# going high or WE# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  4.  $t_{CW}$  is measured from CS# going low to the end of write.
  5.  $t_{AS}$  is measured from the address valid to the beginning of write.
  6.  $t_{WR}$  is measured from the earlier of WE# or CS# going high to the end of write cycle.
  7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
  8. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
  9. Dout is the same phase of the write data of this write cycle.
  10. Dout is the read data of next address.
  11. If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
  12. In the write cycle with OE# low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

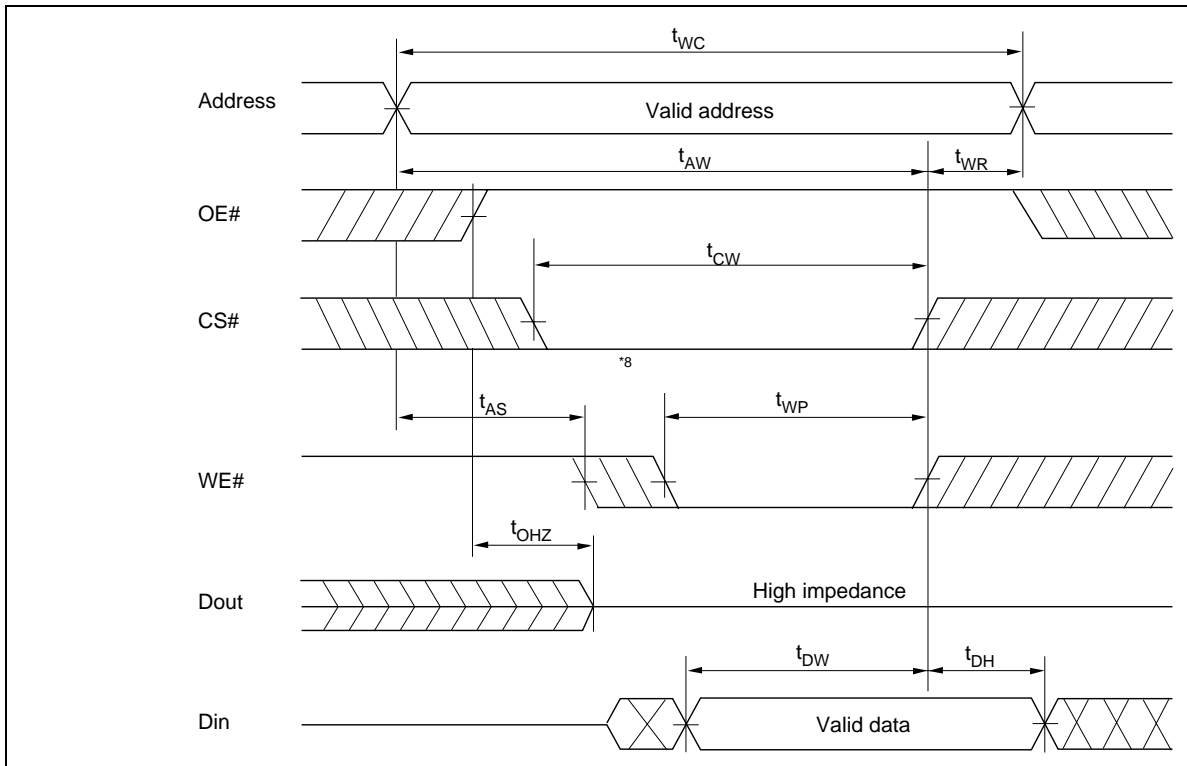


## Timing Waveform

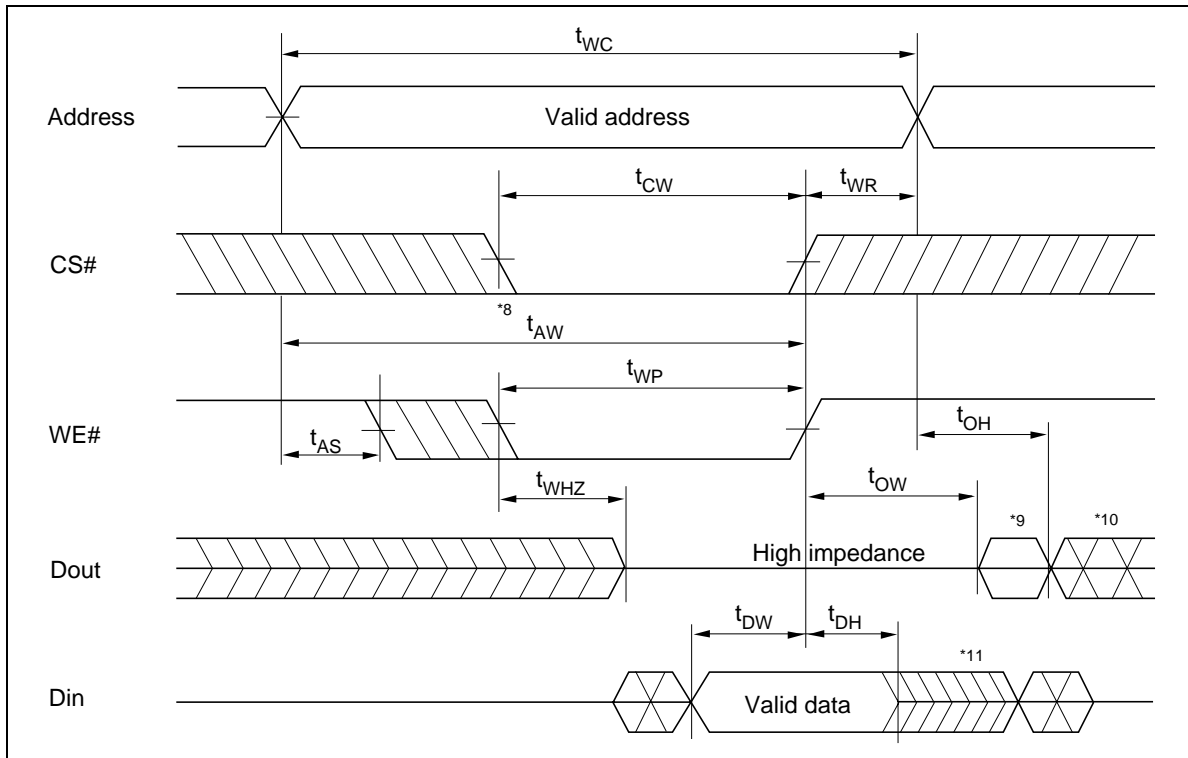
### Read Timing Waveform ( $WE\# = V_{IH}$ )



Write Timing Waveform (1) (OE# Clock)



Write Timing Waveform (2) (OE# Low Fixed)



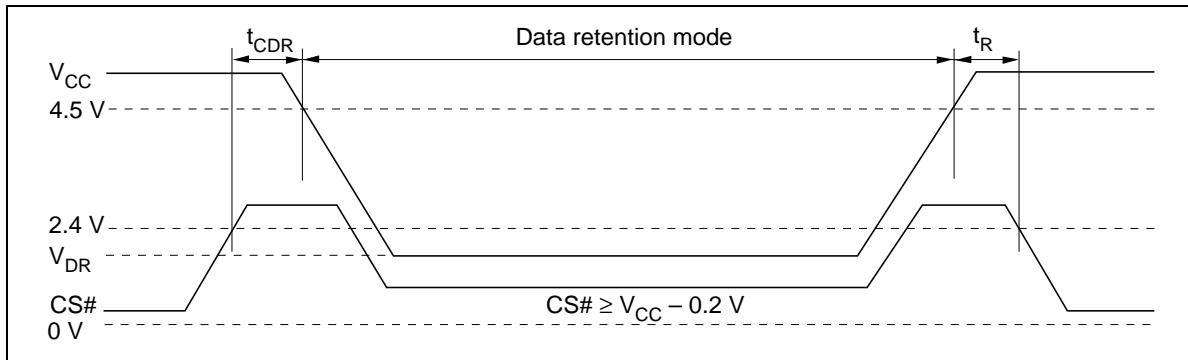
## Low $V_{CC}$ Data Retention Characteristics

( $T_a = -40$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Min	Typ <sup>*4</sup>	Max	Unit	Test conditions <sup>*3</sup>
$V_{CC}$ for data retention	$V_{DR}$	2	—	—	V	$CS\# \geq V_{CC} - 0.2\text{ V}$ , $V_{in} \geq 0\text{ V}$
Data retention current	to $+85^\circ\text{C}$	$I_{CCDR}^{*1}$	—	20	$\mu\text{A}$	$V_{CC} = 3.0\text{ V}$ , $V_{in} \geq 0\text{ V}$
		$I_{CCDR}^{*2}$	—	10		$CS\# \geq V_{CC} - 0.2\text{ V}$
	to $+70^\circ\text{C}$	$I_{CCDR}^{*1}$	—	16	$\mu\text{A}$	
		$I_{CCDR}^{*2}$	—	8		
	to $+40^\circ\text{C}$	$I_{CCDR}^{*1}$	—	10	$\mu\text{A}$	
		$I_{CCDR}^{*2}$	—	3		
	$-40^\circ\text{C}$ to $+25^\circ\text{C}$	$I_{CCDR}^{*1}$	—	10	$\mu\text{A}$	
		$I_{CCDR}^{*2}$	—	3		
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}^{*5}$	—	—	ns	

- Notes:
1. This characteristic is guaranteed only for L version.
  2. This characteristic is guaranteed only for SL version.
  3.  $CS\#$  controls address buffer,  $WE\#$  buffer,  $OE\#$  buffer, and  $Din$  buffer. In data retention mode,  $V_{in}$  levels (address,  $WE\#$ ,  $OE\#$ ,  $I/O$ ) can be in the high impedance state.
  4. Typical values are at  $V_{CC} = 3.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.
  5.  $t_{RC}$  = read cycle time.

### Low $V_{CC}$ Data Retention Timing Waveform ( $CS\#$ Controlled)



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**Revision Record**

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1.00	Jul. 24, 2003	Initial issue		

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