

QLUM3316-PQ280C Device Datasheet



..... Utopia Level 3 Master/Master Bridge

1.0 Utopia Level 3 (L3) Bridge Features

- Implements two Utopia L3 Masters providing a solution to bridge Utopia Slave devices
- Compliant with ATM-Forum af-phy-0136.000 (Utopia L3)
- Meets 90MHz performance offering up to 1.4Gbps cell rate transfers
- Single chip solution for improved system integration
- Support cell level transfer mode
- Cell and clock rate decoupling with on chip FIFOs
- Up to 1.5 KByte of on chip FIFO per data direction
- Integrated management interface and built-in errored cell discard
- ATM Cell size programmable via external pins from 16 to 128 bytes
- Optional Utopia parity generation/checking enable/disable via external pin
- Built in JTAG port (IEEE1149 compliant)
- Simulation model available for system level verification (Contact Quicklogic for details)
- Solution also available as flexible Soft-IP core, delivered with a full device modelization and verification testbenches



2.0 Utopia Overview

The Utopia (Universal Test & Operations PHY Interface for ATM) interface is defined by the ATM Forum to provide a standard interface between ATM devices and ATM PHY or SAR (segmentation and Re-assembly) devices.

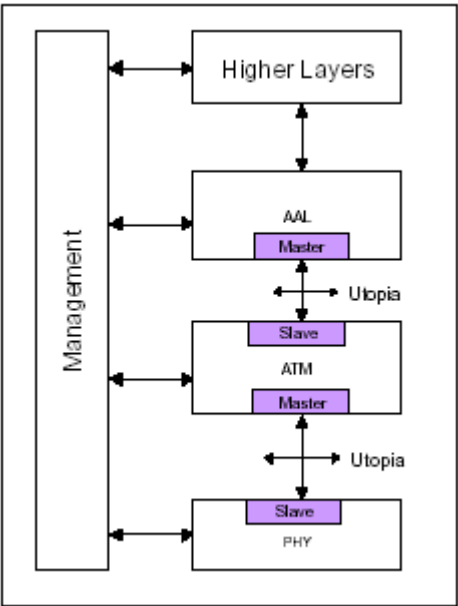


Figure 1: Utopia Reference Model

The Utopia Standard defines a full duplex bus interface with a Master/Slave paradigm. The Slave interface responds to the requests from the Master. The Master performs PHY arbitration and initiates data transfers to and from the Slave device.

The ATM forum has standardized the Utopia Levels 1 (L1) to 3 (L3). Each level extends the maximum supported interface speed from OC3, 155Mbps (L1) over OC12, 622Mbps (L2) to 3.2Gbit/s (L3).

The following Table 1 gives an overview of the main differences in these three levels.

Table 1: Utopia Level Differences

Utopia Level	Interface Width	Max. Interface Speed	Maximum Throughput
1	8-bit	25 MHz	200 Mbps (typ. OC3 155 Mbps)
2	8-bit, 16-bit	50 MHz	800 Mbps (typ. OC12 622 Mbps)
3	8-bit, 32-bit	104 MHz	3.2 Gbps (typ. OC48 2.5 Gbps)

Utopia Level 1 implements an 8-bit interface running at up to 25MHz. Level 2 adds a 16 Bit interface and increases the speed to 50MHz. Level 3 extends the interface further by a 32 Bit word-size and speeds up to 104MHz providing rates up to 3.2 Gbit/s over the interface.

In addition to the differences in throughput, Utopia Level 2 uses a shared bus offering to physically share a single interface bus between one master and up to 31 slave devices (Multi-PHY or MPHY operation). This allows the implementation of aggregation units that multiplex several slave devices to a single Master device. The Level 2 and Level 3 are point-to-point only, whereas Level 1 has no notion of multiple slaves. Level 3 still has the notion of multiple slaves, but they must be implemented in a single physical device connected to the Utopia Interface.

3.0 Utopia Master/Master Bridge Application

As it is not possible to connect two Slave devices together, the Master/Master Bridge provides the necessary interfaces to convey between two Slave devices as shown in Figure 2.

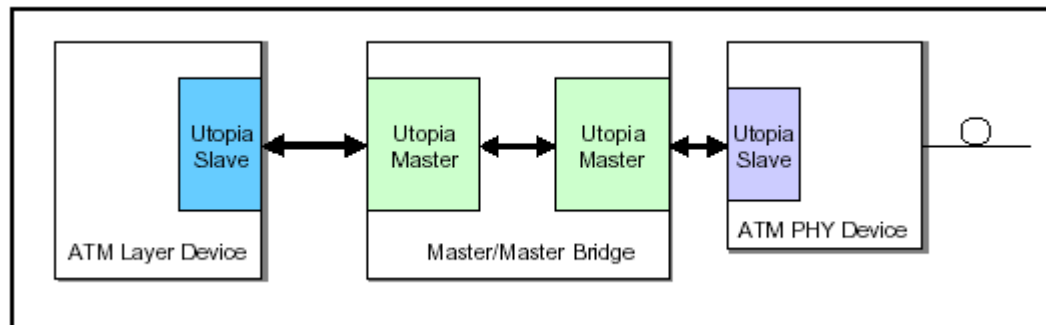


Figure 2: Utopia Master Bridge

The Bridge automatically transfers data as soon as it becomes available from one side to the other. Internal asynchronous FIFOs enable independent clock domains for each interface.

4.0 Application

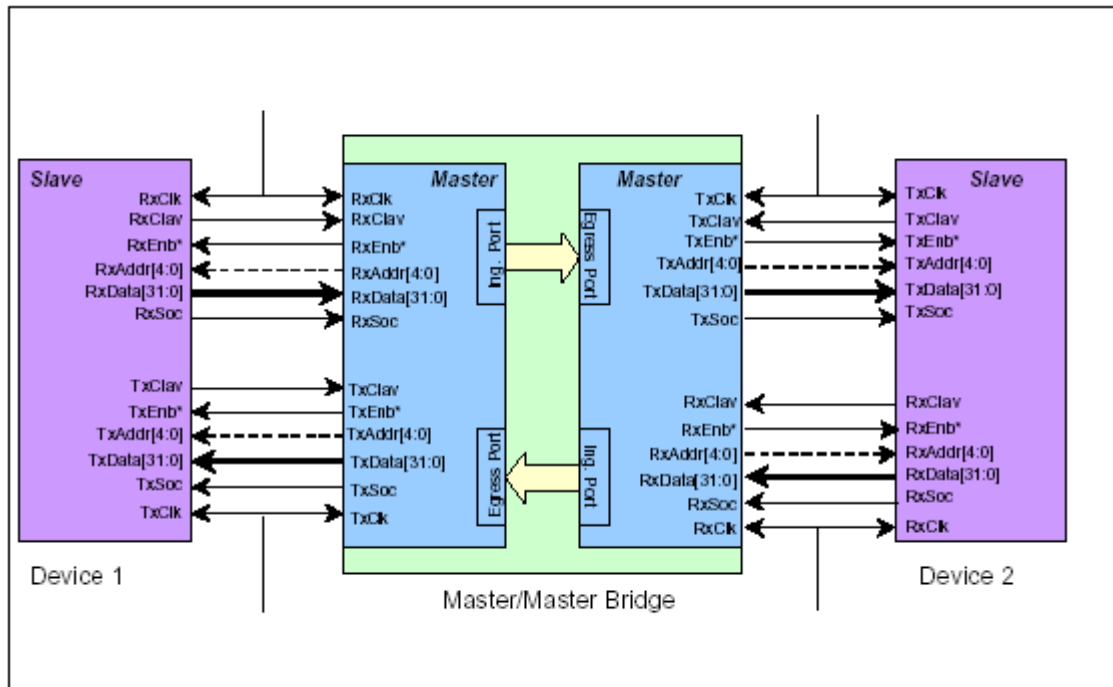


Figure 3: Master/Master Bridge connecting two Slave Devices

Data flows from the Bridge's RX Ports to the corresponding TX Ports on the other side of the bridge.

5.0 Core Pinout

Bridge Core implements all the required Utopia signals and provides all the Utopia optional signals (Indicated by an 'O' in the following tables).

In addition to the Utopia Interface signals, error indication signals are available for error monitoring or statistics. An error indication always shows that a cell has been discarded by the bridge. Possible errors are parity or cell-length errors on the receive interface of the corresponding Utopia Interfaces.

All Utopia interfaces work in the same transfer mode (cell level).

To identify the sides of the bridge, the notion "WEST" and "EAST" for the corresponding interfaces will be used.

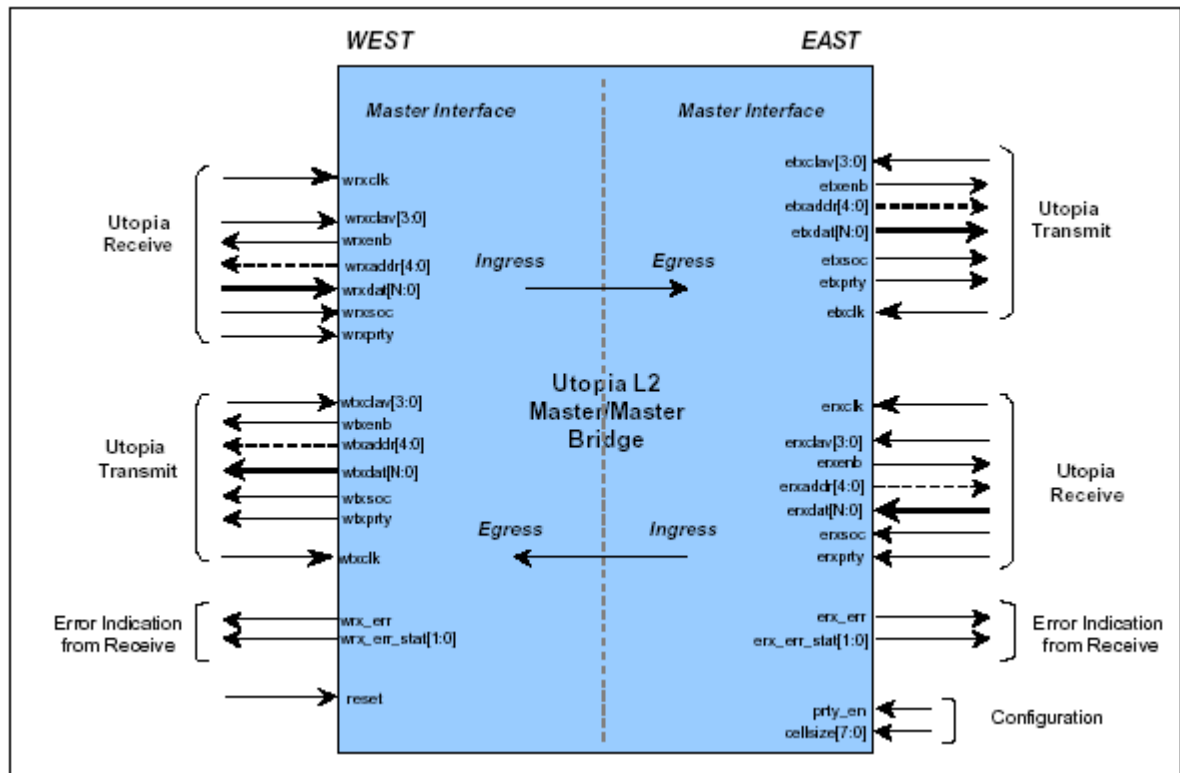


Figure 4: Utopia Level 3 Master/Master Bridge Top Entity

5.1 Signal Descriptions

Table 2: Global Signal

Pin	Mode	Description
reset	In	Active high chip reset

Table 3: Device Management Interface

Pin	Mode	Description
wrx_err	Out	Receive error indication on west receive interface. When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the west interface and is discarded.
wrx_err_stat(1:0)	Out	Receive error status information for west receive interface. When wrx_err is driven, indicates the error status of the discarded cell: <ul style="list-style-type: none"> wrx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. wrx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of ut_tx_soc on the Utopia interface within less than a complete cell time).
erx_err(n)	Out	Receive error indication on east receive interface(s). When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the east interface side.
erx_err_stat(n) (1:0)	Out	Receive error status information for east receive interface. When erx_err is driven, indicates the error status of the discarded cell: <ul style="list-style-type: none"> erx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. erx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of ut_tx_soc on the Utopia interface within less than a complete cell time).

NOTE: wrx_.. signals are sampled with west receive clock (wrxclk). erx_.. signals are sampled with west transmit clock (wtxclk).

Table 4: West Utopia Master Transmit Interface

Pin	Mode	Description
wtxclk	In	90MHz transmit byte clock. The Core samples all Utopia Transmit signals on txcclk rising edge.
wtxdata[15:0]	Out	Transmit data bus.
wtxppty	Out	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave.
		When the parity check is disabled during the Core configuration, or not used in the design, the pin txppty should be left open.
wtxsoc	Out	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
wtxenb	Out	Active low transmit data transfer enable.
wtxclav[0]	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.
wtxclav[3:1] (O)	In	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected during the Core configuration, one txclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
wtxaddr[4:0]	Out	Utopia transmit address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

NOTE: (O) indicates optional signals.

Table 5: West Utopia Master Receive Interface

Pin	Mode	Description
wrxclk	In	90MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
wrxdata[15:0]	In	Receive data bus.
wrxprty(0)	In	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
wrxsoc	In	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
wrxenb	Out	Active low transmit data transfer enable.
wrxclav[0]	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.
wrxclav[3:1] (0)	In	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected, one rxclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
wrxaddn(4:0)	Out	Utopia receive address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Table 6: East Utopia Master Transmit Interface

Pin	Mode	Description
etxclk	In	90MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
etxdata[15:0]	Out	Transmit data bus.
etxprty	Out	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave. When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be left open.
etxsoc	Out	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
etxenb	Out	Active low transmit data transfer enable.
etxclav[0]	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.
etxclav[3:1] (0)	In	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected during the Core configuration, one txclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
etxaddr[4:0]	Out	Utopia transmit address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Table 7: East Utopia Master Receive Interface

Pin	Mode	Description
erxclk	In	90MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
erxdata[15:0]	In	Receive data bus.
erxperty (0)	In	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxperty can be let unconnected.
erxsoc	In	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
erxenb	Out	Active low transmit data transfer enable.
erxclav[0]	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.
rxclav[3:1] (0)	In	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected, one rxclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
erxaddr(4:0)	Out	Utopia receive address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. taddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Table 8: Device Configuration Pins

Pin	Mode	Description
prty_en	In	Enable parity checking on the Utopia interface. If disabled (tied to 0), the wrx_err_stat(0) signal can be ignored and left open and the rx parity input should be tied to 0. Also the tx parity pins can be left open.
cellsize[7:0]	In	Define cellsize: sets the size in bytes of a cell. Binary value to be set usually by board wiring. The size must be a multiple of 2.

The configuration pins are not intended for change during operation. They are usually board wired to configure the device for operation.

6.0 Global Signal Descriptions

The externally provided Utopia Transmit and Receive clocks are connected to global resources to provide low skew and fast chip level distribution. In both data directions, the two corresponding Utopia Interfaces are decoupled by asynchronous FIFOs.

Therefore each interface runs completely independently each at its own tx and rx clocks which typically are 104 MHz.

The Error indications of the two receive interfaces are always sampled within the west clock domains. The errors of the east rx interface is available on the `erx_err` signal, which is handled using the west clock domain (`wtxclk`). The west rx error is directly derived from the west rx block (`wrxclk`).

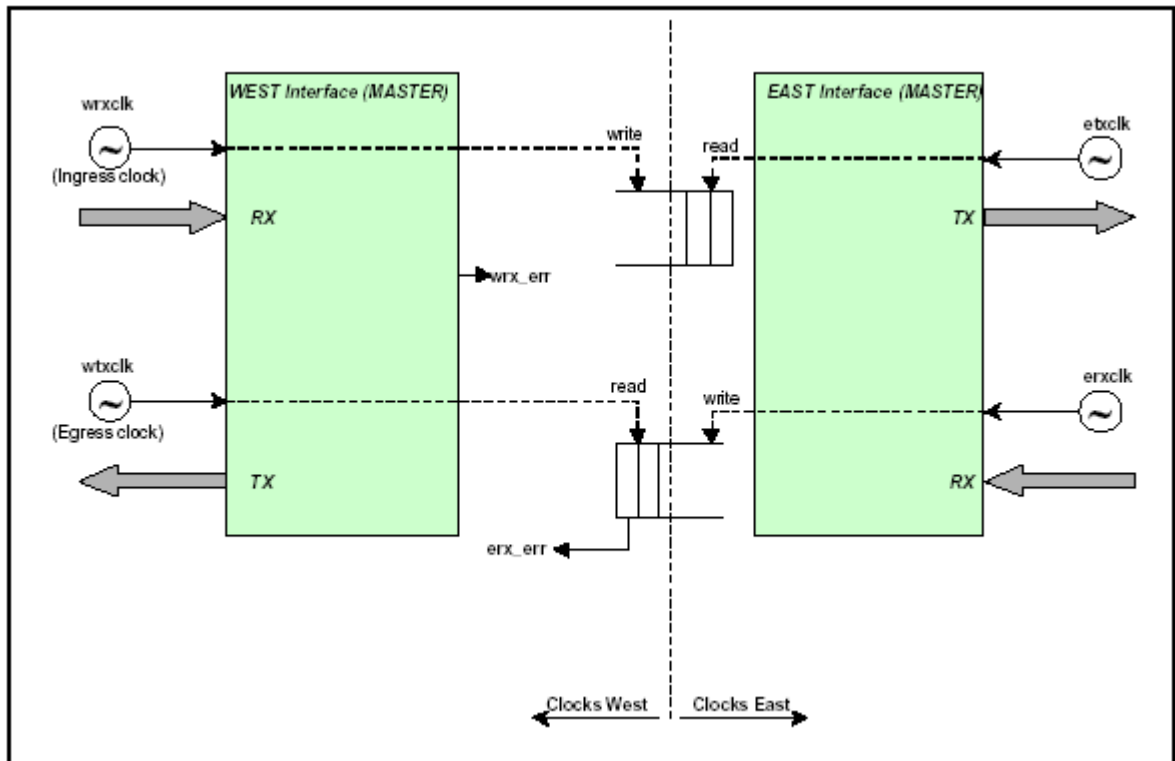


Figure 5: Master/Master Bridge Clock Distribution

7.0 Functional Description - Utopia Interface

The Utopia Bridge operates in single PHY mode. Therefore no address bus and only a single status pin (clav[0]) per direction is used on the interfaces.

7.1 Utopia Interface Single PHY Transmit Interface

The Transmit interface is controlled by the ATM layer.

The transmit interface has data flowing in the same direction as the ATM enable `ut_txenb`. The ATM transmit block generates all output signals on the rising edge of the `ut_txclk`.

Transmit data is transferred from the ATM layer to PHY layer via the following procedure. The Core indicates it can accept data using the `ut_txclav` signal, then the ATM layer drives data onto `ut_txdat` and asserts `ut_txenb`.

When a cell transfer is initiated, the Master or the Slave cannot pause the transfer by any means.

7.1.1 Single Cell Transfer

The Slave asserts `ut_txclav` **1** when it is capable of accepting the transfer of a whole cell. The Core asserts `ut_txenb` (Low) to indicate that it drives valid data to the Slave **2**. Together with the first word of a cell, the Core device asserts `ut_txsoc` for one clock cycle **3**.

To ensure that the ATM Layer (Core) does not cause transmit overrun, the Slave de-asserts `ut_txclav` when `ut_txsoc` is de-asserted by the Core **4**.

To complete the cell transfer, the Core de-asserts the Utopia enable signal `ut_txenb` **5**.

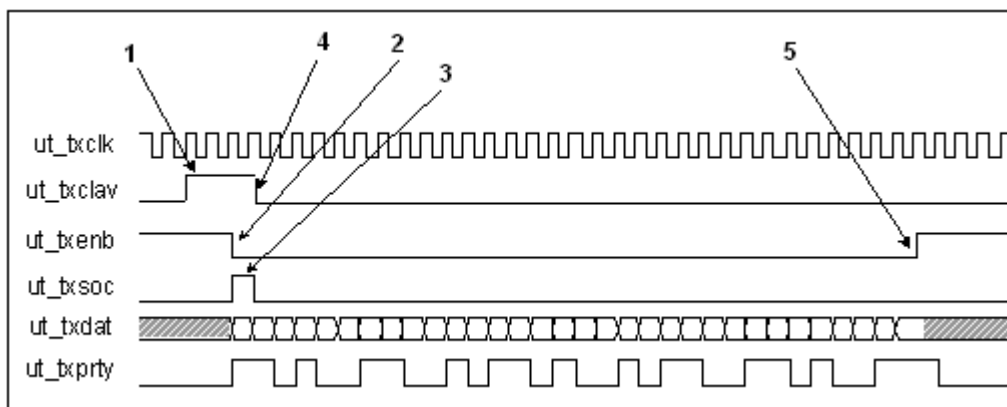


Figure 6: Single Cell Transfer - Cell Level Transfer

7.1.2 Back to Back Cells Transfer

When, during a cell transfer, the Slave is able to receive a subsequent cell, the Master can keep `ut_txenb` asserted between two cells **1** and asserts `ut_txsoc`, to start a new cell transfer, immediately after the last word of the previous cell **2**.

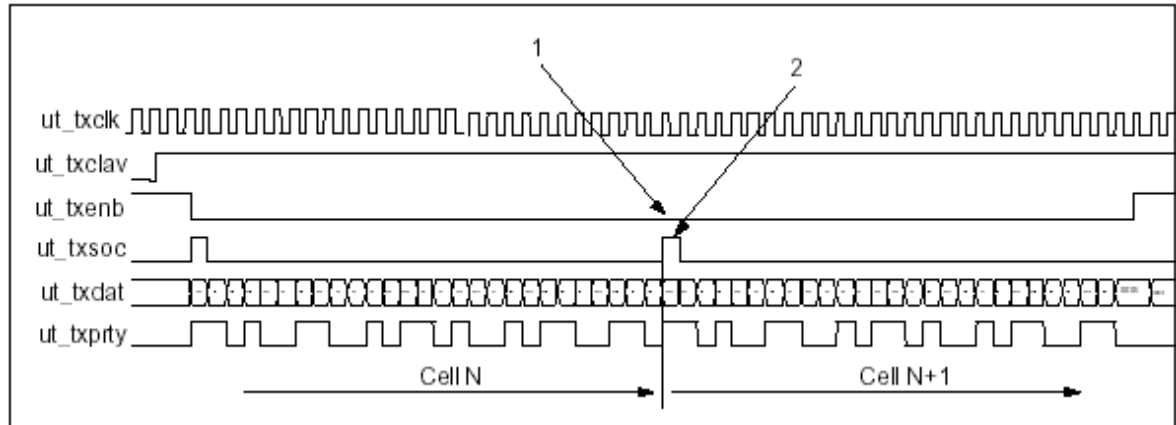


Figure 7: Back to Back Cell Transfer

7.2 Utopia Interface Single PHY Receive Interface

The Receive interface is controlled by the Master interface. The receive interface has data flowing in the opposite direction to the Master's enable `ut_rxenb`.

Receive data is transferred from the Slave to the Master via the following procedure. The Slave indicates it has valid data, then the Master asserts `ut_rxenb` to read this data from the Slave. The Master indicates valid data (thereby controlling the data flow) via the `ut_rxclav` signal.

When a cell transfer is initiated, the transfer cannot be paused by the Master or the Slave.

7.2.1 Cell Level Transfer - Single Cell

The Slave asserts `ut_rxclav` when it is ready to send a complete cell to the Master **1**. The Master interface asserts `ut_rxenb` to start the cell transfer **2**. The Slave samples `ut_rxenb` and start driving data on the following clock edge **3**. The Slave asserts `ut_rxsoc` together with the cell first word to indicate the start of a cell **4**.

The Master drives `ut_txenb` high two clock cycles before the expected end of the current cell if the Slave has no more cell to transfer **5**. The Slave de-asserts `ut_rxclav` to indicate that no new cell is available **6** together with the start of cell indication.

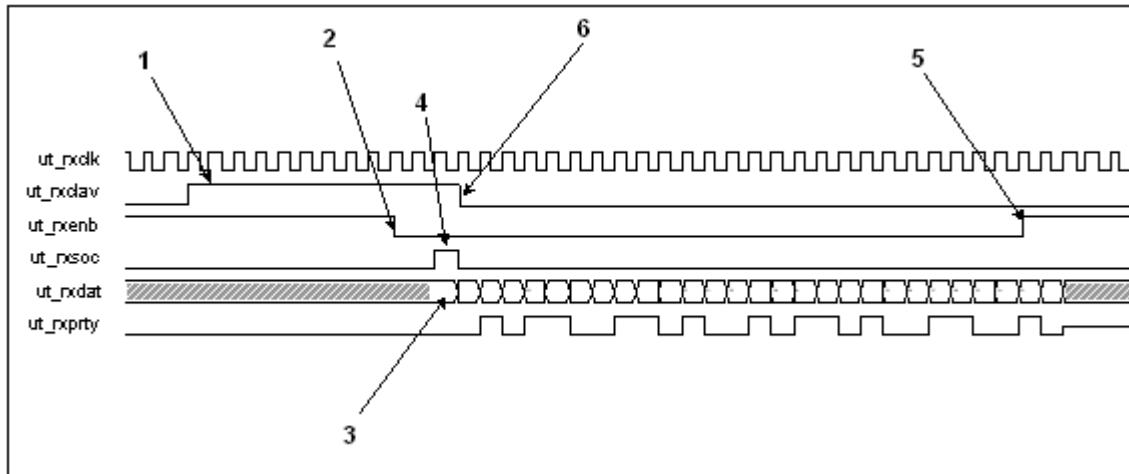


Figure 8: Single Cell Transfer

7.2.2 Cell Level Transfer - Back to Back Cells

If the Master keeps `ut_rxenb` asserted at the end of a cell transfer **1** and if the Slave has a new cell to send, the Slave keeps `ut_rxclav` drives the new cell asserting `ut_rxsoc` to indicate the start of a new cell **2**.

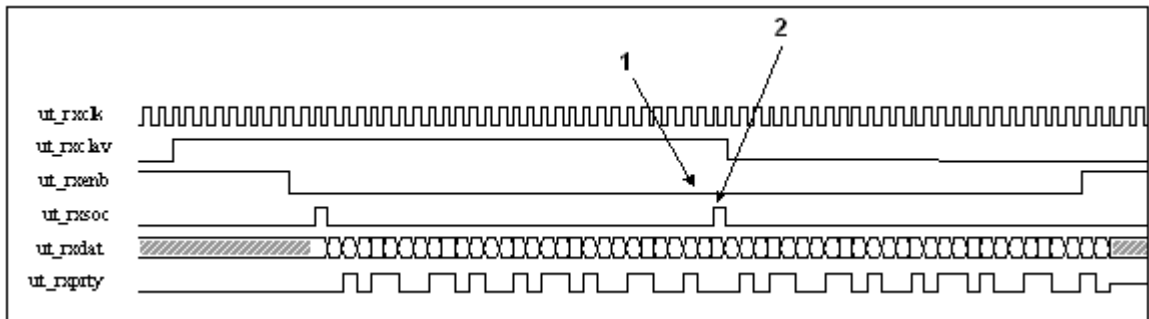


Figure 9: Back to Back Cells Transfer

8.0 Core Management and Error Handling

On Ingress, the Utopia Master Blocks are designed to handle and report Utopia errors such as Parity error or wrong cell length. Errored cells are discarded with an error status provided on pins for use by external management facilities.

The error handling only applies to the corresponding receive parts of the Core (i.e. Ingress Ports).

When an errored cell is received on the Utopia interface, the Core discards the complete cell and provides a cell discard indication (Signal `eg_err` asserted) **1** together with a cell discard status (Signal `eg_err_stat(1:0)`) **2**.

NOTE: `eg_err` is routed to the corresponding `wrx_err` and `erx_err` respectively (see Figure 4).

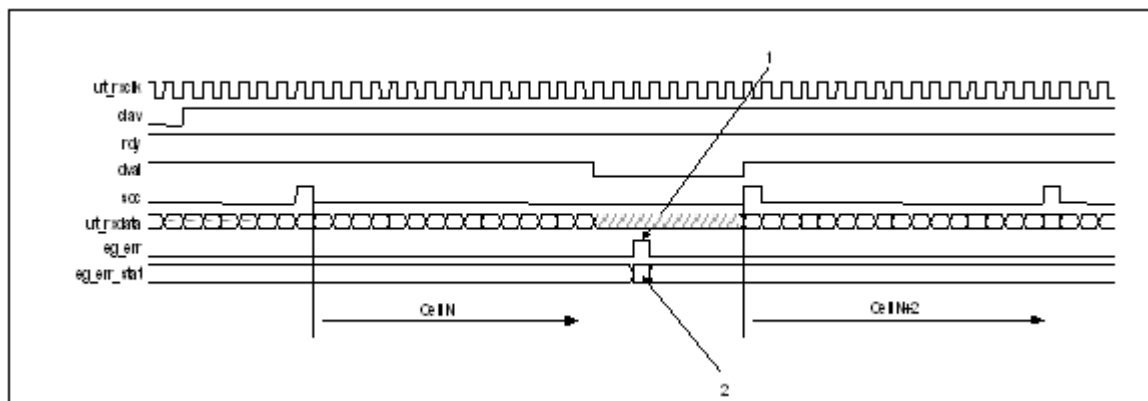


Figure 10: Cell Discard Indication

Table 9: Error Status Word Bit Coding

Error Status Bit	Name	Description
0	PARITY_ERR	Valid when <code>wrx/erx_err</code> is asserted. If set to one indicates that a cell is discarded with a parity error decoded by the Core.
1	LENGTH_ER	Valid when <code>wrx/erx_err</code> is asserted. If set to one indicates that a cell is discarded with a cell length error detected on the Utopia interface.

The signals are sampled on the corresponding clocks from the west interface:

- `erx_...` sampled with `wtxclk` (west transmit clock)
- `wrx_...` sampled with `wrxclk` (west receive clock)

9.0 Complexity and Performance Summary

9.1 Timing Parameters Definition

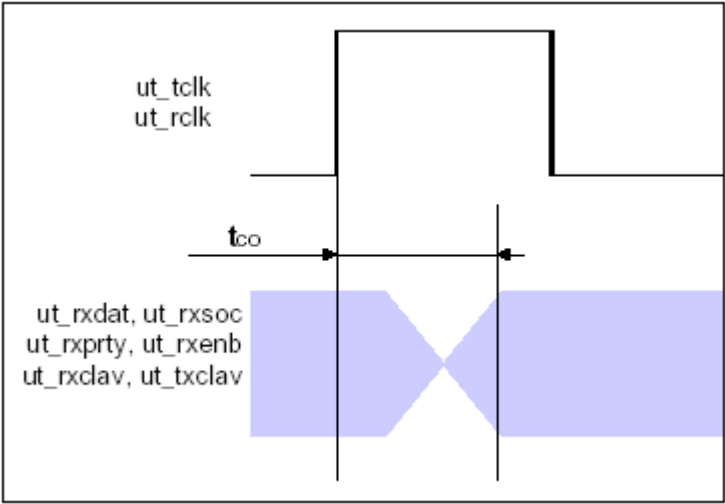


Figure 11: t_{co} Timing Parameter Definition

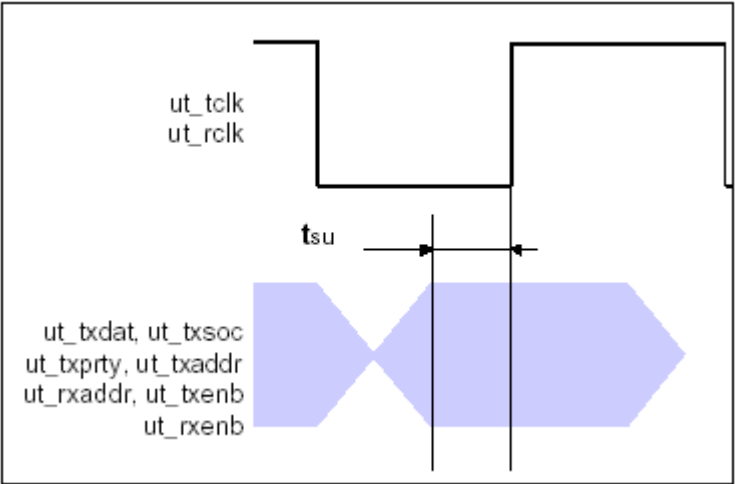


Figure 12: t_{su} Timing Parameter Definition

Table 10: 16-Bit Utopia Interface Timing Characteristics

Parameter	typ	Max (worst)	Unit
tco	7.0	6.0	ns
tsu	2.5	1.8	ns
wrxclk		90	MHz
wtxclk		90	MHz
erxclk		90	MHz
etxclk		90	MHz
minimum reset time	50		ns

NOTE: timing model "worst" case is used.

10.0 Device Pinout

10.1 Signals Overview

Table 11: Signals Overview Table

Signals	Description
wrxclk, wrxclav, wrxenb*, wrxdat, wrxsoc	West Utopia Receive Interface.
wtxclk, wtxclav, wtxenb*, wtxdata, wtxsoc	West Utopia Transmit Interface.
wrx_err, wrx_err_stat	West Interface error indication (sampled with wrxclk).
erxclk, erxclav, erxenb*, erxdata, erxsoc	East Utopia Receive Interface.
etxclk, etxclav, etxenb*, etxdata, etxsoc	East Utopia Transmit Interface.
erx_err, erx_err_stat	East Interface error indication (sampled with wtxclk).
prty_en, cellsize	Configuration Pins to be board wired. Cellsize [0] should be tied to GND.
reset	Active high device reset
GND	Ground
VCC	Device Power 2.5 V
clk(x)	unused clock inputs should be tied to GND
IOCTRL(x)	
VCCIO(x)	IO Power 3.3 V
INREF(x)	connect to GND
PLL_RST(x)	connect to GND or VCC
PLLOUT(x)	connect to GND or VCC
VCCPLL(x)	
GNDPLL(x)	
TCK, TRSTB	JTAG signals. connect to GND
TMS, TDI	JTAG signals. connect to VCC
TDO	JTAG signal. leave open
iov	
nc	not connected. should be left open

*: active low signal

NOTE: Unused Pins (data busses) in the following tables are to be handled like "nc".

10.2 PT280 FPBGA Device Diagram

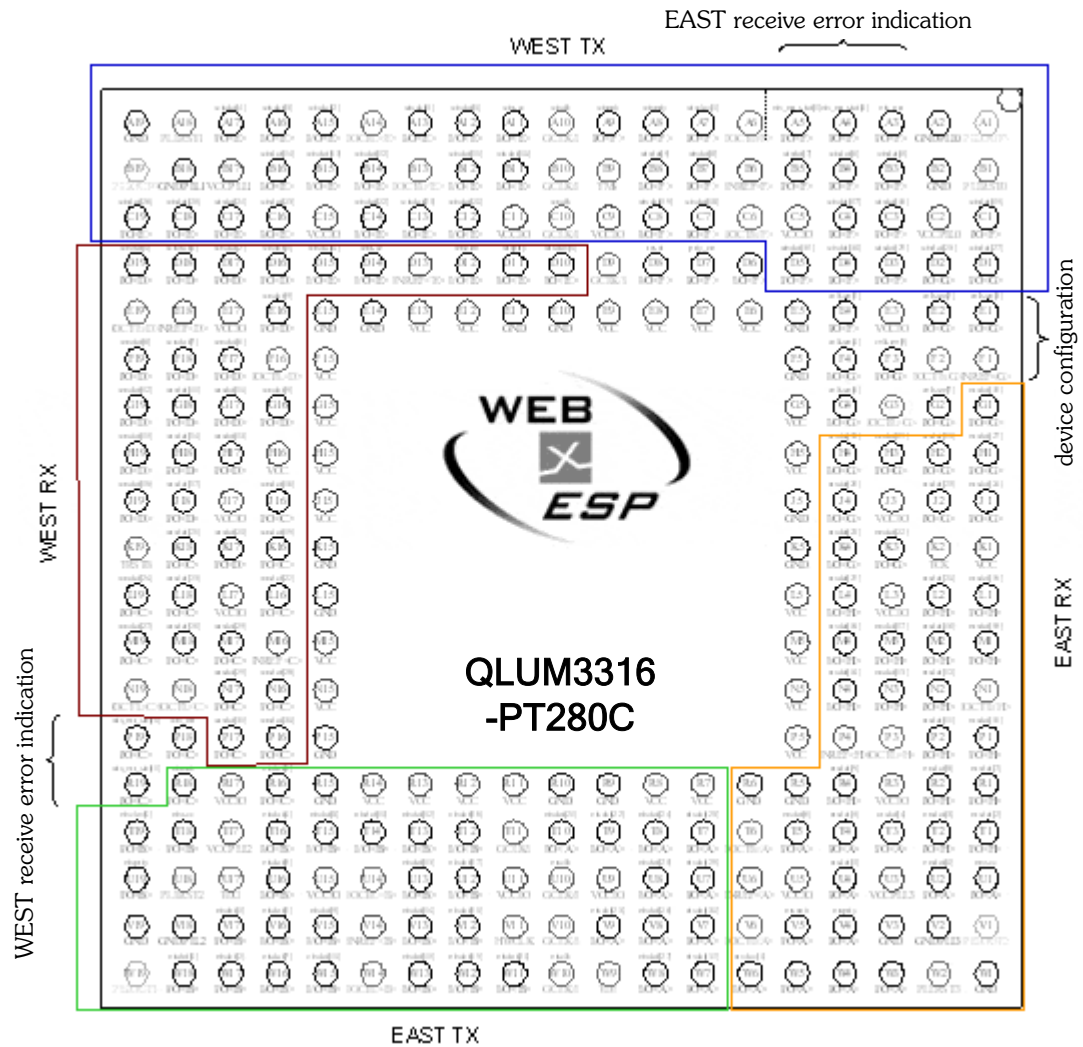


Figure 13: PT280 bottom view (0.8mm FPBGA)

10.3 PT280 FPBGA Pinout Table

Table 12: PT280 FPBGA Pinout Table

PIN	Function	PIN	Function	PIN	Function	PIN	Function	PIN	Function
A1	pllout(3)	D1	N/C	G19	wtxd[12]	N16	N/C	U6	inref(a)
A2	gndpll(0)	D2	N/C	H1	N/C	N17	N/C	U6	N/C
A3	erx_err	D3	N/C	H2	N/C	N18	ioctrl(c)	U8	N/C
A4	erx_err_stat[0]	D4	N/C	H3	N/C	N19	ioctrl(c)	U9	vccio(a)
A5	erx_err_stat[1]	D5	N/C	H4	N/C	P1	wtxd[10]	U10	erxclk
A6	ioctrl(f)	D6	nc (cellsize[0])	H5	vcc	P2	wtxd[11]	U11	vccio(b)
A7	wtxc[0]	D7	prty_en	H15	vcc	P3	ioctrl(h)	U12	N/C
A8	wtxp[0]	D8	reset	H16	vcc	P4	inref(h)	U13	etxd[13]
A9	wtxc	D9	clk(8)	H17	wtxd[13]	P5	vcc	U14	ioctrl(b)
A10	wtxc	D10	wrx[0]	H18	wtxd[14]	P15	gnd	U15	vccio(b)
A11	wtxsoc	D11	wrxp[0]	H19	wtxd[15]	P16	N/C	U16	etxd[5]
A12	wtxd[0]	D12	wrxnb	J1	N/C	P17	N/C	U17	tdo
A13	wtxd[1]	D13	inref(e)	J2	N/C	P18	wrx_err	U18	pll[2]
A14	ioctrl(e)	D14	wrxsoc	J3	vccio(g)	P19	wrx_err_stat[0]	U19	etxp[0]
A15	wtxd[2]	D15	wrx[0]	J4	N/C	R1	erxd[7]	V1	pllout(2)
A16	wtxd[3]	D16	wrx[1]	J5	gnd	R2	erxd[8]	V2	gndpll(3)
A17	wtxd[4]	D17	wrx[2]	J15	vcc	R3	vccio(h)	V3	gnd
A18	pll[1]	D18	wrx[3]	J16	N/C	R4	etxd[9]	V4	erxp[0]
A19	gnd	D19	wrx[4]	J17	vccio(d)	R5	gnd	V5	erxnb
B1	pll[0]	E1	cellsize[3]	J18	N/C	R6	gnd	V6	ioctrl(a)
B2	gnd	E2	cellsize[2]	J19	N/C	R7	vcc	V7	N/C
B3	wtxd[5]	E3	vccio(g)	K1	vcc	R8	vcc	V8	N/C
B4	wtxd[6]	E4	cellsize[1]	K2	tck	R9	gnd	V9	N/C
B5	wtxd[7]	E5	gnd	K3	N/C	R10	gnd	V10	clk(1)
B6	inref(f)	E6	vcc	K4	N/C	R11	vcc	V11	clk(4)
B7	wtxd[8]	E7	vcc	K5	gnd	R12	vcc	V12	N/C
B8	wtxd[9]	E8	vcc	K15	gnd	R13	vcc	V13	etxd[14]
B9	tms	E9	vcc	K16	N/C	R14	vcc	V14	inref(b)
B10	clk(6)	E10	gnd	K17	N/C	R15	gnd	V15	etxd[9]
B11	wtxd[10]	E11	gnd	K18	N/C	R16	etxd[3]	V16	etxd[6]
B12	wtxd[11]	E12	vcc	K19	trstb	R17	vccio(c)	V17	etxd[1]
B13	ioctrl(e)	E13	vcc	L1	N/C	R18	etxnb	V18	gndpll(2)
B14	wtxd[12]	E14	gnd	L2	N/C	R19	wrx_err_stat[1]	V19	gnd
B15	wtxd[13]	E15	gnd	L3	vccio(h)	T1	erxd[2]	W1	gnd
B16	wtxd[14]	E16	wrx[5]	L4	N/C	T2	erxd[3]	W2	pll[3]
B17	vccpll(1)	E17	vccio(d)	L5	vcc	T3	erxd[4]	W3	nc
B18	gndpll(1)	E18	inref(d)	L15	gnd	T4	erxd[5]	W4	nc
B19	pllout(0)	E19	ioctrl(d)	L16	N/C	T5	erxd[6]	W5	nc
C1	wtxd[15]	F1	inref(g)	L17	vccio(c)	T6	ioctrl(a)	W6	erxc[0]
C2	vccpll(0)	F2	ioctrl(g)	L18	N/C	T7	N/C	W7	etxd[31]
C3	N/C	F3	cellsize[5]	L19	N/C	T8	N/C	W8	N/C
C4	N/C	F4	cellsize[4]	M1	N/C	T9	N/C	W9	tdi
C5	vccio(f)	F5	gnd	M2	N/C	T10	N/C	W10	etxclk
C6	ioctrl(f)	F15	vcc	M3	N/C	T11	clk(3)	W11	N/C
C7	N/C	F16	ioctrl(d)	M4	N/C	T12	N/C	W12	N/C
C8	N/C	F17	wrx[6]	M5	vcc	T13	etxd[12]	W13	etxd[15]
C9	vccio(f)	F18	wrx[7]	M15	vcc	T14	etxd[13]	W14	ioctrl(b)
C10	wrxclk	F19	wrx[8]	M16	inref(c)	T15	etxd[8]	W15	etxd[10]
C11	vccio(e)	G1	N/C	M17	N/C	T16	etxd[4]	W16	etxd[7]
C12	N/C	G2	cellsize[7]	M18	N/C	T17	vccpll(2)	W17	etxd[2]
C13	N/C	G3	ioctrl(g)	M19	N/C	T18	etxsoc	W18	etxd[0]
C14	N/C	G4	cellsize[6]	N1	ioctrl(h)	T19	etxc[0]	W19	pllout(1)
C15	vccio(e)	G5	vcc	N2	wtxd[12]	U1	erxsoc		
C16	N/C	G15	vcc	N3	wtxd[13]	U2	erxd[0]		
C17	N/C	G16	wtxd[9]	N4	wtxd[14]	U3	vccpll(3)		
C18	N/C	G17	wtxd[10]	N5	vcc	U4	erxd[1]		
C19	N/C	G18	wtxd[11]	N15	vcc	U5	vccio(a)		

11.0 References

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12.0 Contact

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