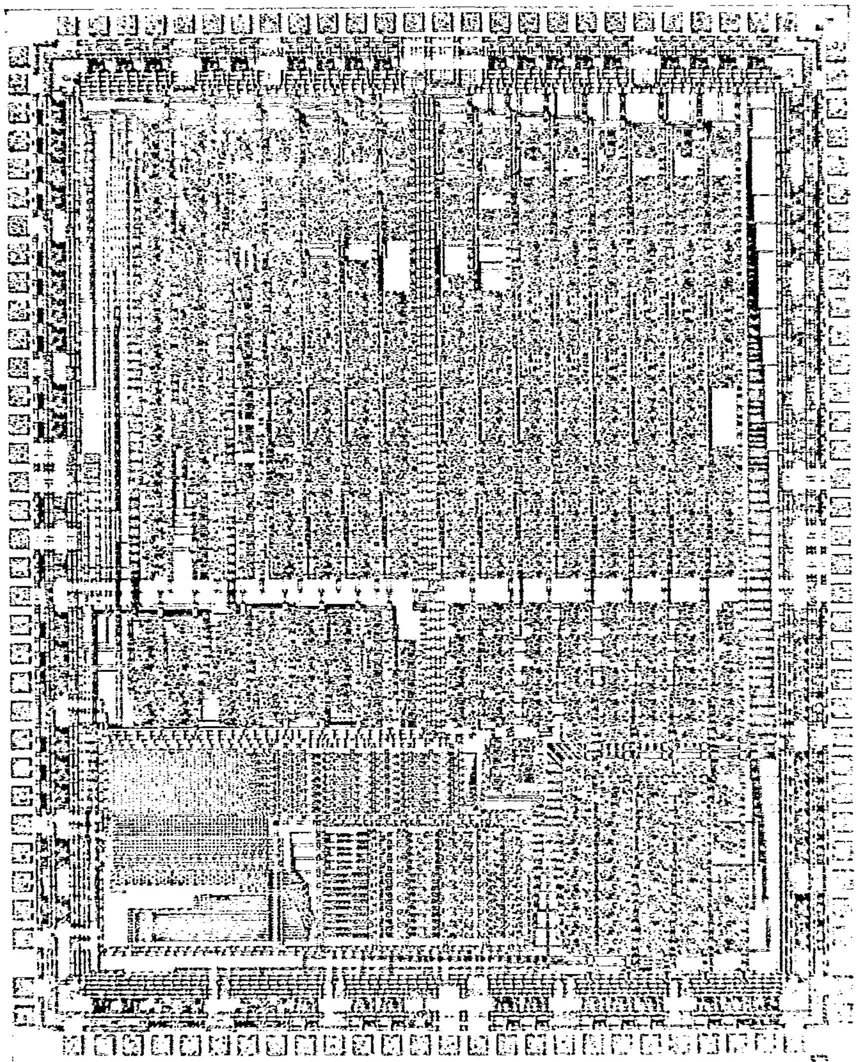
T-42-41

# QLSI™ Standard Cells

- Supports LSI solutions from 100MHz to beyond 2GHz
- Directly interfaces to ECL, TTL and CMOS based systems
- Mixed analog & digital circuitry
- Integrated ROM cells
- Commercial & military temperature ranges
- MIL-STD-883C screening
  Class B package
  Class S die
- Supported on Mentor Graphics and Dazix workstations
- Turn-key design options available



**QLSI Standard Cell design integrating 2K-Bits of ROM and 3000 equivalent gates with operation to 1GHz.**

**Design examples for use with TriQuint MLC packages**

| | | | | | |
|---|---|---|---|---|---|
| Equiv. Gates | 375 | 1000 | 2000 | 4500 | 10000 |
| Unit Cells | 75 | 200 | 400 | 900 | 2000 |
| # of D Flip-flops | 35 | 100 | 200 | 450 | 1000 |
| # of I/O Cells | 24 | 40 | 64 | 84 | 128 |
| MLC Package | MLC44 | MLC68 | MLC132/64 | MLC132/84 | MLC196 |

## APPLICATIONS:

- High speed logic
- Digital signal processing
- Crosspoint switch matrix
- Direct digital synthesis (DDS)
- Fiber-optic telecommunications
- CPU and high speed graphics

TriQuint® SEMICONDUCTOR

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# Product Description

Ideally suited for designs requiring high speed/density, low power and direct interface to ECL, TTL and CMOS circuitry, QLSI standard cells offer designers state-of-the-art capability in digital/linear ASICs. QLSI standard cells were developed to offer designers the high performance and low power capabilities of GaAs though the use of logic function macros. The fully characterized logic functions eliminate the intricate and time consuming tasks associated with custom IC design. Complete workstation design support in conjunction with design consultation reduces the time and effort required to turn a design into reality.

QLSI standard cells are based upon a fully differential logic structure called Source Coupled FET Logic (SCFL). SCFL offers exceptional functional performance and flexibility, high fanout and low power dissipation. Five speed/power versions are available to tailor designs for optimum speed with minimum power dissipation. Fully compatible ECL, TTL and CMOS I/Os eliminate the system level problems associated with non-standard interface levels.

The QLSI standard cells are manufactured using TriQuint's proven QED enhancement/depletion Gallium Arsenide (GaAs) process and are backed by extensive quality and reliability programs.

| Cell Function | Name* |
|---|---|
| Inverter/Buffer | SX10 |
| 2-Input OR/NOR | SX20 |
| 3-Input OR/NOR | SX30 |
| 4-Input OR/NOR | SX40 |
| 5-Input OR/NOR | SX50 |
| 6-Input OR/NOR | SX60 |
| 2-Input Exclusive OR/NOR | SX2XOR |
| 3-Input Exclusive OR/NOR | SX3XOR |
| 2-Input AND/NAND | SX01 |
| 3-Input AND/NAND | SX3AND |
| 1 AND, 1 OR/INVERT | SX11 |
| 1 by 2-Input O/A/I | SXOA12 |
| 2-Input Multiplexer | SX2MUX |
| 4-Input Multiplexer | SX4MUX |
| 8-Input Multiplexer | SX8MUX |
| 2-Bit Accumulator | SXACC_2 |
| Carry Generate | SXCG |
| ROM | |
| R S Latch | SXRSL |
| Master Latch | SXDDML |
| Master Latch w/ Reset | SXDDMLR |
| Master Latch w/ Set | SXDDMLS |
| Master/Slave Flip-flop | SXDDFF |
| Master/Slave Flip-flop w/ Reset | SXDDFFR |
| Master/Slave Flip-flop w/ Set | SXDDFFS |
| Master/Slave Flip-flopReset/Set | SXDDFFRS |
| Master/Slave Flip-flop w/2:1 Mux | SXMDDFF |
| TTL Input | IMTS1 |
| CMOS Input | IMCS1 |
| TTL/CMOS Output | OXSC1 |
| Tri-State TTL/CMOS Output | OXSCZ |
| ECL Input (Single-ended) | IXES1 |
| (Differential) | IXES2 |
| ECL Output (Single-ended) | OXSE1 |
| (Differential) | OXSE2 |
| AC-Coupled RF Input | IMRF1 |

* X=F,M,S,L or T depending on the power family

# Macro Functions

## Digital Macro Library

- ❑ Fully characterized over process and temperature
- ❑ Custom cells and macros built to customer requirements.

## Linear Functional Blocks

- ❑ Integrated analog (linear) and digital functions
- ❑ Analog functions tailored to customer specifications

Linear Functional Blocks have been designed to integrate with the digital macro functions. The functional block's basic operation has been characterized and initial layout completed. TriQuint engineers will work with each customer to tailor each functional block to meet the design specifications. TriQuint will perform all design modification and layout tasks. Contact factory for complete details.

**Amplifiers:**

| | |
|---|---|
| Bias Amplifier | AA01 |
| Operational Amplifier | AA02 |
| High Speed Buffer | AA03 |

**Laser Drivers:**

| | |
|---|---|
| Single Stage | LD001 |
| Multi-Stage | LD002 |
| Multi-Stage w/ Output control | LD003 |

**Transimpedance Amplifiers:**

| | |
|---|---|
| Single Supply (+5V) | |
| Single Stage | TA01-1,2 |
| Multi-stage | TA01-3 |
| Dual Supply (+/-5V) | |
| Single Stage | TA02-1,2 |
| Multi-stage | TA02-3 |

**Additional Functions:**

Comparators
Digital to Analog Converters
Analog to Digital Converters
Voltage Controlled Oscillators

# DC Electrical Specifications

## Absolute Maximum Ratings

| SYMBOL | CHARACTERISTICS | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply | | 0 | | +7 | V |
| $V_{EE}$ | Negative Supply | | -7 | | 0 | V |
| $T_O$ | Operating Temperature | Junction | -55 | | +150 | °C |
| $T_S$ | Storage Temperature | | -65 | | +175 | °C |

## Recommeded Operating Conditions

| SYMBOL | CHARACTERISTICS | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$* | Positive Supply | | +4.5 | | +5.5 | V |
| $V_{EE}$** | Negative Supply | | -5.5 | | -4.5 | V |

$T_{case}$=-55°C to 125°C unless otherwise specified
* Not required if TTL or CMOS outputs are not used
** Not required if inverted ECL I/O are used

## ECL Inputs & Outputs

| SYMBOL | CHARACTERISTICS | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HI Voltage | | -1100 | | 0 | mV |
| $V_{IL}$ | Input LO Voltage | | $V_{TT}$ | | -1500 | mV |
| $I_{IL}$ | Input HI Current | $V_{IH}^{max}$ | | | +10 | µA |
| $I_{IL}$ | Input LO Current | $V_{IL}^{min}$ | | | -10 | µA |
| $V_{OH}$ | Output HI Voltage | Note 1 | -1000 | | -500 | mV |
| $V_{OL}$ | Output LO Voltage | Note 1 | $V_{TT}$ | | -1600 | mV |
| $I_{OH}$ | Output HI Current | Note 2 | 20 | 23 | 30 | mA |
| $I_{OL}$ | Output LO Current | Note 2 | 0 | 5 | 8 | mA |
| $V_{ref}$ | Internal ECL Ref. | | | -1300 | | mV |

Note 1: $R_{load}$ = 50 Ohm to $V_{TT}$ = -2.0V
Note 2: Not tested, consistent with $V_{OH}$ and $V_{OL}$ tests

## TTL Inputs & Outputs

| SYMBOL | CHARACTERISTICS | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HI Voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LO Voltage | | 0 | | 0.8 | V |
| $I_{IH}$ | Input HI Current | $V_{IH}^{max}$ | | | +100 | µA |
| $I_{IL}$ | Input LO Current | $V_{IL}^{min}$ | -100 | | | µA |
| $V_{OH}$ | Output HI Voltage | $I_{OH}$= 3mA | 2.4 | | $V_{CC}$ | V |
| $V_{OL}$ | Output LO Voltage | $I_{OL}$= -3mA | 0 | | 0.4 | V |

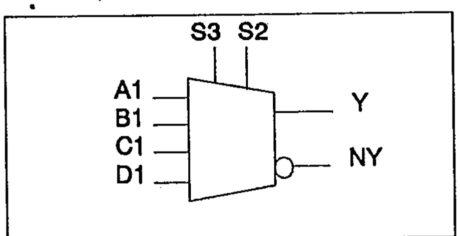
## CMOS Inputs & Outputs

| SYMBOL | CHARACTERISTICS | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIH | Input HI Voltage | | 3.5 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LO Voltage | | 0 | | 1.5 | V |
| $I_{IH}$ | Input HI Current | $V_{IH}^{max}$ | | | +100 | µA |
| $I_{IL}$ | Input LO Current | $V_{IL}^{min}$ | -100 | | | µA |
| $V_{OH}$ | Output HI Voltage | $I_{OH}$= 3mA | 4.2 | | $V_{CC}$ | V |
| $V_{OL}$ | Output LO Voltage | $I_{OL}$= -3mA | 0 | | 0.8 | V |

# AC Electrical Specifications

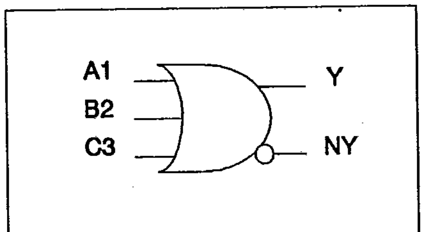
- Symmetrical rise & fall delays
- Characterized over the full military temperature range
- Multiple speed/power options

4:1 Multiplexer (SX4MUX)



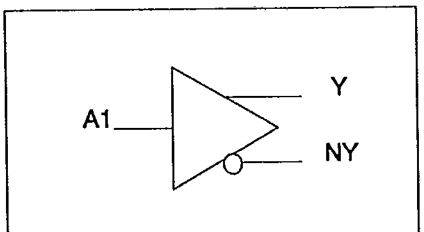

| Cell Characteristics | | | | | |
|---|---|---|---|---|---|
| Family Name | Node | Base Delay (ps) | Loading (ps/fF) | Cin (fF) | Power (mW) |
| SM4MUX | A1-D1 | 88 | 0.45 | 35 | 8 |
| | S2 | 168 | | | |
| | S3 | 228 | | | |
| SS4MUX | A1-D1 | 120 | 1.15 | 18 | 4 |
| | S2 | 205 | | | |
| | S3 | 270 | | | |
| SL4MUX | A1-D1 | 115 | 2.03 | 17 | 2 |
| | S2 | 205 | | | |
| | S3 | 275 | | | |

3-Input OR/NOR (SX30)



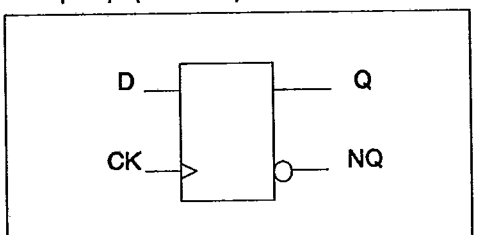

| Cell Characteristics | | | | | |
|---|---|---|---|---|---|
| Family Name | Node | Base Delay (ps) | Loading (ps/fF) | Cin (fF) | Power (mW) |
| SM10 | A1 | 83 | 0.45 | 35 | 8 |
| | B2 | 123 | | | |
| | C3 | 163 | | | |
| SS10 | A1 | 115 | 1.15 | 18 | 4 |
| | B2 | 160 | | | |
| | C3 | 205 | | | |
| SL10 | A1 | 110 | 2.03 | 17 | 2 |
| | B2 | 160 | | | |
| | C3 | 210 | | | |

Inverter/Buffer (SX10)




| Cell Characteristics | | | | | |
|---|---|---|---|---|---|
| Family Name | Node | Base Delay (ps) | Loading (ps/fF) | Cin (fF) | Power (mW) |
| SF10 | A1 | 65 | 0.15 | 105 | 24 |
| SM10 | A1 | 73 | 0.45 | 35 | 8 |
| SS10 | A1 | 105 | 1.15 | 18 | 4 |
| SL10 | A1 | 100 | 2.03 | 17 | 2 |

D Flip-flop (SXDDFF)




| Cell Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| Family Name | Base Delay (ps) | | | Loading (ps/fF) | Cin (fF) D/CK | Power (mW) |
| | CK->Q | Setup | Hold | | | |
| SMDDFF | 154 | 94 | 50 | 0.45 | 35/70 | 16 |
| SSDDFF | 196 | 131 | 50 | 0.45 | 35/70 | 8 |
| SLDDFF | 210 | 140 | 50 | 0.45 | 35/70 | 4 |

Base delays are nominal unloaded value @ $T_j$=25°C

Typical interconnect (metal) capacitance = 25fF/Fanout

Interconnect load : (Cin+ Metal C) * loading(ps/fF)

Worst case delay derating (includes process, temperature and power supply):
commercial - 1.5 x nominal, military - 1.7 x nominal

# Process Technology

## QED GaAs Process

- High performance enhancement/depletion MESFET process
- Highly reliable gold based process
- 12 mask layers simplifies manufacturing
- Very low capacitance air dielectric interconnect metal
- Gold interconnect metal eliminates metal migration, reduces IR drop improving noise margin and interconnect delays

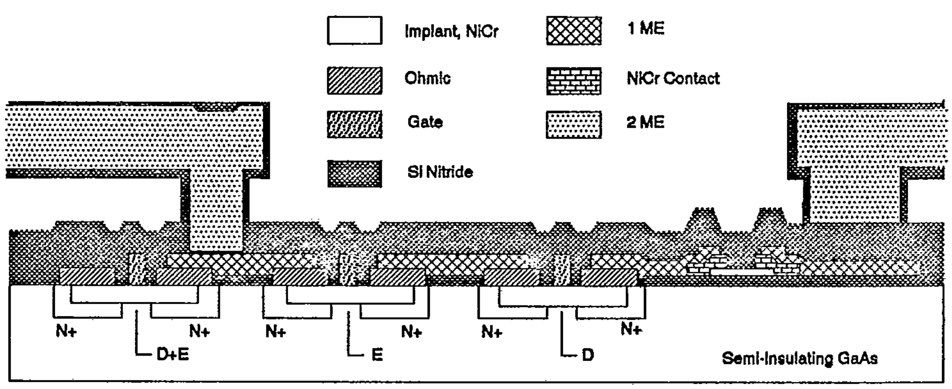
TriQuint's philosophy has always been to provide the highest level of performance possible based upon a solid high volume manufacturing process. QLSI standard cells are manufactured on 4 inch wafers using TriQuint's QED 1 micron MESFET enhancement / depletion process. The QED process has been commercially available since 1986.

The QED process offers both the normally-off enhancement and the normally-on depletion mode MESFETs. The addition of the enhancement mode MESFET eliminates the need for multiple power supplies and reduces the devices' power dissipation. A QED process option (QED/A) offers Metal-Insulator-Metal (MIM) capacitors, spiral inductors and precision nichrome resistors (TCR ≈ 0 ) necessary for many analog functions.

All of TriQuint's processes are based upon proven high performance gold interconnect technology. Gold interconnect technology is used by high performance silicon bipolar and GaAs manufacturers in place of alternatives such as aluminum. In addition to alleviating the various electro-migration and corrosion characteristics of aluminum, gold's higher conductivity reduces the noise on ground lines, improving the noise margins critical in LSI designs.

Interconnect capacitance is the major performance limiting factor in high speed designs. TriQuint uses an airbridge technique for routing the second layer of interconnect metal. Airbridge technology has been used for many years to reduce the capacitance by using air as the dielectric. Air dielectric reduces the interconnect capacitance by approximately one half to one third as compared to standard "landed" interconnect. TriQuint's airbridges have been extensively tested for reliability and exceed all military requirements.

*QED/A Enhancement/Depletion Process*

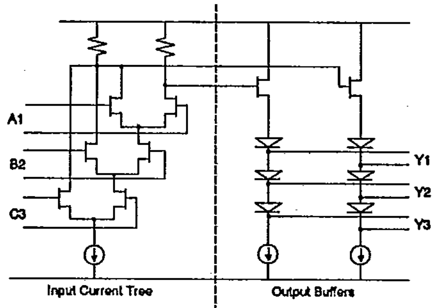


# Architecture

## Source Coupled FET Logic

- Fully differential complementary logic
- Symmetrical rise & fall delays
- Macro characterization over -55°C to +125°C temperature range

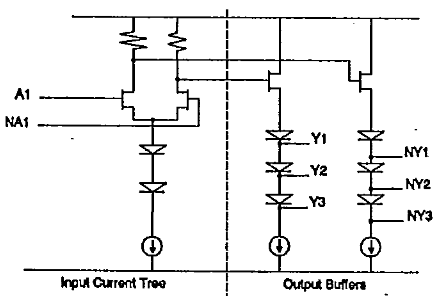
In development of a high performance LSI ASIC product, design issues such as logic complexity, noise margin, signal symmetry, skew, and system power were considered. TriQuint designed the QLSI standard cells based upon a fully differential design known as Source Coupled FET Logic (SCFL).



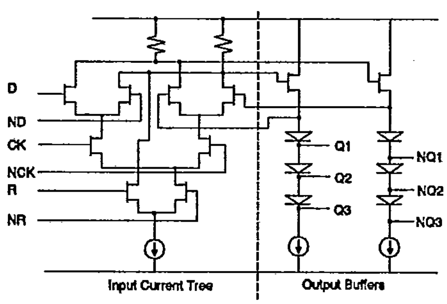

Simplified SCFL schematic

SCFL implements logic functions in a manner similiar to silicon ECL utilizing differential amplifiers to implement the desired logic functions. As shown in the above figure, the basic SCFL "cell" consists of the input logic tree and two output buffers. The fully differential design of SCFL eliminates the on-board reference generators used in silicon ECL designs. The 5 volt power supply specification allows up to 3 levels of current steering differential amplifier pairs to implement the logic functions.

Utilizing all 3 levels of logic steering, functions ranging from inverter/buffers to master latches w/set or reset and fully decoded 4:1 multiplexers can be constructed from a single cell. This basic SCFL "cell" based design approach offers designers increased logic function density and performance compared to conventional single-ended "NOR gate" based designs such as Direct Coupled FET Logic (DCFL).




*Inverter/Buffer*




*Master Latch w/Reset*

# Architecture (cont.)

## Source Coupled FET Logic

- Excellent noise margin
- Symmetrical rise and fall for minimum signal distortion
- Multiple speed/power versions offer design optimization

The differential structure of SCFL inherently provides both the true and complement logic outputs. For example, a design may implement both the NOR and OR logic operation on a single set of inputs. The ability to use the true and complement outputs of a function can greatly reduce the number of devices required in a design.

Noise margin is a major concern in high performance LSI designs utilizing a large number of gates and consequently FETs. Worst case design analysis must deal with variations in process (FET pinch-off $V_P$) and voltage distribution across the die (IR drop) and changes in device characteristics with temperature. Logic designs implemented using other common single-ended topologies such as Direct Coupled FET Logic (DCFL) have low noise margins (100-200mV). Variations in device $V_P$ in conjuction with supply voltage variations (IR) can reduce an individual gate's noise margin to zero or less using DCFL. In comparision, TriQuint's SCFL has an equivalent noise margin of approximately 400mV and operates in a common-mode arrangement reducing the effects of process, temperature and supply variations.

Signal symmetry is another characteristic critical to many applications. As a signal propagates through even a single gate, the signal symmetry will change if the gates have asymmetrical rising and falling delays. Fully differential logic eliminates the asymmetrical delays by using the crossing of both the true and complement signal to determine the reference for state transition.

Signal skew is affected by the delay introduced due to the interconnect metal RC value. With large designs the ability to match the interconnect metal length of critical signals becomes almost impossible. By reducing the interconnect metal's contribution to delay the matching of critical paths is improved. TriQuint's Gold interconnect metal's high conductivity in conjunction with the airbridge's very low capacitance minimizes the interconnect metal delay.

System power requirements are often a factor in ASIC designs. Lower power dissipation reduces the system supply requirements, simplifies the thermal management task, and improves the device reliability and lifetime. The majority of designs have a mixture of critical high speed or high load driving logic mixed with lower speed or lower load driving logic. To maximize performance and minimize device power, five (5) speed/power families are available in the QLSI library. Each macro cell is available in 1mW, 2mW, 4mW and 8mW versions, with selected macros available in a 24mW version for driving very high speed or high load signals.

# ASIC Design Support

TriQuint offers complete ASIC development support services. Customers can select development options including Turn-key (TriQuint designs to specifications), Semicustom (Customer designs logic, TriQuint performs layout) and Full Custom (Customer licenses QLSI cells and are responsible for design and layout). The majority of ASIC designs are developed using the semicustom methodology.

TriQuint's semicustom development support includes a complete set of workstation software tools and documentation providing a simple yet complete design environment.

Workstation support is provided for Dazix and Mentor Graphics platforms. Design support includes schematic models, timing models, net loading program providing pre and post-layout capacitance values, electrical rule checking and design submission programs.

Training is available to review the workstation design tools and become familiar with designing with the high performance capabilities of GaAs. Customer training is available either at TriQuint or at the customer site. Additionally, TriQuint offers a week long training class for customers interested in learning the specific details necessary for the full custom development option.

### Semicustom DevelopmentOption

**Customer Tasks**

- Develop circuit specifications
- Logic design & schematic capture
- Test vector generation
- Execute statistical load capacitance program
- Functional & timing simulations
- Execute electrical rule check program
- Submit design to TriQuint
- Re-simulate design using back annotated layout capacitance
- Final design sign-off
- Evaluate delivered prototypes

**TriQuint Tasks**

- Review initial specifications
- QLSI product & software training
- Provide consultation during design phases
- Review design & simulations following submission
- Place & route design to meet design specifications
- Supply layout capacitance back annotation file
- Execute DRC & LVS on final layout
- Fabricate masks & wafers
- Package & test prototype parts
- Ship prototype parts

## Development Options

- ❑ Semicustom
- ❑ Turn-key custom
- ❑ Full custom (QLSI cell license)

## Workstation Software

- ❑ Mentor Graphics
- ❑ Dazix

## Support Services

- ❑ Product & software training
- ❑ Design reviews
- ❑ Design consultation

# High Speed Packaging

## Standard Packages

- 44 to 196 pins
- Controlled impedance signals pins/paths
- Signals > 3GHz

## Engineering Test Fixtures

- Solderless, controlled electrical environment
- Rapid prototype evaluation

## Custom Packages

- Low cost, rapid prototyping
- Single and multiple chip carriers

Performance advances in digital logic ASICs have resulted in a re-evaluation of standard dual in-line and pin-grid array packages. As the signal speeds push beyond 50-100MHz, the relatively large lead inductance and uncontrolled signal impedance begin to adversly affect the signal quality and consequently the system performance. System designers must deal with the package as an integral part of the circuit operation.

TriQuint acknowledged the need for new package technology, developing and manufacturing a complete line of high performance packages. TriQuint's packages are constructed using a Multi-Layer Ceramic (MLC) process providing separate power and ground planes, on-board decoupling capacitors and controlled impedance signal paths.

Standard packages are available with 24, 40, 64, 84 and 128 high speed signals. The packages are designed with 50 Ohm signal path impedance capable of handling signals greater than 3GHz and edge rates less than 125ps. The packages are designed for cavity down surface mounting.

| STANDARD PACKAGES | | | | | |
|---|---|---|---|---|---|
| MLC | 44/24 | 68/40 | 132/64 | 132/84 | 196/128 |
| Package pins | 44 | 68 | 132 | 132 | 196 |
| Signal pins | 24 | 40 | 64 | 84 | 128 |
| Lead pitch (mils) | 50 | 50 | 25 | 25 | 25 |
| Size (in sq.) | 0.650 | 0.950 | 0.950 | 0.950 | 1.350 |
| Maximum die size (mils) | 80 | 120 | 160 | 210 | 380 |

For each standard package offered by TriQuint, a solderless high speed test fixture is available. The Engineering Test Fixtures (ETF) are designed to provide a controlled evaluation environment including 50 Ohm signal lines with SMA connectors, power and ground planes, signal termination and a chip socket for quick mounting.

Many applications have unique requirements not addressed by standard packaging. TriQuint's complete custom package design and manufacturing capability offers customers quick and cost effective solutions. TriQuint's MLC manufacturing process utilizes programmable (soft) tooling for rapid prototyping with low development costs. The soft tooling is ideal for low to medium production volumes (<10,000 parts/year). For higher volume applications, custom package designs can be transferred to high volume package manufacturers.

## Testing

- Process control monitor structures for wafer fabrication testing
- DC and AC functional testing for die and packaged parts

Product testing is performed throughout the manufacturing process. Wafer fabrication is monitored at numerous stages using Process Control Monitor (PCM) structures. PCM testing allows TriQuint to monitor the fabrication process ensuring finished wafers will meet TriQuint's specifications. Completed wafers passing the PCM tests are die probed for DC parametrics and logic functionality using the simulation test vectors.

Functionally good die are packaged if required and again tested for DC parametric and AC functionality using the simulation test vectors. High speed AC testing, if required, is available using a Tektronix LT1001 (up to 200MHz) or custom test fixtures if required.

## Reliability & Quality Assurance

- Acknowledged industry leader in reliability
- Mil-spec compliant
- TQM commitment

TriQuint's reliability and quality assurance programs are based upon detailed element testing. Each element (FET, resistors, interconnect metal, etc.) is stressed and tested until failure to better understand the various mechanisms associated with component failure. Element testing is more costly and time consuming than ordinary life testing, but provides TriQuint with the ability to determine actual failure mechanisms and under what conditions failures occur. This critical information enables TriQuint to continually make process improvements for greater reliability. TriQuint has presented many award winning papers on gallium arsenide reliability which are available upon request.

TriQuint's quality assurance program is integral to every phase of product development and manufacture. The program is based on a philosophy of Total Quality Management (TQM) and compliance with the applicable US military standard for IC manufacturing. TriQuint is currently approved to MIL-I-45208 and will be compliant with MIL-Q-9858 and ISO-9001 in 1990.

## Military Support

- MIL-STD-883C
  Class B packaged parts
  Class S die
- Lot qualification
  Method 5005 groups A,B,C,D
- MIL-I-45208 approved
- MIL-Q-9858 scheduled 1990
- MIL-M-38510 appendix A
  scheduled 1991

Product screening and qualification to military standards is offered with QLSI standard cells. TriQuint's military support is based upon MIL-M-38510 requirements and offers screening to MIL-STD-883C Class S and Class B requirements. TriQuint also offers lot qualification for both die and packaged product.

A small number of exceptions are typically required to account for physical and electrical differences between silicon and gallium arsenide. TriQuint works with each customer to ensure all program requirements are addressed using Source Control Drawings (SCD).

TriQuint's Quality Assurance staff participates on a regular basis with the Rome Air Development Center (RADC) and the Defense Electronics Supply Command (DESC) on JEDEC Committee JC13 Task Forces to incorporate requirements for gallium arsenide ICs into MIL-STD-883, MIL-M-38510 and other military specifications.