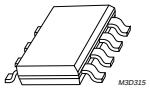


# PHK13N03LT

TrenchMOS™ logic level FET

**Rev. 01 — 23 June 2003** **Product data**

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHK13N03LT in SOT96-1 (SO8).

### 1.2 Features

- Low gate charge
- Low on-state resistance
- Surface mount package
- Fast switching.

### 1.3 Applications

- Portable appliances
- Lithium-ion battery chargers
- Notebook computers
- DC-to-DC converters.

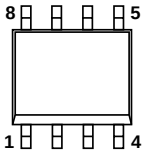
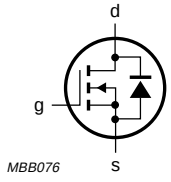
### 1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $P_{tot} \leq 6.25$ W
- $I_D \leq 13.8$ A
- $R_{DSon} \leq 20$ mΩ



## 2. Pinning information

**Table 1: Pinning - SOT96-1 (SO8), simplified outline and symbol**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1,2,3 | source (s) |  |  |
| 4 | gate (g) | | |
| 5,6,7,8 | drain (d) | | |



**SOT96-1 (SO8)**

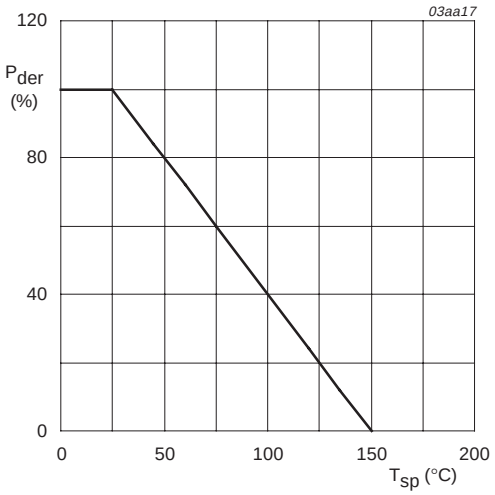
PHILIPS

## 3. Limiting values

**Table 2: Limiting values**

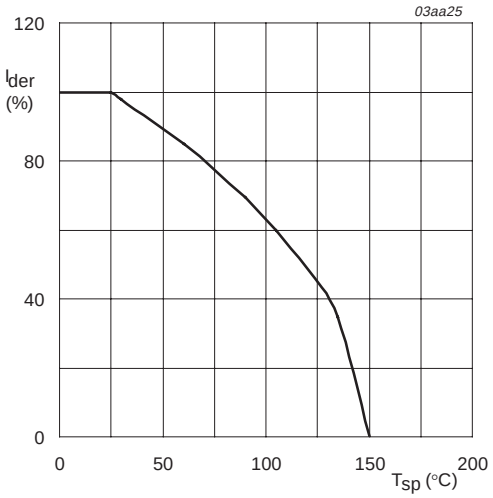
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C | - | 30 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | - | 30 | V |
| $V_{GS}$ | gate-source voltage (DC) | | - | ±20 | V |
| $I_D$ | drain current (DC) | $T_{sp}$ = 25 °C; $V_{GS}$ = 10 V; Figure 2 and 3 | - | 13.8 | A |
| | | $T_{sp}$ = 100 °C; $V_{GS}$ = 10 V; Figure 2 | - | 8.7 | A |
| $I_{DM}$ | peak drain current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; Figure 3 | - | 55 | A |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C; Figure 1 | - | 6.25 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –55 | +150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source (diode forward) current (DC) | $T_{sp}$ = 25 °C | - | 5.7 | A |
| $I_{SM}$ | peak source (diode forward) current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs | - | 55 | A |




$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

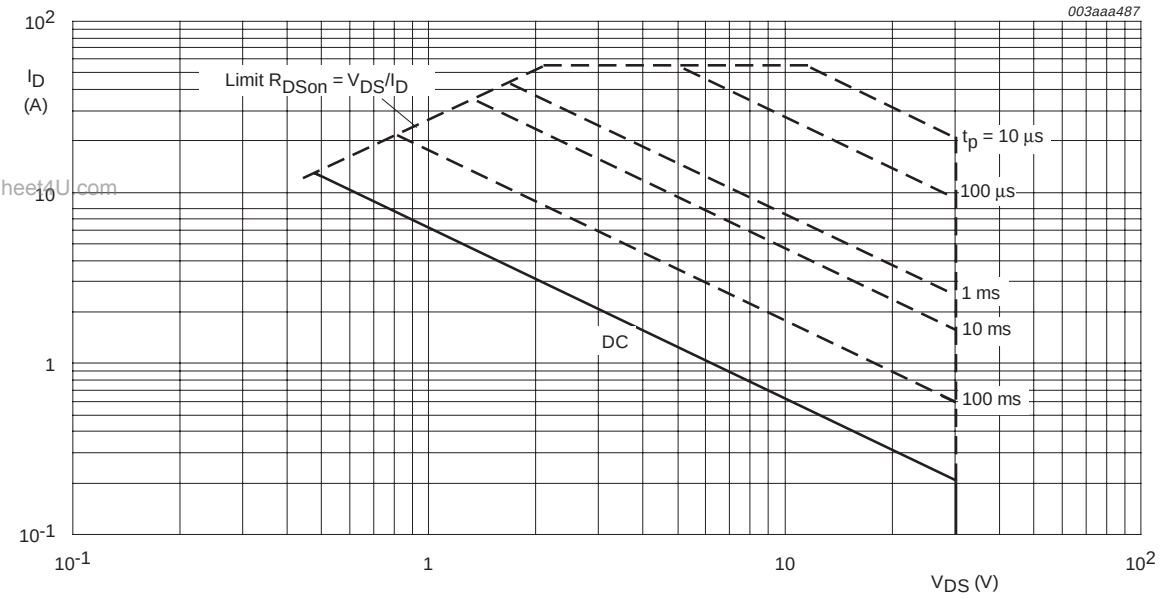
**Fig 1. Normalized total power dissipation as a function of solder point temperature.**




$V_{GS} \geq 5$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of solder point temperature.**






$T_{sp}$ = 25 °C; $I_{DM}$ is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

# 4. Thermal characteristics

**Table 3: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | Figure 4 | - | - | 20 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint; mounted on a printed-circuit board | - | 70 | - | K/W |

## 4.1 Transient thermal impedance

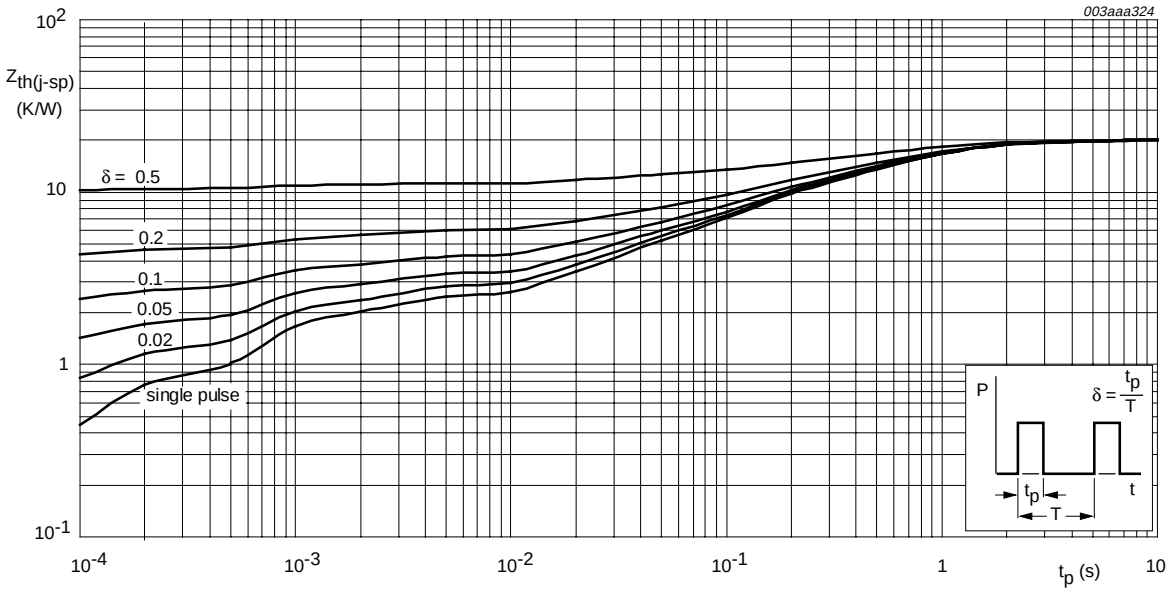




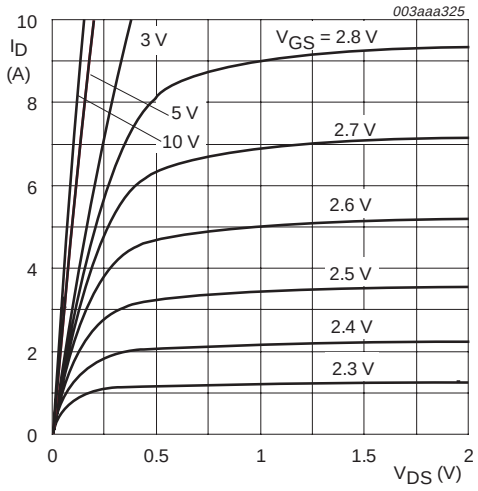

**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.**

## 5. Characteristics

**Table 4: Characteristics**

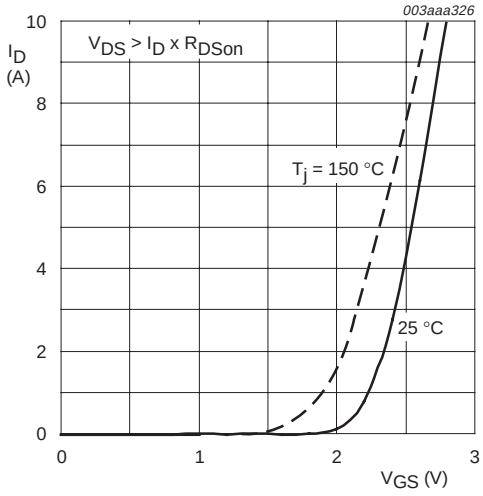
*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | 30 | - | - | V |
| | | $T_j$ = –55 °C | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 250 µA; $V_{DS}$ = $V_{GS}$; Figure 9 | | | | V |
| | | $T_j$ = 25 °C | 1 | 1.5 | 2 | V |
| | | $T_j$ = 150 °C | 0.5 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 2.2 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 24 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | 1 | µA |
| | | $T_j$ = 100 °C | - | - | 5 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±20 V; $V_{DS}$ = 0 V | - | - | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 8 A; Figure 7 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 17 | 20 | mΩ |
| | | $T_j$ = 150 °C | - | - | 33 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 7 A; Figure 7 | - | 21 | 26 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = 8 A; $V_{DD}$ = 15 V; $V_{GS}$ = 5 V; Figure 13 | - | 10.7 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 2.7 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 3.9 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 15 V; f = 1 MHz; Figure 11 | - | 752 | - | pF |
| $C_{oss}$ | output capacitance | | - | 200 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 130 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD}$ = 15 V; $I_D$ = 1.5 A; $V_{GS}$ = 10 V; $R_G$ = 6 Ω | - | 6 | - | ns |
| $t_r$ | rise time | | - | 7 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 23 | - | ns |
| $t_f$ | fall time | | - | 11 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 7 A; $V_{GS}$ = 0 V; Figure 12 | - | 0.86 | 1.1 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 7 A; $dI_S/dt$ = –100 A/µs; $V_R$ = 30 V; $V_{GS}$ = 0 V | - | 25 | - | ns |
| $Q_r$ | recovered charge | | - | 5 | - | nC |



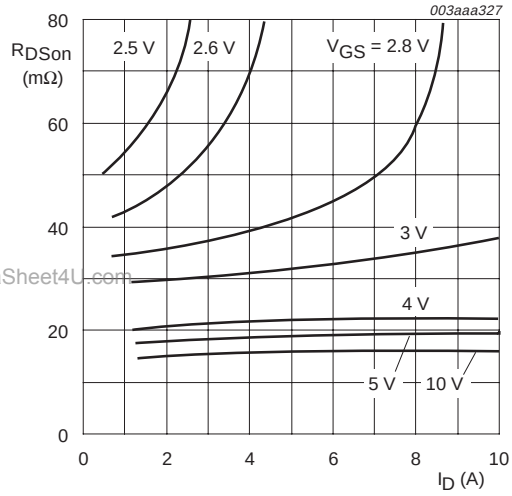

$T_j$ = 25 °C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**




$T_j$ = 25 °C and 150 °C; $V_{DS}$ > $I_D$ x $R_{DSon}$

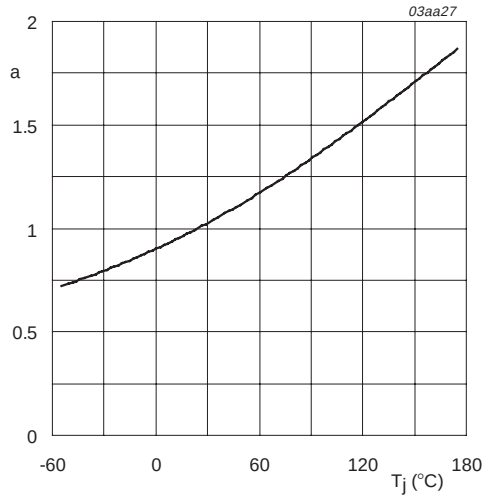
**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**





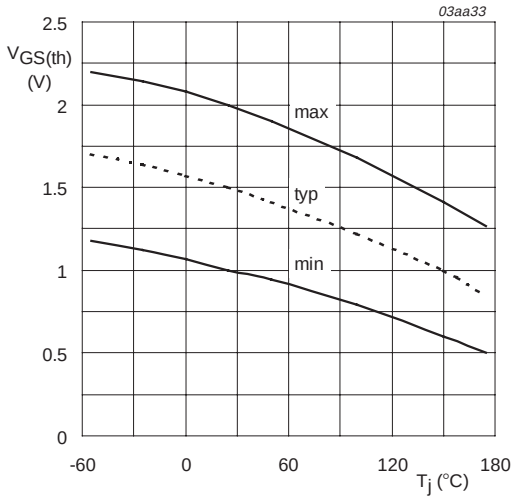

$T_j$ = 25 °C

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



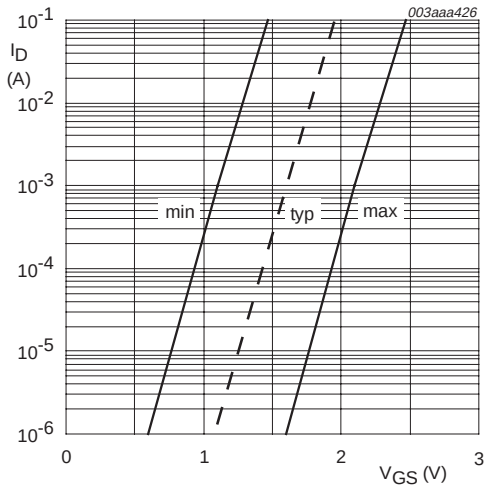

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



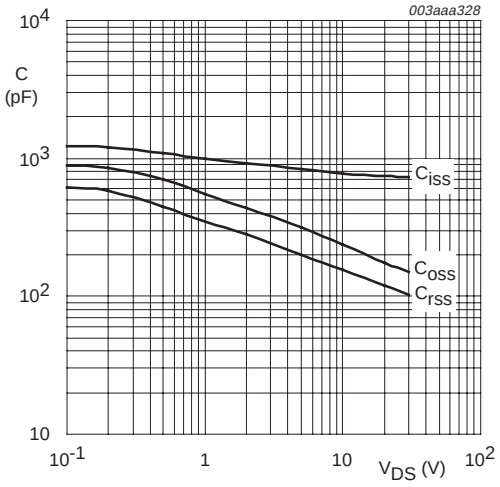

$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**




$T_j$ = 25 °C; $V_{DS}$ = 5 V

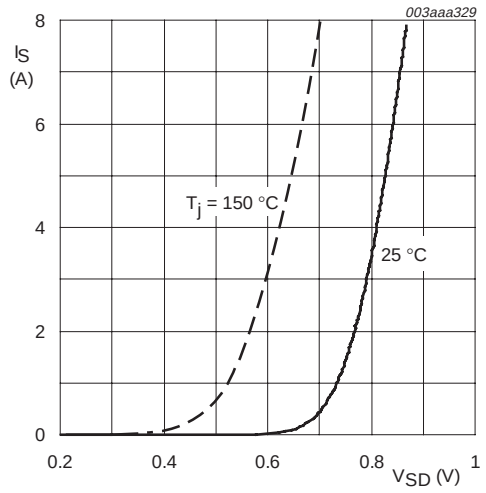
**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**





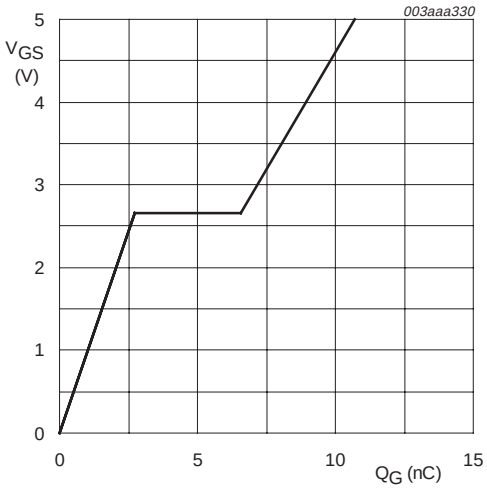

$V_{GS}$ = 0 V; f = 1 MHz

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**




$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**

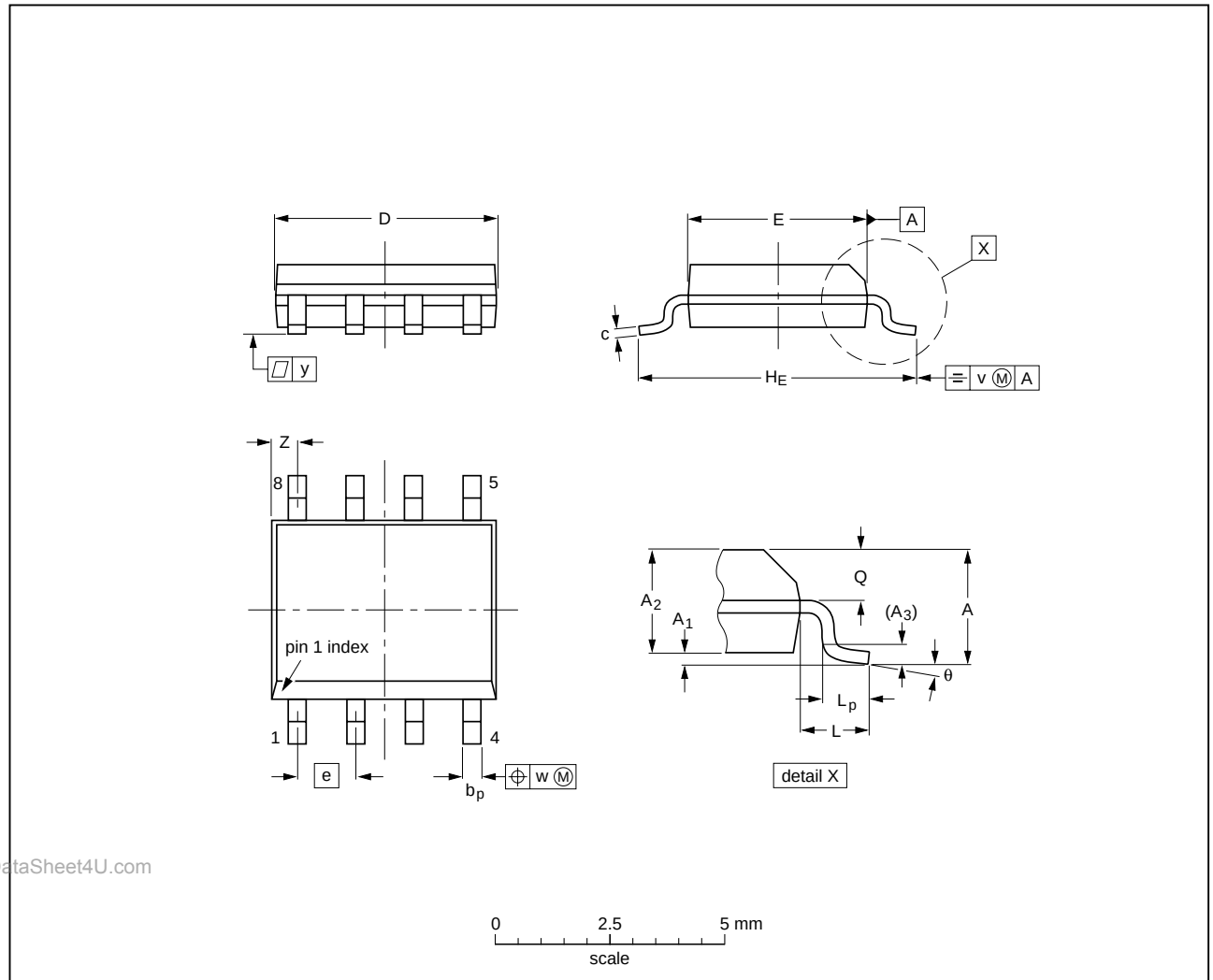



$I_D$ = 8 A; $V_{DD}$ = 15 V

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**

# 6. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**






**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 14. SOT96-1 (SO8).**

# 7. Revision history

**Table 5: Revision history**

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 01 | 20030623 | - | Product data (9397 750 11611) |

## 8. Data sheet status

| Level | Data sheet status[1] | Product status[2][3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 9. Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information —** Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 10. Disclaimers



**Life support —** These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes —** Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## 11. Trademarks

**TrenchMOS —** is a trademark of Koninklijke Philips Electronics N.V.

## Contact information

For additional information, please visit **http://www.semiconductors.philips.com**.
For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

**Fax: +31 40 27 24825**

# Contents







**Date of release: 23 June 2003** **Document order number: 9397 750 11611**