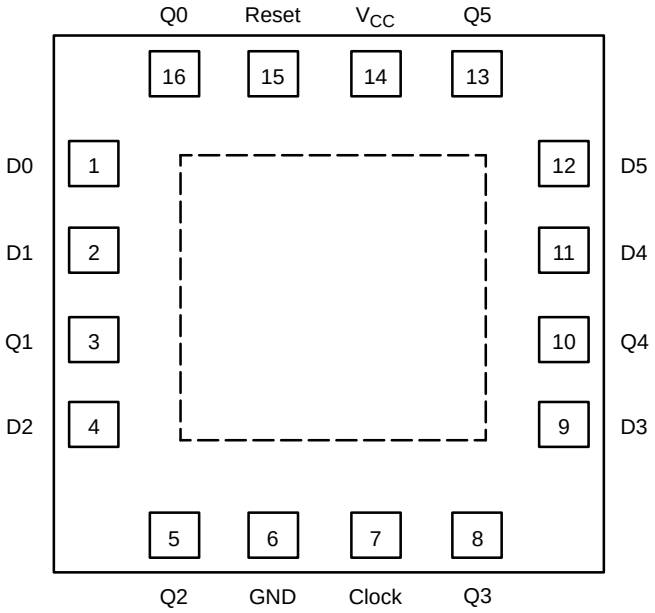
NLSF1174

Hex D Flip-Flop with Common Clock and Reset

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active low. All inputs/outputs are standard CMOS compatible.

Features

- Output Drive Compatibility: 10 LSTTL Loads
- Outputs Directly Interface to CMOS
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1.0 μA
- MSL Level 1
- Chip Complexity: 162 FET



Center pad on bottom may be connected to V_{CC} of device.
This pad must be isolated or connected to V_{CC}.

Figure 1. Pin Assignment (Top View)

FUNCTION TABLE

Inputs			Output
Reset	**Clock**	**D**	**Q**
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	No Change
H	↘	X	No Change

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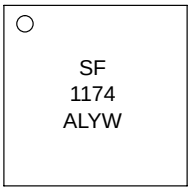
QFN-16
MN SUFFIX
CASE 485G

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

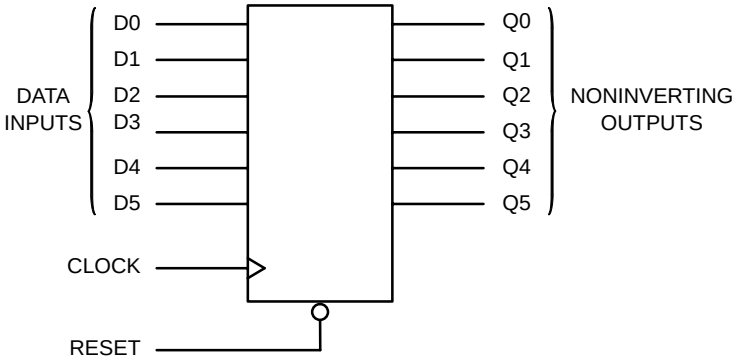


Figure 2. Logic Diagram

DESIGN/VALUE TABLE

Design Criteria	Value	Units
Internal Gate Count*	40.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two-input NAND gate.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	−0.5 to +7.0	V
V_{IN}	DC Input Voltage	(Referenced to GND)	−1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage	(Referenced to GND) (Note 2)	−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	PDIP, SOIC, TSSOP	260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	QFN	80	°C/W
P_D	Power Dissipation in Still Air at 85°C	QFN	800	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30 to 35	UL 94 V-O @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >100 >500	V
$I_{LATCH-UP}$	Latch-Up Performance	Above V_{CC} and Below GND at 85°C (Note 6)	±300	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.
7. For high frequency or heavy load considerations, see the ON Semiconductor High- Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage	(Referenced to GND) (Note 8)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 4)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

8. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55°C to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\| \leq 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\| \leq 20$ μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA $\|I_{OUT}\| \leq 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA $\|I_{OUT}\| \leq 5.2$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0 μA	6.0	4.0	40	160	μA

9. Information on typical parametric values, along with high frequency or heavy load considerations, can be found in the ON Semiconductor High- Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55°C to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 4 and 7)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 5 and 7)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 7)	2.0 4.5 6.0	110 21 19	140 28 24	160 32 27	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 4 and 7)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

10. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High- Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance, per Enabled Output (Note 11)	62	pF

11. Used to determine the no- load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High- Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Figure	V_{CC} V	Guaranteed Limit						Unit
				−55°C to 25°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	6	2.0 4.5 6.0	50 10 9.0		65 13 11		75 15 13		ns
t_h	Minimum Hold Time, Clock to Data	6	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock	5	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Clock	4	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t_w	Minimum Pulse Width, Reset	5	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t_r, t_f	Maximum Input Rise and Fall Times	4	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns

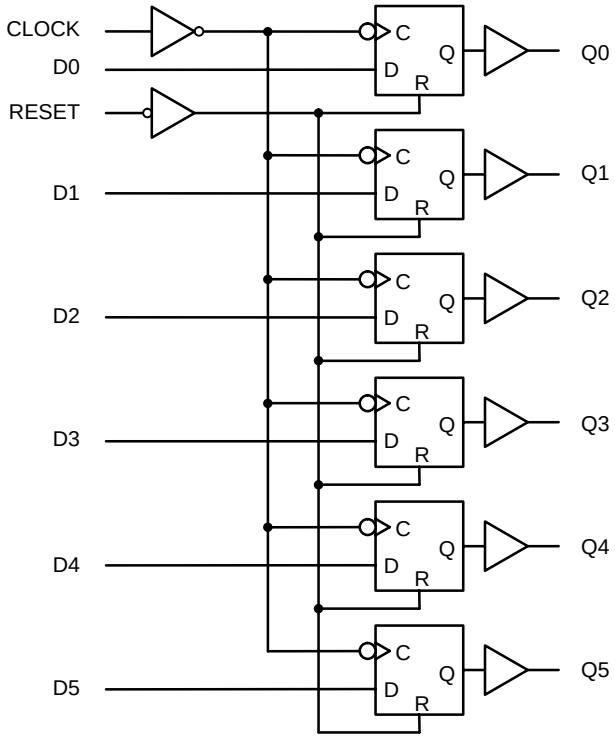


Figure 3. Expanded Logic Diagram

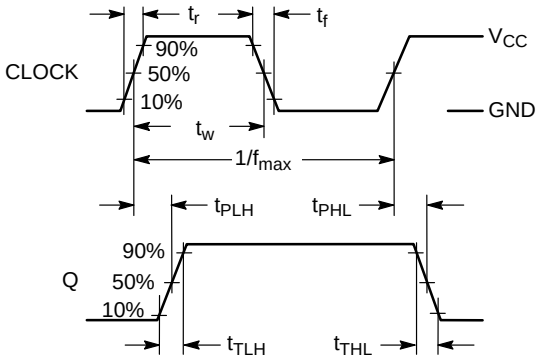


Figure 4. Switching Waveform

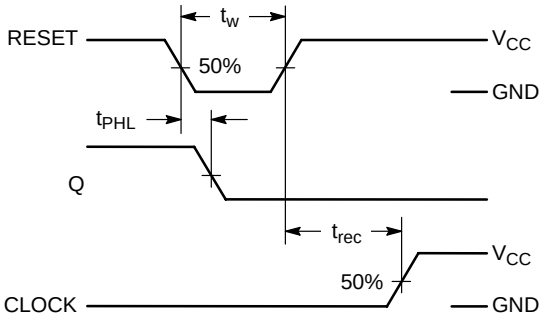


Figure 5. Switching Waveform

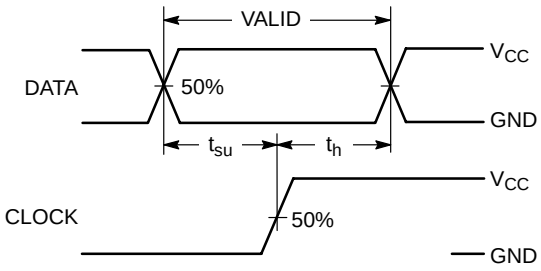
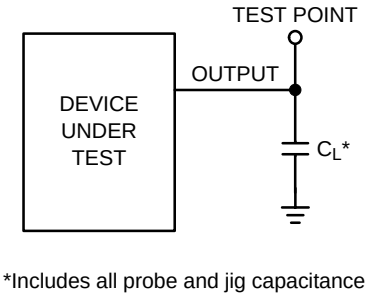


Figure 6. Switching Waveform



*Includes all probe and jig capacitance

Figure 7. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature					Package Type	Tape & Reel Size
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLSF1174MNR2	NL	SF	1174	MN	R2	QFN	7-inch/2500 Unit

PIN1/PRODUCT ORIENTATION CARRIER TAPE

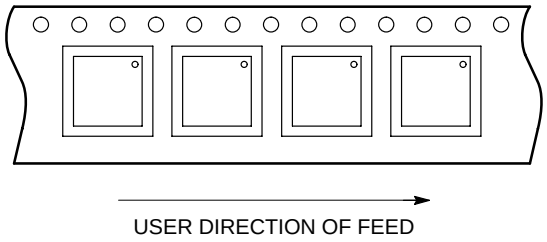
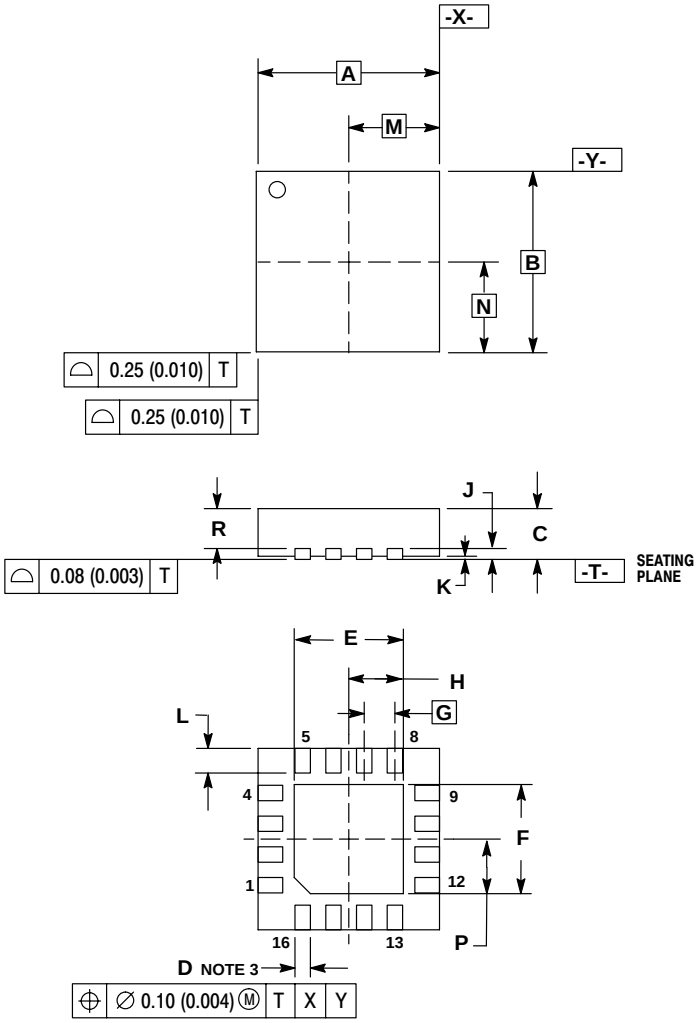


Figure 8.

PACKAGE DIMENSIONS

QFN-16
MN SUFFIX
CASE 485G-01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

Notes

PUBLICATION ORDERING INFORMATION

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