

LH532000B-S

CMOS 2M (256K × 8/128K × 16)
3 V-Drive Mask-Programmable ROM

FEATURES

- 262,144 words × 8 bit organization
(Byte mode)
131,072 words × 16 bit organization
(Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access times:
500 ns (MAX.) at $2.6 \text{ V} \leq V_{\text{CC}} < 4.5 \text{ V}$
150 ns (MAX.) at $4.5 \text{ V} \leq V_{\text{CC}} \leq 5.5 \text{ V}$
- Static operation
- Three-state outputs
- Low-power supply: 2.6 to 5.5 V
- Programmable $\text{OE}/\overline{\text{OE}}$ and $\text{OE}_1/\overline{\text{OE}}_1/\text{DC}$
- Packages:
40-pin, 600-mil DIP
40-pin, 525-mil SOP
48-pin, $12 \times 18 \text{ mm}^2$ TSOP (Type I)

DESCRIPTION

The LH532000B-S is a CMOS 4M-bit mask-programmable ROM organized as $262,144 \times 8$ bits (Byte mode) or $131,072 \times 16$ bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin.

It is suited for use in compact battery back-up systems due to be operated on 3 V power supply.

PIN CONNECTIONS

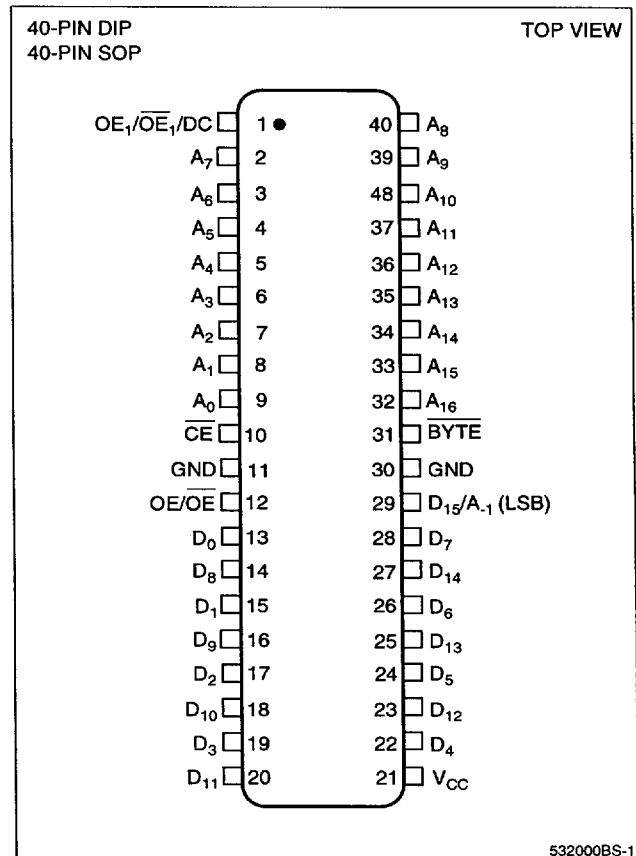


Figure 1. Pin Connections for DIP and SOP Packages

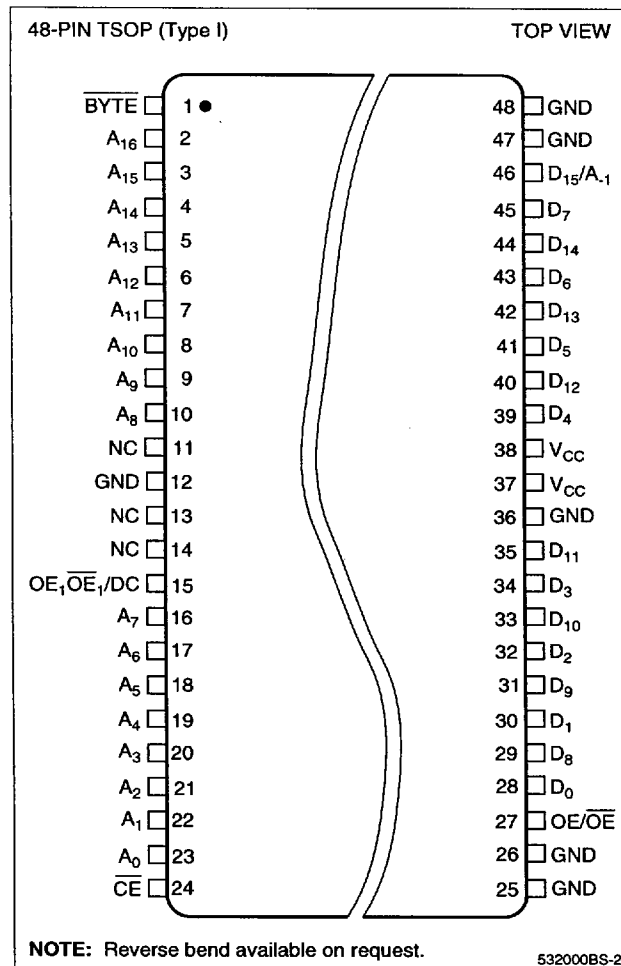


Figure 2. Pin Connections for TSOP Package

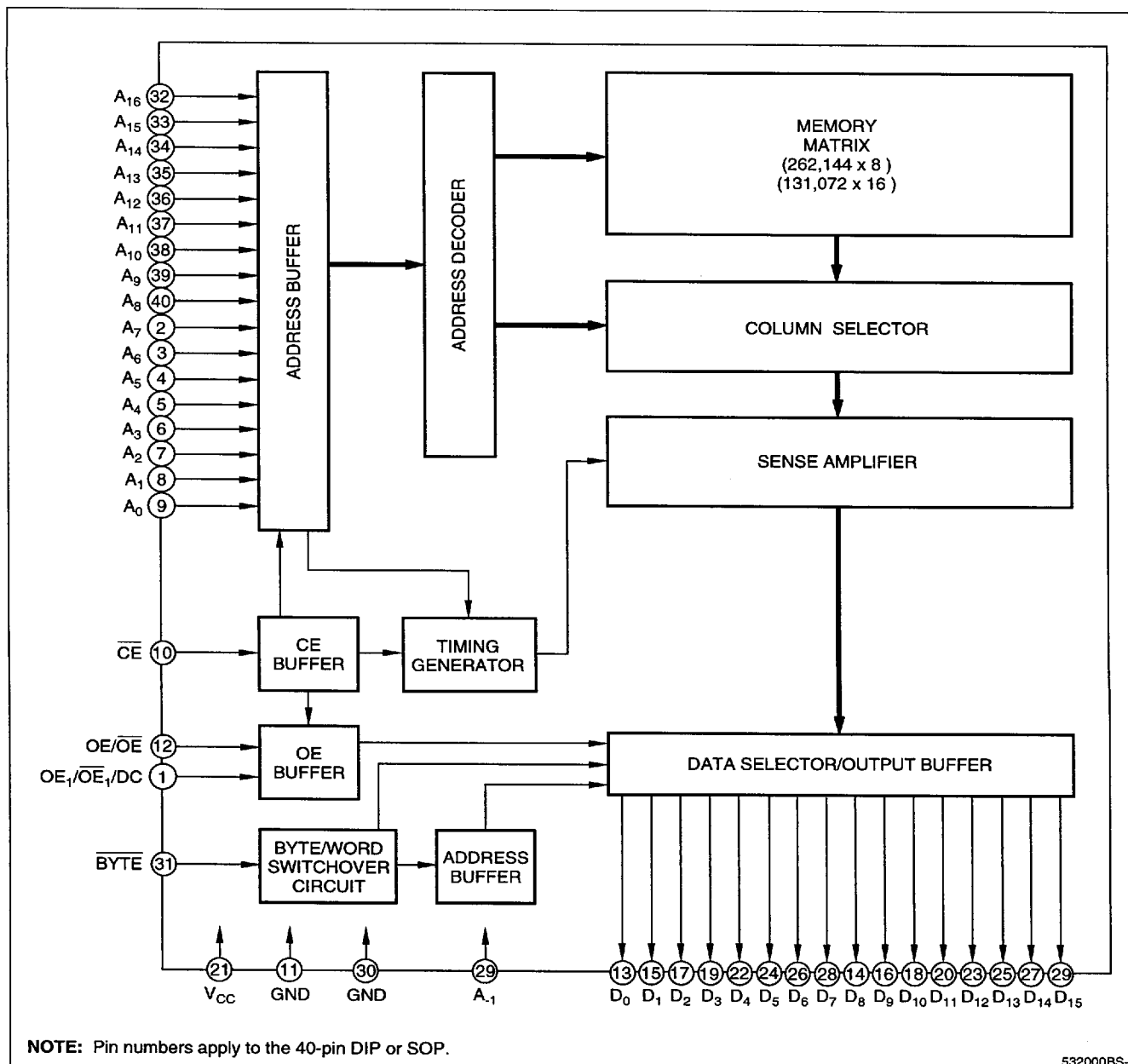


Figure 3. LH532000B-S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₁ – A ₁₆	Address input	1
D ₀ – D ₁₅	Data output	1
BYTE	Byte/word mode switch	1
CE	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/OE	Output enable input	2
OE ₁ /OE ₁ /DC	Output enable input	2, 3
V _{CC}	Power supply	
GND	Ground	

NOTES:

- The D₁₅/A₁ pin becomes LSB address input (A₁) when the $\overline{\text{BYTE}}$ pin is set to be LOW in byte mode, and data output (D₁₅) when set to be HIGH in word mode.
- Active levels of OE/OE and OE₁/OE₁/DC are mask-programmable.
- DC = Don't care.

TRUTH TABLE

$\overline{CE}$	$OE/\overline{OE}$	$OE_1/\overline{OE}_1$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	—	—	Standby
L	L/H	X	X	X	High-Z	High-Z	—	—	Operating
L	X	L/H	X	X	High-Z	High-Z	—	—	Operating
L	H/L	H/L	H	—	$D_0 - D_7$	$D_8 - D_{15}$	A_0	A_{16}	Operating
L	H/L	H/L	L	L	$D_0 - D_7$	High-Z	A_{-1}	A_{16}	Operating
L	H/L	H/L	L	H	$D_8 - D_{15}$	High-Z	A_{-1}	A_{16}	Operating

NOTE:

X = H or L, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		5.5	V

DC CHARACTERISTICS ($V_{CC} = 2.6$ to 5.5 V, $T_A = 0$ to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		0.8 V_{CC}	$V_{CC} + 0.3$	V	
Input 'Low' voltage	V_{IL}		-0.3	0.4	V	
Output 'High' voltage	V_{OH}	$I_{OH} = -100 \mu A$	0.8 V_{CC}		V	
Output 'Low' voltage	V_{OL}	$I_{OL} = 400 \mu A$		0.4	V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0 \text{ V to } V_{CC}$		10	μA	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0 \text{ V to } V_{CC}$		10	μA	1
Operating current	I_{CC1}	$t_{RC} = 150 \text{ ns}$		50	mA	2
	I_{CC2}	$t_{RC} = 500 \text{ ns}$		35	mA	3
	I_{CC3}	$t_{RC} = 500 \text{ ns}$		15	mA	4
Standby current	I_{SB1}	$\overline{CE} = V_{IH}$		3	mA	
	I_{SB2}	$\overline{CE} = V_{CC} - 0.2 \text{ V}$		100	μA	
Input capacitance	C_{IN}	$f = 1 \text{ MHz}$ $T_A = 25^\circ C$		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:

1. $\overline{CE}/OE/\overline{OE}_1 = V_{IH}$, $OE/OE_1 = V_{IL}$
2. $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$, outputs open
3. $3.4 \text{ V} < V_{CC} < 4.5 \text{ V}$, outputs open
4. $2.6 \text{ V} \leq V_{CC} \leq 3.4 \text{ V}$, outputs open

AC CHARACTERISTICS ($V_{CC} = 2.6$ to 5.5 V, $T_A = 0$ to $+70^\circ\text{C}$)

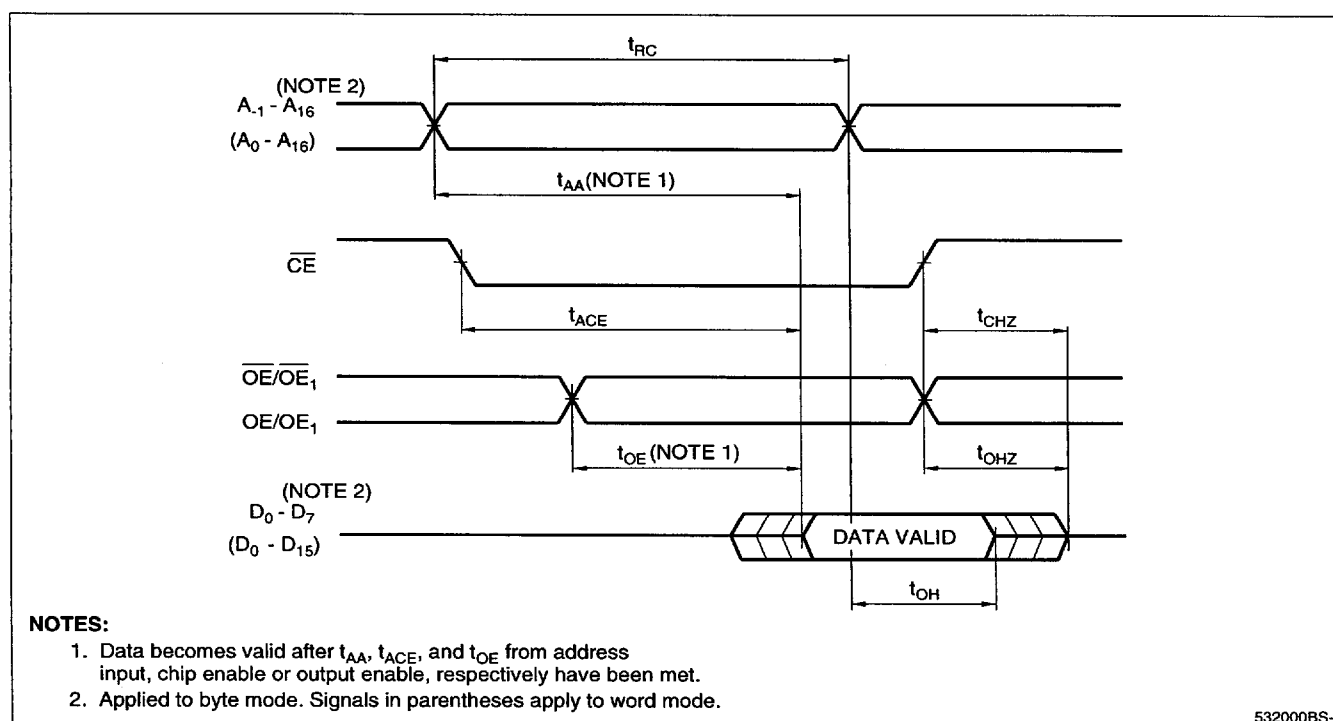
PARAMETER	SYMBOL	$2.6 \leq V_{CC} < 4.5$		$4.5 \leq V_{CC} \leq 5.5$		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	500		150		ns	
Address access time	t_{AA}		500		150	ns	
Chip enable time	t_{ACE}		500		150	ns	
Output enable time	t_{OE}		150		80	ns	
Output hold time	t_{OH}	10		10		ns	
CE to output in High-Z	t_{CHZ}		150		80	ns	1
OE to output in High-Z	t_{OHZ}		150		80	ns	

NOTE:

1. This is the time required for the outputs to become high-impedance.

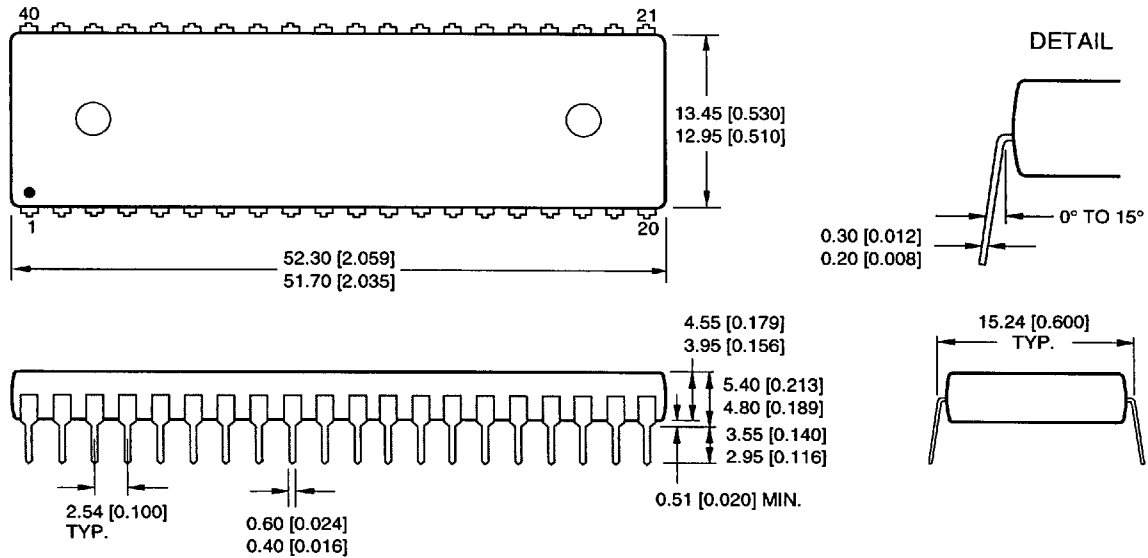
AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 to $(0.8 \times V_{CC})$ V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF

**Figure 4. Timing Diagram**

PACKAGE DIAGRAMS

40DIP (DIP040-P-0600)

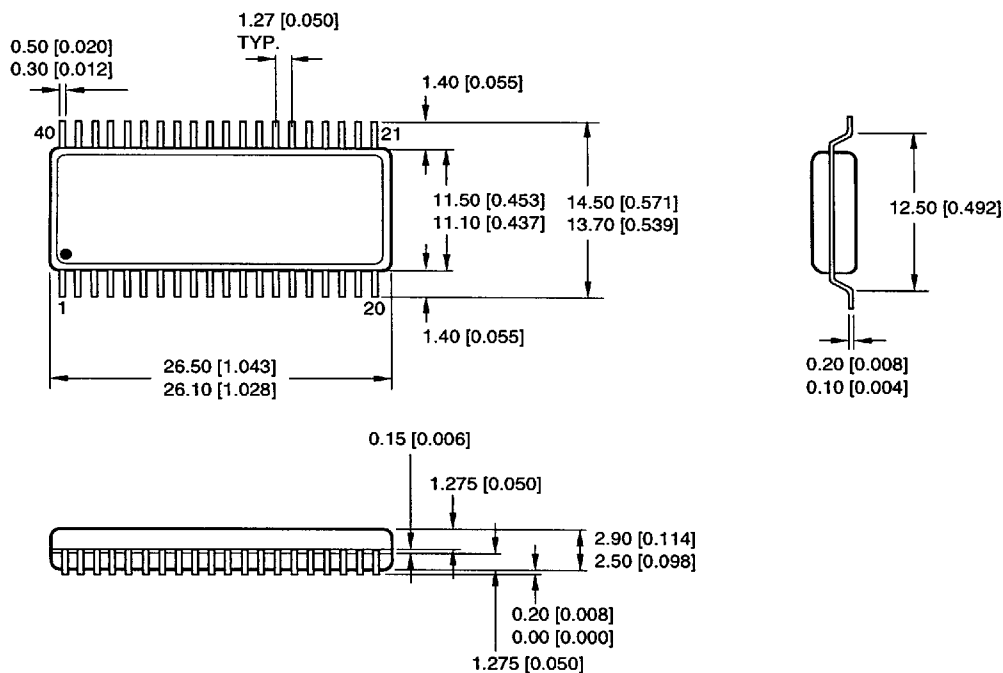


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
 MINIMUM LIMIT

40DIP

40-pin, 600-mil DIP

40SOP (SOP040-P-0525)

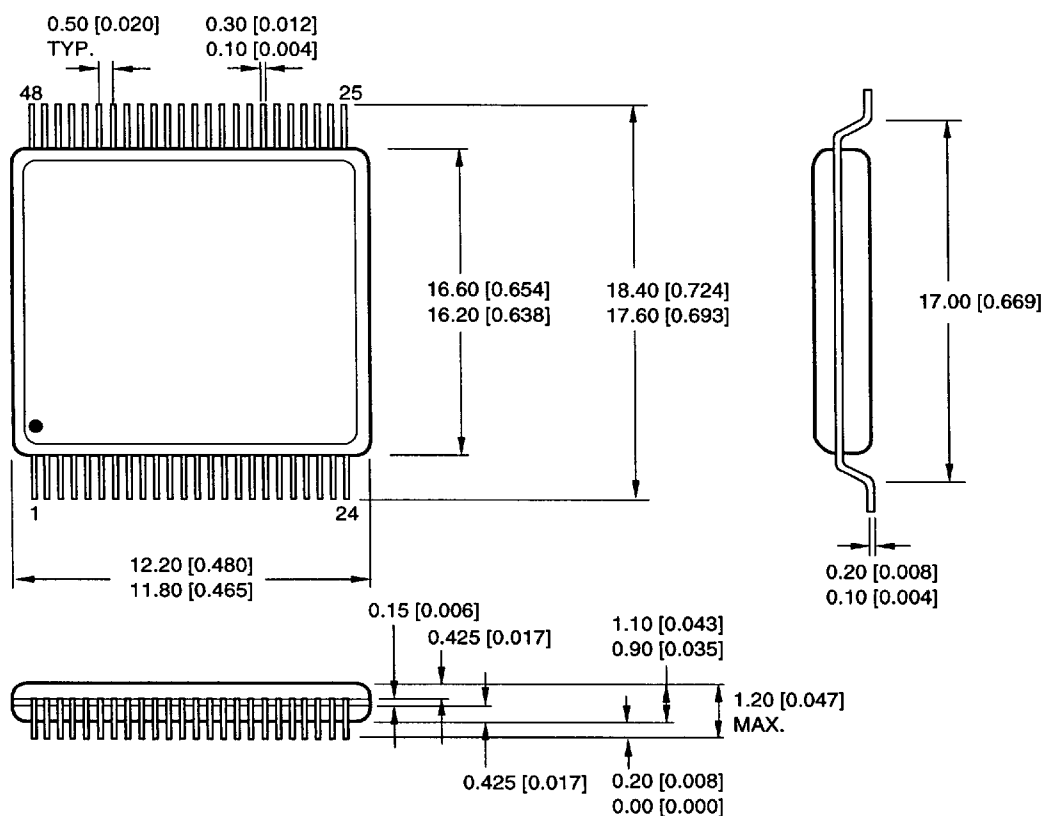


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
 MINIMUM LIMIT

40SOP

40-pin, 525-mil SOP

48TSOP (TSOP048-P-1218)



DIMENSIONS IN MM (INCHES) MAXIMUM LIMIT
MINIMUM LIMIT

48TSOP

48-pin, 12 × 18 mm² TSOP (Type I)

ORDERING INFORMATION

LH532000B Device Type	X Package	- S Low-Voltage Operation
		D 40-pin, 600-mil DIP (DIP040-P-0600) N 40-pin, 525-mil SOP (SOP040-P-0525) T 48-pin, 12 x 18 mm ² TSOP (Type I) (TSOP048-P-1218) TR 48-pin, 12 x 18 mm ² TSOP (Type I) Reverse bend (TSOP048-P-1218)
		CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM
Example: LH532000BD-S (CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM, Low-Voltage Operation, 40-pin, 600-mil DIP)		

532000BS-6

SHARP

8180798 0015868 898