

LH28F320S5-L90/12 32-MBIT (4MBx8/2MBx16) Smart 5 Flash MEMORY

- **Smart 5 Technology**
 - 5V V_{CC}
 - 5V V_{PP}
- **Common Flash Interface (CFI)**
 - Universal & Upgradable Interface
- **Scalable Command Set (SCS)**
- **High Speed Write Performance**
 - 32 Bytes x 2 plane Page Buffer
 - 2 μ S/Byte Write Transfer Rate
- **High Speed Read Performance**
 - 90/12: 90ns(5V \pm 5%), 100/120ns(5V \pm 10%)
- **Enhanced Automated Suspend Options**
 - Write Suspend to Read
 - Block Erase Suspend to Write
 - Block Erase Suspend to Read
- **Industry-Standard Packaging**
 - 56-Lead SSOP
- **Chip Size Packaging**
 - 64-Lead CSP
- **SRAM-Compatible Write Interface**
- **User-Configurable x8 or x16 Operation**
- **High-Density Symmetrically-Blocked Architecture**
 - Sixty-four 64-Kbyte Erasable Blocks
- **Enhanced Data Protection Features**
 - Absolute Protection with $V_{PP}=GND$
 - Flexible Block Locking
 - Erase/Write Lockout during Power Transitions
- **Extended Cycling Capability**
 - 100,000 Block Erase Cycles
 - 6.4 Million Block Erase Cycles/Chip
- **Low Power Management**
 - Deep Power-Down Mode
 - Automatic Power Savings Mode Decreases I_{CC} in Static Mode
- **Automated Write and Erase**
 - Command User Interface
 - Status Register
- **ETOX™* V Nonvolatile Flash Technology**
- **Not designed or rated as radiation hardened**

SHARP's LH28F320S5-L90/12 Flash memory with Smart 5 technology is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. Its symmetrically-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F320S5-L90/12 offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F320S5-L90/12 is conformed to the flash Scalable Command Set (SCS) and the Common Flash Interface (CFI) specification which enable universal and upgradable interface, enable the highest system/device data transfer rates and minimize device and system-level implementation costs.

The LH28F320S5-L90/12 is manufactured on SHARP's 0.4 μ m ETOX™* V process technology. It comes in industry-standard package: the 56-Lead SSOP or Chip size package: the 64-Lead CSP, ideal for board constrained applications.

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LH28F320S5-L90/12 Smart 5 Flash MEMORY

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CONTENTS

| | PAGE | | PAGE |
|---|------|---|----------|
| 1 INTRODUCTION | 4 | 5 DESIGN CONSIDERATIONS | 33 |
| 1.1 Product Overview | 4 | 5.1 Three-Line Output Control | 33 |
| 2 PRINCIPLES OF OPERATION | 8 | 5.2 STS and Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration Polling..... | 33 33 |
| 2.1 Data Protection | 8 | 5.3 Power Supply Decoupling | 33 |
| 3 BUS OPERATION | 10 | 5.4 V _{PP} Trace on Printed Circuit Boards | 33 |
| 3.1 Read | 10 | 5.5 V _{CC} , V _{PP} , RP# Transitions..... | 34 |
| 3.2 Output Disable | 10 | 5.6 Power-Up/Down Protection..... | 34 |
| 3.3 Standby | 10 | 5.7 Power Dissipation | 34 |
| 3.4 Deep Power-Down | 10 | 6 ELECTRICAL SPECIFICATIONS | 35 |
| 3.5 Read Identifier Codes Operation | 11 | 6.1 Absolute Maximum Ratings | 35 |
| 3.6 Query Operation..... | 11 | 6.2 Operating Conditions | 35 |
| 3.7 Write..... | 11 | 6.2.1 Capacitance | 35 |
| 4 COMMAND DEFINITIONS | 11 | 6.2.2 AC Input/Output Test Conditions | 36 |
| 4.1 Read Array Command..... | 14 | 6.2.3 DC Characteristics..... | 37 |
| 4.2 Read Identifier Codes Command | 14 | 6.2.4 AC Characteristics - Read-Only Operations | 39 |
| 4.3 Read Status Register Command..... | 14 | 6.2.5 AC Characteristics - Write Operations | 42 |
| 4.4 Clear Status Register Command..... | 14 | 6.2.6 Alternative CE#-Controlled Writes | 44 |
| 4.5 Query Command..... | 15 | 6.2.7 Reset Operations | 46 |
| 4.5.1 Block Status Register | 15 | 6.2.8 Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration Performance..... | 46 47 |
| 4.5.2 CFI Query Identification String..... | 16 | 7 ADDITIONAL INFORMATION | 48 |
| 4.5.3 System Interface Information | 16 | 7.1 Ordering Information | 48 |
| 4.5.4 Device Geometry Definition | 17 | | |
| 4.5.5 SCS OEM Specific Extended Query Table .. | 17 | | |
| 4.6 Block Erase Command..... | 18 | | |
| 4.7 Full Chip Erase Command | 18 | | |
| 4.8 Word/Byte Write Command..... | 19 | | |
| 4.9 Multi Word/Byte Write Command | 19 | | |
| 4.10 Block Erase Suspend Command..... | 20 | | |
| 4.11 (Multi) Word/Byte Write Suspend Command... | 20 | | |
| 4.12 Set Block Lock-Bit Command..... | 21 | | |
| 4.13 Clear Block Lock-Bits Command..... | 21 | | |
| 4.14 STS Configuration Command | 22 | | |

LH28F320S5-L90/12 Smart 5 Flash MEMORY

1 INTRODUCTION

This datasheet contains LH28F320S5-L90/12 specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 Product Overview

The LH28F320S5-L90/12 is a high-performance 32-Mbit Smart 5 Flash memory organized as 4MBx8/2MBx16. The 4MB of data is arranged in sixty-four 64-Kbyte blocks which are individually erasable, lockable, and unlockable in-system. The memory map is shown in Figure 4.

Smart 5 technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. 5V V_{CC} provides the highest read performance. V_{PP} at 5V eliminates the need for a separate 12V converter, while $V_{PP}=5V$ maximizes erase and write performance. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{CC} and V_{PP} Voltage Combinations Offered by Smart 5 Technology

| V_{CC} Voltage | V_{PP} Voltage |
|------------------|------------------|
| 5V | 5V |

Internal V_{CC} and V_{PP} detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

A block erase operation erases one of the device's 64-Kbyte blocks typically within 0.34 second (5V V_{CC} ,

5V V_{PP}) independent of other blocks. Each block can be independently erased 100,000 times (6.4 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

A word/byte write is performed in byte increments typically within 9.24 μ s (5V V_{CC} , 5V V_{PP}). A multi word/byte write has high speed write performance of 2 μ s/byte (5V V_{CC} , 5V V_{PP}). (Multi) Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits and WP#, Sixty-four block lock-bits, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and (multi) word/byte write operations. Block lock-bit configuration operations (Set Block Lock-Bit and Clear Block Lock-Bits commands) set and cleared block lock-bits.

The status register indicates when the WSM's block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is finished.

The STS output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using STS minimizes both CPU overhead and system power consumption. STS pin can be configured to different states using the Configuration command. The STS pin defaults to RY/BY# operation. When low, STS indicates that the WSM is performing a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration. STS-High Z indicates that the WSM is ready for a new command, block erase is suspended and (multi) word/byte write are inactive, (multi) word/byte write are suspended, or the device is in deep power-down mode. The other 3 alternate configurations are all pulse mode for use as a system interrupt.

The access time is 90ns (t_{AVAV}) over the commercial temperature range (0°C to +70°C) and V_{CC} supply voltage range of 4.75V-5.25V. At lower V_{CC} voltages, the access times are 100ns/120ns (4.5V-5.5V).

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 1 mA at 5V V_{CC} .

When either $CE_0\#$ or $CE_1\#$, and $RP\#$ pins are at V_{CC} , the I_{CC} CMOS standby mode is enabled. When the $RP\#$ pin is at GND, deep power-down mode is

enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from $RP\#$ switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from $RP\#$ -high until writes to the CUI are recognized. With $RP\#$ at GND, the WSM is reset and the status register is cleared.

The device is available in 56-Lead SSOP (Shrink Small Outline Package) and 64-Lead CSP (Chip Size Package). Pinout is shown in Figure 2 and 3.

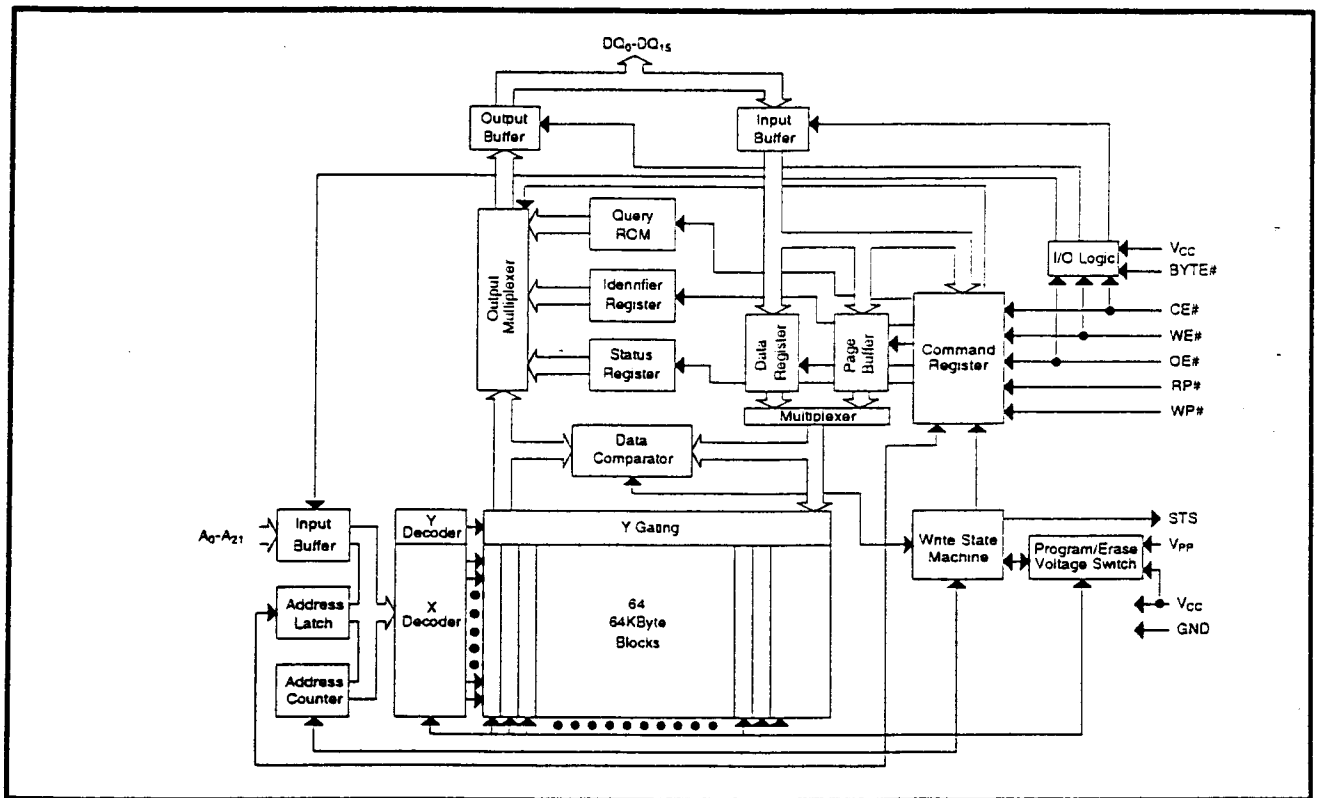


Figure 1. Block Diagram

LH28F320S5-L90/12 Smart 5 Flash MEMORY

Table 2. Pin Descriptions

| Symbol | Type | Name and Function |
|---|-------------------------|--|
| A ₀ -A ₂₁ | INPUT | ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A ₀ : Byte Select Address. Not used in x16 mode (can be floated). A ₁ -A ₄ : Column Address. Selects 1 of 16 bit lines. A ₅ -A ₁₅ : Row Address. Selects 1 of 2048 word lines. A ₁₆ -A ₂₁ : Block Address. |
| DQ ₀ -DQ ₁₅ | INPUT/ OUTPUT | DATA INPUT/OUTPUTS: DQ ₀ -DQ ₇ : Inputs data and commands during CUI write cycles; outputs data during memory array, status register, query, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ ₈ -DQ ₁₅ : Inputs data during CUI write cycles in x16 mode; outputs data during memory array read cycles in x16 mode; not used for status register, query and identifier code read mode. Data pins float to high-impedance when the chip is deselected, outputs are disabled, or in x8 mode (Byte# = V _{IL}). Data is internally latched during a write cycle. |
| CE ₀ #, CE ₁ # | INPUT | CHIP ENABLE: Activates the device's control logic, input buffers decoders, and sense amplifiers. Either CE ₀ # or CE ₁ # V _{IH} deselected the device and reduces power consumption to standby levels. Both CE ₀ # and CE ₁ # must be V _{IL} to select the devices. |
| RP# | INPUT | RESET/DEEP POWER-DOWN: Puts the device in deep power-down mode and resets internal automation. RP# V _{IH} enables normal operation. When driven V _{IL} , RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. |
| OE# | INPUT | OUTPUT ENABLE: Gates the device's outputs during a read cycle. |
| WE# | INPUT | WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse. |
| STS | OPEN DRAIN OUTPUT | STS (RY/BY#): Indicates the status of the internal WSM. When configured in level mode (default mode), it acts as a RY/BY# pin. When low, the WSM is performing an internal operation (block erase, full chip erase, (multi) word/byte write or block lock-bit configuration). STS High Z indicates that the WSM is ready for new commands, block erase is suspended, and (multi) word/byte write is inactive, (multi) word/byte write is suspended or the device is in deep power-down mode. For alternate configurations of the STATUS pin, see the Configuration command. |
| WP# | INPUT | WRITE PROTECT: Master control for block locking. When V _{IL} . Locked blocks can not be erased and programmed, and block lock-bits can not be set and reset. |
| BYTE# | INPUT | BYTE ENABLE: BYTE# V _{IL} places device in x8 mode. All data is then input or output on DQ ₀₋₇ , and DQ ₈₋₁₅ float. BYTE# V _{IH} places the device in x16 mode, and turns off the A ₀ input buffer. |
| V _{PP} | SUPPLY | BLOCK ERASE, FULL CHIP ERASE, (MULTI) WORD/BYTE WRITE, BLOCK LOCK-BIT CONFIGURATION POWER SUPPLY: For erasing array blocks, writing bytes or configuring block lock-bits. With V _{PP} ≤ V _{PPLK} , memory contents cannot be altered. Block erase, full chip erase, (multi) word/byte write and block lock-bit configuration with an invalid V _{PP} (see DC Characteristics) produce spurious results and should not be attempted. |
| V _{CC} | SUPPLY | DEVICE POWER SUPPLY: Internal detection configures the device for 5V operation. Do not float any power pins. With V _{CC} ≤ V _{LKO} , all write attempts to the flash memory are inhibited. Device operations at invalid V _{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted. |
| GND | SUPPLY | GROUND: Do not float any ground pins. |
| NC | | NO CONNECT: Lead is not internal connected; it may be driven or floated. |

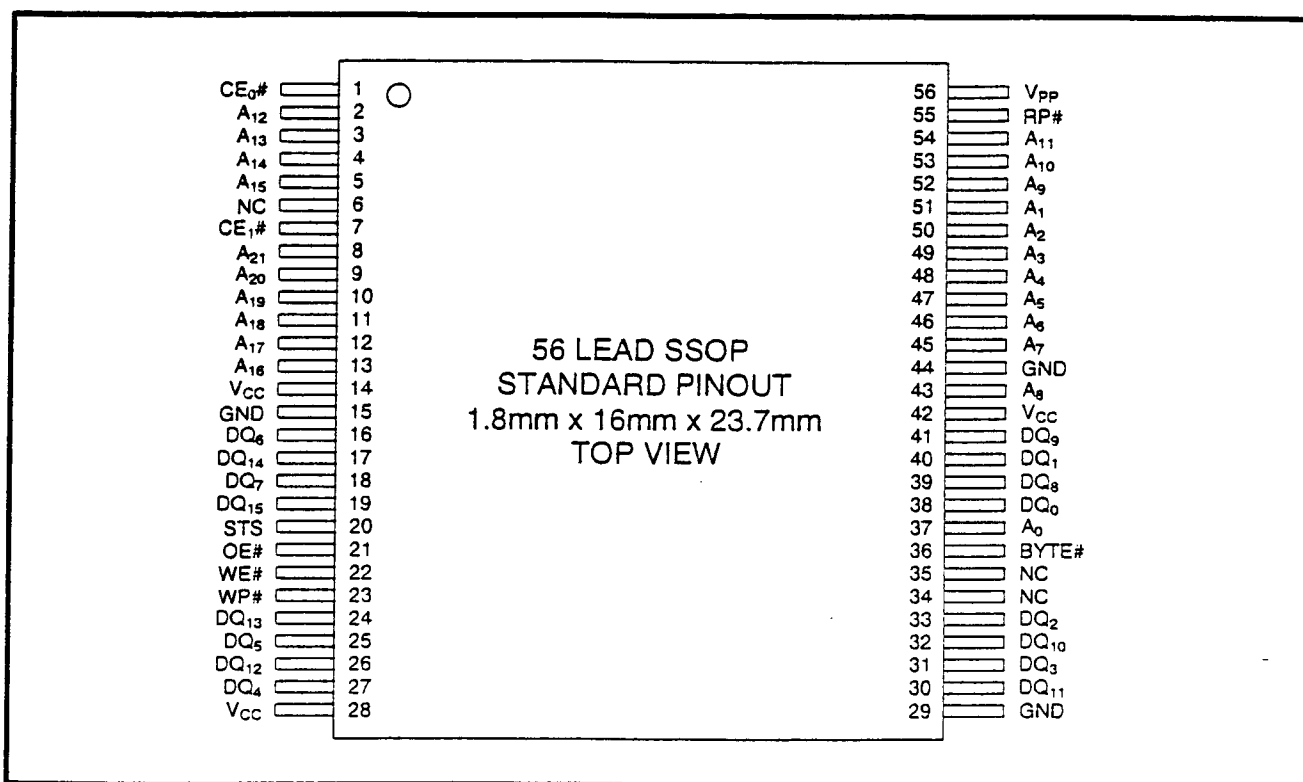


Figure 2. SSOP 56-Lead Pinout

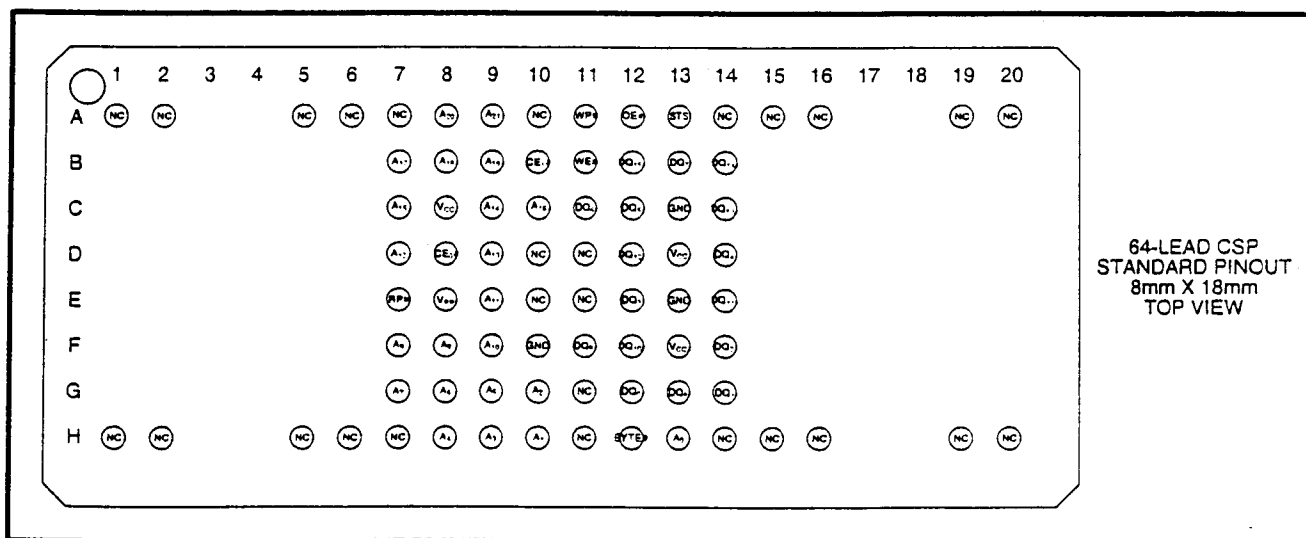


Figure 3. CSP 64-Lead Pinout

LH28F320S5-L90/12 Smart 5 Flash MEMORY

2 PRINCIPLES OF OPERATION

The LH28F320S5-L90/12 Flash memory includes an on-chip WSM to manage block erase, full chip erase, (multi) word/byte write and block lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, and minimal processor overhead with RAM-Like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register, query structure and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. All functions associated with altering memory contents—block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, status, query and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, outputs query structure or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, (multi) word/byte write and block lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Write suspend allows system software to suspend a (multi) word/byte write to read data from any other flash memory array location.

2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when block erase, full chip erase, (multi) word/byte write and block lock-bit configuration are required) or hardwired to V_{PPH1} . The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with multi-step block erase, full chip erase, (multi) word/byte write and block lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP} . All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when $RP\#$ is at V_{IL} . The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and (multi) word/byte write operations.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes, query structure, or status register independent of the V_{PP} voltage. RP# must be at V_{IH} .

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, Query or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component: CE# ($CE_0\#$, $CE_1\#$), OE#, WE#, RP# and WP#. $CE_0\#$, $CE_1\#$ and OE# must be driven active to obtain data at the outputs. $CE_0\#$, $CE_1\#$ is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0 - DQ_{15}) control and when active drives the selected memory data onto the I/O bus. WE# and RP# must be at V_{IH} . Figure 18, 19 illustrates a read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ_0 - DQ_{15} are placed in a high-impedance state.

3.3 Standby

Either $CE_0\#$ or $CE_1\#$ at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0 - DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, full chip erase, (multi) word/byte write and

block lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time t_{pHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, full chip erase, (multi) word/byte write or block lock-bit configuration modes, RP#-low will abort the operation. STS remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{pHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code, device code, block status codes for each block (see Figure 5). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block status codes identify locked or unlocked block setting and erase completed or erase uncompleted condition.

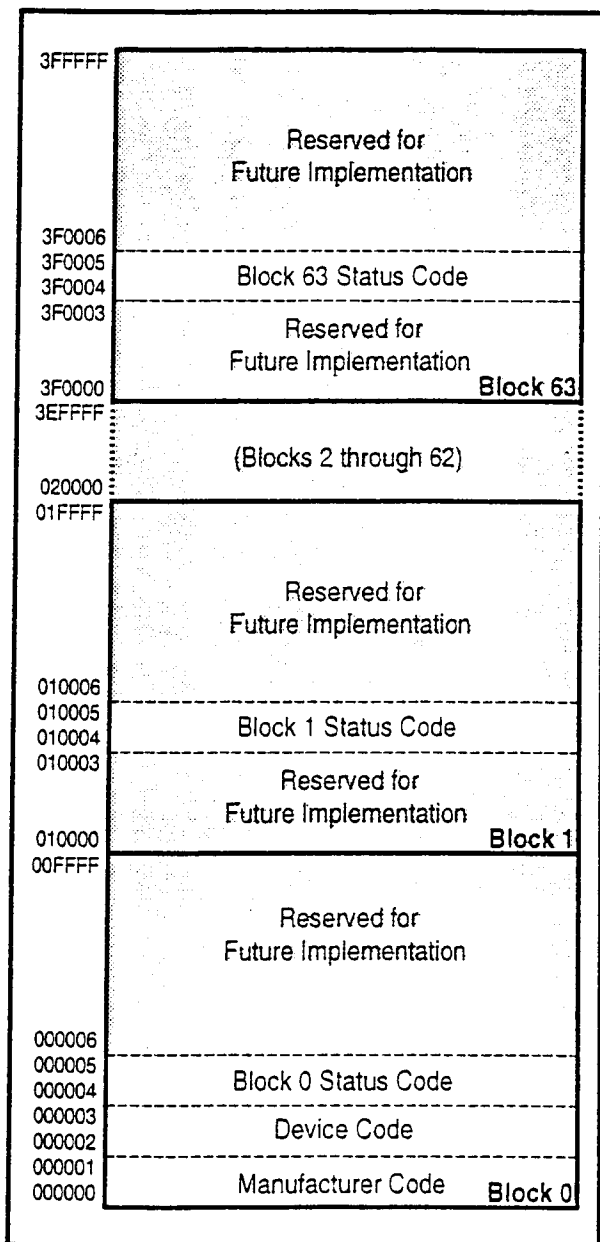


Figure 5. Device Identifier Code Memory Map

3.6 Query Operation

The query operation outputs the query structure. Query database is stored in the 48Byte ROM. Query structure allows system software to gain critical information for controlling the flash component. Query structure are always presented on the lowest-order data output (DQ₀-DQ₇) only.

3.7 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1}$, the CUI additionally controls block erase, full chip erase, (multi) word/byte write and block lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/byte Write command requires the command and address of the location to be written. Set Block Lock-Bit command requires the command and block address within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 20 and 21 illustrate WE# and CE#-controlled write operations.

4 COMMAND DEFINITIONS

When the V_{PP} voltage $\leq V_{PPLK}$, Read operations from the status register, identifier codes, query, or blocks are enabled. Placing V_{PPH1} on V_{PP} enables successful block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

Table 3. Bus Operations(BYTE#=V_{IH})

| Mode | Notes | RP# | CE ₀ # | CE ₁ # | OE# | WE# | Address | V _{PP} | DQ ₀₋₁₅ | STS |
|-----------------------|---------|-----------------|---|---|-----------------|-----------------|----------------|-----------------|--------------------|--------|
| Read | 1,2,3,9 | V _{IH} | V _{IL} | V _{IL} | V _{IL} | V _{IH} | X | X | D _{OUT} | X |
| Output Disable | 3 | V _{IH} | V _{IL} | V _{IL} | V _{IH} | V _{IH} | X | X | High Z | X |
| Standby | 3 | V _{IH} | V _{IH} V _{IH} V _{IL} | V _{IH} V _{IL} V _{IH} | X | X | X | X | High Z | X |
| Deep Power-Down | 4 | V _{IL} | X | X | X | X | X | X | High Z | High Z |
| Read Identifier Codes | 9 | V _{IH} | V _{IL} | V _{IL} | V _{IL} | V _{IH} | See Figure 5 | X | Note 5 | High Z |
| Query | 9 | V _{IH} | V _{IL} | V _{IL} | V _{IL} | V _{IH} | See Table 7-11 | X | Note 6 | High Z |
| Write | 3,7,8,9 | V _{IH} | V _{IL} | V _{IL} | V _{IH} | V _{IL} | X | X | D _{IN} | X |

Table 3.1. Bus Operations(BYTE#=V_{IL})

| Mode | Notes | RP# | CE ₀ # | CE ₁ # | OE# | WE# | Address | V _{PP} | DQ ₀₋₇ | STS |
|-----------------------|---------|-----------------|---|---|-----------------|-----------------|----------------|-----------------|-------------------|--------|
| Read | 1,2,3,9 | V _{IH} | V _{IL} | V _{IL} | V _{IL} | V _{IH} | X | X | D _{OUT} | X |
| Output Disable | 3 | V _{IH} | V _{IL} | V _{IL} | V _{IH} | V _{IH} | X | X | High Z | X |
| Standby | 3 | V _{IH} | V _{IH} V _{IH} V _{IL} | V _{IH} V _{IL} V _{IH} | X | X | X | X | High Z | X |
| Deep Power-Down | 4 | V _{IL} | X | X | X | X | X | X | High Z | High Z |
| Read Identifier Codes | 9 | V _{IH} | V _{IL} | V _{IL} | V _{IL} | V _{IH} | See Figure 5 | X | Note 5 | High Z |
| Query | 9 | V _{IH} | V _{IL} | V _{IL} | V _{IL} | V _{IH} | See Table 7-11 | X | Note 6 | High Z |
| Write | 3,7,8,9 | V _{IH} | V _{IL} | V _{IL} | V _{IH} | V _{IL} | X | X | D _{IN} | X |

NOTES:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH1} for V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH1} voltages.
3. STS is V_{OL} (if configured to RY/BY# mode) when the WSM is executing internal block erase, full chip erase, (multi) word/byte write or block lock-bit configuration algorithms. It is floated during when the WSM is not busy, in block erase suspend mode with (multi) word/byte write inactive, (multi) word/byte write suspend mode, or deep power-down mode.
4. RP# at GND±0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. See Section 4.5 for query data.
7. Command writes involving block erase, full chip erase, (multi) word/byte write or block lock-bit configuration are reliably executed when $V_{PP} = V_{PPH1}$ and $V_{CC} = V_{CC1/2}$.
8. Refer to Table 4 for valid D_{IN} during a write operation.
9. Don't use the timing both OE# and WE# are V_{IL}.

Table 4. Command Definitions⁽¹⁰⁾

| Command | Bus Cycles Req'd | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|--|------------------|-------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| | | | Oper ⁽¹⁾ | Addr ⁽²⁾ | Data ⁽³⁾ | Oper ⁽¹⁾ | Addr ⁽²⁾ | Data ⁽³⁾ |
| Read Array/Reset | 1 | | Write | X | FFH | | | |
| Read Identifier Codes | ≥2 | 4 | Write | X | 90H | Read | IA | ID |
| Query | ≥2 | | Write | X | 98H | Read | QA | QD |
| Read Status Register | 2 | | Write | X | 70H | Read | X | SRD |
| Clear Status Register | 1 | | Write | X | 50H | | | |
| Block Erase Setup/Confirm | 2 | 5 | Write | BA | 20H | Write | BA | D0H |
| Full Chip Erase Setup/Confirm | 2 | | Write | X | 30H | Write | X | D0H |
| Word/Byte Write Setup/Write | 2 | 5,6 | Write | WA | 40H | Write | WA | WD |
| Alternate Word/Byte Write Setup/Write | 2 | 5,6 | Write | WA | 10H | Write | WA | WD |
| Multi Word/Byte Write Setup/Confirm | ≥4 | 9 | Write | WA | E8H | Write | WA | N |
| Block Erase and (Multi) Word/byte Write Suspend | 1 | 5 | Write | X | B0H | | | |
| Confirm and Block Erase and (Multi) Word/byte Write Resume | 1 | 5 | Write | X | D0H | | | |
| Block Lock-Bit Set Setup/Confirm | 2 | 7 | Write | BA | 60H | Write | BA | 01H |
| Block Lock-Bit Reset Setup/Confirm | 2 | 8 | Write | X | 60H | Write | X | D0H |
| STS Configuration Level-Mode for Erase and Write (RY/BY# Mode) | 2 | | Write | X | B8H | Write | X | 00H |
| STS Configuration Pulse-Mode for Erase | 2 | | Write | X | B8H | Write | X | 01H |
| STS Configuration Pulse-Mode for Write | 2 | | Write | X | B8H | Write | X | 02H |
| STS Configuration Pulse-Mode for Erase and Write | 2 | | Write | X | B8H | Write | X | 03H |

NOTES:

- BUS operations are defined in Table 3 and Table 3.1.
- X=Any valid address within the device.
IA=Identifier Code Address: see Figure 5.
QA=Query Offset Address.
BA=Address within the block being erased or locked.
WA=Address of memory location to be written.
- SRD=Data read from status register. See Table 14 for a description of the status register bits.
WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
ID=Data read from identifier codes.
QD=Data read from query database.
- Following the Read Identifier Codes command, read operations access manufacturer, device and block status codes. See Section 4.2 for read identifier code data.
- If the block is locked, WP# must be at V_{IH} to enable block erase or (multi) word/byte write operations. Attempts to issue a block erase or (multi) word/byte write to a locked block while RP# is V_{IH}.
- Either 40H or 10H are recognized by the WSM as the byte write setup.
- A block lock-bit can be set while WP# is V_{IH}.
- WP# must be at V_{IH} to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits.
- Following the Third Bus Cycle, inputs the write address and write data of 'N'+1 times. Finally, input the confirm command 'D0H'.
- Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend and (Multi) Word/byte Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and $RP\#$ must be V_{IH} .

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 5 retrieve the manufacturer, device, block lock configuration and block erase status (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and $RP\#$ must be V_{IH} . Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

| Code | Address A20-A0 | Data |
|--|--|--------------------|
| Manufacture Code | 000000 000001 | B0 |
| Device Code | 000002 000003 | D4 |
| Block Status Code | X0004 ⁽¹⁾ X0005 ⁽¹⁾ | |
| •Block is Unlocked | | DQ ₀ =0 |
| •Block is Locked | | DQ ₀ =1 |
| •Last erase operation completed successfully | | DQ ₁ =0 |
| •Last erase operation did not completed successfully | | DQ ₁ =1 |
| •Reserved for Future Use | | DQ ₂₋₇ |

NOTE:

1. X selects the specific block status code to be read. See Figure 5 for the device identifier code memory map.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration is complete and whether the operation completed successfully(see Table 14). It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#(Either CE₀# or CE₁#), whichever occurs. OE# or CE#(Either CE₀# or CE₁#) must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. $RP\#$ must be V_{IH} .

The extended status register may be read to determine multi byte write availability(see Table 14.1). The extended status register may be read at any time by writing the Multi Byte Write command. After writing this command, all subsequent read operations output data from the extended status register, until another valid command is written. The contents of the extended status register are latched on the falling edge of OE# or CE#(Either CE₀# or CE₁#), whichever occurs last in the read cycle. Multi Byte Write command must be re-issued to update the extended status register latch.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 14). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurs during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} Voltage. $RP\#$ must be V_{IH} . This command is not functional during block erase, full chip erase, (multi) word/byte write block lock-bit configuration, block erase suspend or (multi) word/byte write suspend modes.

4.5 Query Command

Query database can be read by writing Query command (98H). Following the command write, read cycle from address shown in Table 7-11 retrieve the critical information to write, erase and otherwise control the flash component. A_0 of query offset address is ignored when X8 mode (BYTE#=V_{IL}).

Query data are always presented on the low-byte data output (DQ₀-DQ₇). In x16 mode, high-byte (DQ₈-DQ₁₅) outputs 00H. The bytes not assigned to any information or reserved for future use are set to "0". This command functions independently of the V_{PP} voltage. RP# must be V_{IH}.

Table 6. Example of Query Structure Output

| Mode | Offset Address | Output | |
|----------|---|--------------------|-------------------|
| | | DQ ₁₅₋₈ | DQ ₇₋₀ |
| X8 mode | A ₅ , A ₄ , A ₃ , A ₂ , A ₁ , A ₀ 1, 0, 0, 0, 0, 0 (20H) | High-Z | "Q" |
| | 1, 0, 0, 0, 0, 1 (21H) | High-Z | "Q" |
| | 1, 0, 0, 0, 1, 0 (22H) | High-Z | "R" |
| | 1, 0, 0, 0, 1, 1 (23H) | High-Z | "R" |
| X16 mode | A ₅ , A ₄ , A ₃ , A ₂ , A ₁ 1, 0, 0, 0, 0 (10H) | 00H | "Q" |
| | 1, 0, 0, 0, 1 (11H) | 00H | "R" |

4.5.1 Block Status Register

This field provides lock configuration and erase status for the specified block. These informations are only available when device is ready (SR.7=1). If block erase or full chip erase operation is finished irregularly, block erase status bit will be set to "1". If bit 1 is "1", this block is invalid.

Table 7. Query Block Status Register

| Offset (Word Address) | Length | Description |
|-----------------------|--------|---|
| (BA+2)H | 01H | Block Status Register bit0 Block Lock Configuration 0=Block is unlocked 1=Block is Locked bit1 Block Erase Status 0=Last erase operation completed successfully 1=Last erase operation not completed successfully bit2-7 reserved for future use |

Note:

1. BA=The beginning of a Block Address.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

4.5.2 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version of the spec and which Vendor-specified command set(s) is(are) supported.

Table 8. CFI Query Identification String

| Offset (Word Address) | Length | Description |
|--------------------------|--------|--|
| 10H,11H,12H | 03H | Query Unique ASCII string "QRY" 51H,52H,59H |
| 13H,14H | 02H | Primary Vendor Command Set and Control Interface ID Code 01H,00H (SCS ID Code) |
| 15H,16H | 02H | Address for Primary Algorithm Extended Query Table 31H,00H (SCS Extended Query Table Offset) |
| 17H,18H | 02H | Alternate Vendor Command Set and Control Interface ID Code 0000H (0000H means that no alternate exists) |
| 19H,1AH | 02H | Address for Alternate Algorithm Extended Query Table 0000H (0000H means that no alternate exists) |

4.5.3 System Interface Information

The following device information can be useful in optimizing system interface software.

Table 9. System Information String

| Offset (Word Address) | Length | Description |
|--------------------------|--------|---|
| 1BH | 01H | V _{CC} Logic Supply Minimum Write/Erase voltage 45H (4.5V) |
| 1CH | 01H | V _{CC} Logic Supply Maximum Write/Erase voltage 55H (5.5V) |
| 1DH | 01H | V _{PP} Programming Supply Minimum Write/Erase voltage 45H (4.5V) |
| 1EH | 01H | V _{PP} Programming Supply Maximum Write/Erase voltage 55H (5.5V) |
| 1FH | 01H | Typical Timeout per Single Byte/Word Write 04H (2 ⁴ =16 μsec) |
| 20H | 01H | Typical Timeout for Maximum Size Buffer Write (32 Bytes) 06H (2 ⁶ =64 μsec) |
| 21H | 01H | Typical Timeout per Individual Block Erase 09H (09H=9, 2 ⁹ =512 msec) |
| 22H | 01H | Typical Timeout for Full Chip Erase 0FH (0FH=15, 2 ¹⁵ =32768 msec) |
| 23H | 01H | Maximum Timeout per Single Byte/Word Write, 2 ^N times of typical. 04H (2 ⁴ =16, 8 μsecx16=512 μsec) |
| 24H | 01H | Maximum Timeout Maximum Size Buffer Write, 2 ^N times of typical. 04H (2 ⁴ =16, 64 μsecx16=4096 μsec) |
| 25H | 01H | Maximum Timeout per Individual Block Erase, 2 ^N times of typical. 04H (2 ⁴ =16, 1024 msecx16=16384 msec) |
| 26H | 01H | Maximum Timeout for Full Chip Erase, 2 ^N times of typical. 04H (2 ⁴ =16, 32768msecx16=524288 msec) |

4.5.4 Device Geometry Definition

This field provides critical details of the flash device geometry.

Table 10. Device Geometry Definition

| Offset (Word Address) | Length | Description |
|--------------------------|--------|--|
| 27H | 01H | Device Size 16H (16H=22, 2 ²² =4194304=4M Bytes) |
| 28H,29H | 02H | Flash Device Interface description 02H,00H (x8/x16 supports x8 and x16 via BYTE#) |
| 2AH,2BH | 02H | Maximum Number of Bytes in Multi-byte 05H,00H (2 ⁵ =32 Bytes) |
| 2CH | 01H | Number of Erase Block Regions within device 01H (symmetrically blocked) |
| 2DH,2EH | 02H | The Number of Erase Blocks 3FH,00H (3FH=63 ==> 63+1=64 Blocks) |
| 2FH,30H | 02H | The Number of "256 Bytes" cluster in a Erase block 00H,01H (0100H=256 ==>256 Bytes x 256= 64K Bytes in a Erase Block) |

4.5.5 SCS OEM Specific Extended Query Table

Certain flash features and commands may be optional in a vendor-specific algorithm specification. The optional vendor-specific Query table(s) may be used to specify this and other types of information. These structures are defined solely by the flash vendor(s).

Table 11. SCS OEM Specific Extended Query Table

| Offset (Word Address) | Length | Description |
|--------------------------|----------|--|
| 31H,32H,33H | 03H | PRI 50H,52H,49H |
| 34H | 01H | 31H (1) Major Version Number , ASCII |
| 35H | 01H | 30H (0) Minor Version Number, ASCII |
| 36H,37H, 38H,39H | 04H | 0FH,00H,00H,00H Optional Command Support bit0=1 : Chip Erase Supported bit1=1 : Suspend Erase Supported bit2=1 : Suspend Write Supported bit3=1 : Lock/Unlock Supported bit4=0 : Queued Erase Not Supported bit5-31=0 : reserved for future use |
| 3AH | 01H | 01H Supported Functions after Suspend bit0=1 : Write Supported after Erase Suspend bit1-7=0 : reserved for future use |
| 3BH,3CH | 02H | 03H,00H Block Status Register Mask bit0=1 : Block Status Register Lock Bit [BSR.0] active bit1=1 : Block Status Register Valid Bit [BSR.1] active bit2-15=0 : reserved for future use |
| 3DH | 01H | V _{CC} Logic Supply Optimum Write/Erase voltage(highest performance) 50H(5.0V) |
| 3EH | 01H | V _{PP} Programming Supply Optimum Write/Erase voltage(highest performance) 50H(5.0V) |
| 3FH | reserved | Reserved for future versions of the SCS Specification |

LH28F320S5-L90/12 Smart 5 Flash MEMORY

4.6 Block Erase Command

Block erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect block erase completion by analyzing the output data of the STS pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP}\leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase requires that the corresponding block lock-bit be cleared or if set, that $WP\#=V_{IH}$. If block erase is attempted when the corresponding block lock-bit is set and $WP\#=V_{IL}$, SR.1 and SR.5 will be set to "1".

4.7 Full Chip Erase Command

This command followed by a confirm command (DOH) erases all of the unlocked blocks. A full chip

erase setup is first written, followed by a full chip erase confirm. After a confirm command is written, device erases the all unlocked blocks from block 0 to Block 63 block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect full chip erase completion by analyzing the output data of the STS pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing the block and begin to erase the next block. Reading the block valid status by issuing Read ID Codes command or Query command informs which blocks failed to its erase.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable full chip erasure can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1}$. In the absence of this high voltage, block contents are protected against erasure. If full chip erase is attempted while $V_{PP}\leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". When $WP\#=V_{IH}$, all blocks are erased independent of block lock-bits status. When $WP\#=V_{IL}$, only unlocked blocks are erased. Full chip erase can not be suspended.

4.8 Word/Byte Write Command

Word/byte write is executed by a two-cycle command sequence. Word/Byte Write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect the completion of the word/byte write event by analyzing the STS pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1}$. In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write requires that the corresponding block lock-bit be cleared or, if set, that $WP\#=V_{IH}$. If word/byte write is attempted when the corresponding block lock-bit is set and $WP\#=V_{IL}$, SR.1 and SR.4 will be set to "1". Word/byte write operations with $V_{IL} < WP\# < V_{IH}$ produce spurious results and should not be attempted.

4.9 Multi Word/Byte Write Command

Multi word/byte write is executed by at least four-cycle or up to 35-cycle command sequence. Up to 32 bytes in x8 mode (16 words in x16 mode) can be loaded into the buffer and written to the Flash Array. First, multi word/byte write setup (E8H) is written with the write address. At this point, the device automatically outputs extended status register data (XSR) when read (see Figure 9, 10). If extended status register bit XSR.7 is 0, no Multi Word/Byte Write command is available and multi word/byte write setup which just has been written is ignored. To retry,

continue monitoring XSR.7 by writing multi word/byte write setup with write address until XSR.7 transitions to 1. When XSR.7 transitions to 1, the device is ready for loading the data to the buffer. A word/byte count (N) is written with write address. After writing a word/byte count(N), the device automatically turns back to output status register data. The word/byte count (N) must be less than or equal to 1FH in x8 mode (0FH in x16 mode). On the next write, device start address is written with buffer data. Subsequent writes provide additional device address and data, depending on the count. All subsequent address must lie within the start address plus the count. After the final buffer data is written, write confirm (D0H) must be written. This initiates WSM to begin copying the buffer data to the Flash Array. An invalid Multi Word/Byte Write command sequence will result in both status register bits SR.4 and SR.5 being set to "1". For additional multi word/byte write, write another multi word/byte write setup and check XSR.7. The Multi Word/Byte Write command can be queued while WSM is busy as long as XSR.7 indicates "1", because LH28F320S5-L90/12 has two buffers. If an error occurs while writing, the device will stop writing and flush next multi word/byte write command loaded in multi word/byte write command. Status register bit SR.4 will be set to "1". No multi word/byte write command is available if either SR.4 or SR.5 are set to "1". SR.4 and SR.5 should be cleared before issuing multi word/byte write command. If a multi word/byte write command is attempted past an erase block boundary, the device will write the data to Flash Array up to an erase block boundary and then stop writing. Status register bits SR.4 and SR.5 will be set to "1".

Reliable multi byte writes can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1}$. In the absence of this high voltage, memory contents are protected against multi word/byte writes. If multi word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful multi word/byte write requires that the corresponding block lock-bit be cleared or, if set, that $WP\#=V_{IH}$. If multi byte write is attempted when the corresponding block lock-bit is set and $WP\#=V_{IL}$, SR.1 and SR.4 will be set to "1".

LH28F320S5-L90/12 Smart 5 Flash MEMORY

4.10 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or (multi) word/byte-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). STS will also transition to High-Z. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A (Multi) Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the (Multi) Word/Byte Write Suspend command (see Section 4.11), a (multi) word/byte write operation can also be suspended. During a (multi) word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the STS (if set to RY/BY#) output will transition to V_{OL} . However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and STS will return to V_{OL} . After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 11). V_{PP} must remain at V_{PPH1} (the same V_{PP} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH} . Block erase cannot resume until

(multi) word/byte write operations initiated during block erase suspend have completed.

4.11 (Multi) Word/Byte Write Suspend Command

The (Multi) Word/Byte Write Suspend command allows (multi) word/byte write interruption to read data in other flash memory locations. Once the (multi) word/byte write process starts, writing the (Multi) Word/Byte Write Suspend command requests that the WSM suspend the (multi) word/byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the (Multi) Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the (multi) word/byte write operation has been suspended (both will be set to "1"). STS will also transition to High-Z. Specification t_{WHRH1} defines the (multi) word/byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while (multi) word/byte write is suspended are Read Status Register and (Multi) Word/Byte Write Resume. After (Multi) Word/Byte Write Resume command is written to the flash memory, the WSM will continue the (multi) word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and STS will return to V_{OL} . After the (Multi) Word/Byte Write command is written, the device automatically outputs status register data when read (see Figure 12). V_{PP} must remain at V_{PPH1} (the same V_{PP} level used for (multi) word/byte write) while in (multi) word/byte write suspend mode. WP# must also remain at V_{IH} or V_{IL} .

4.12 Set Block Lock-Bit Command

A flexible block locking and unlocking scheme is enabled via block lock-bits. The block lock-bits gate program and erase operations. With $WP\#=V_{IH}$, individual block lock-bits can be set using the Set Block Lock-Bit command. See Table 13 for a summary of hardware and software write protection options.

Set block lock-bit is executed by a two-cycle command sequence. The set block lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked). The WSM then controls the set block lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 13). The CPU can detect the completion of the set block lock-bit event by analyzing the STS pin output or status register bit SR.7.

When the set block lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1}$. In the absence of this high voltage, block lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires $WP\#=V_{IH}$. If it is attempted with $WP\#=V_{IL}$, SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations with $WP\#<V_{IH}$ produce spurious results and should not be attempted.

4.13 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With $WP\#=V_{IH}$,

block lock-bits can be cleared using only the Clear Block Lock-Bits command. See Table 13 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 14). The CPU can detect completion of the clear block lock-bits event by analyzing the STS Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1}$. If a clear block lock-bits operation is attempted while $V_{PP}\leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires $WP\#=V_{IH}$. If it is attempted with $WP\#=V_{IL}$, SR.1 and SR.5 will be set to "1" and the operation will fail. Clear block lock-bits operations with $V_{IH}<RP\#$ produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{CC} transitioning out of valid range or $RP\#$ active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

4.14 STS Configuration Command

The Status (STS) pin can be configured to different states using the STS Configuration command. Once the STS pin has been configured, it remains in that configuration until another configuration command is issued, the device is powered down or RP# is set to V_{IL} . Upon initial device power-up and after exit from deep power-down mode, the STS pin defaults to RY/BY# operation where STS low indicates that the WSM is busy. STS High Z indicates that the WSM is ready for a new operation.

To reconfigure the STS pin to other modes, the STS Configuration is issued followed by the appropriate configuration code. The three alternate configurations are all pulse mode for use as a system interrupt. The STS Configuration command functions independently of the V_{pp} voltage and RP# must be V_{IH} .

Table 12. STS Configuration Coding Description

| Configuration Bits | Effects |
|--------------------|--|
| 00H | Set STS pin to default level mode (RY/BY#). RY/BY# in the default level-mode of operation will indicate WSM status condition. |
| 01H | Set STS pin to pulsed output signal for specific erase operation. In this mode, STS provides low pulse at the completion of Block Erase, Full Chip Erase and Clear Block Lock-bits operations. |
| 02H | Set STS pin to pulsed output signal for a specific write operation. In this mode, STS provides low pulse at the completion of (Multi) Byte Write and Set Block Lock-bit operation. |
| 03H | Set STS pin to pulsed output signal for specific write and erase operation. STS provides low pulse at the completion of Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-bit Configuration operations. |

Table 13. Write Protection Alternatives

| Operation | Block Lock-Bit | WP# | Effect |
|--|----------------|----------------------|--|
| Block Erase, (Multi) Word/Byte Write | 0 | V_{IL} or V_{IH} | Block Erase and (Multi) Word/Byte Write Enabled |
| | 1 | V_{IL} | Block is Locked. Block Erase and (Multi) Word/Byte Write Disabled |
| | | V_{IH} | Block Lock-Bit Override. Block Erase and (Multi) Word/Byte Write Enabled |
| Full Chip Erase | 0,1 | V_{IL} | All unlocked blocks are erased, locked blocks are not erased |
| | X | V_{IH} | All blocks are erased |
| Set Block Lock-Bit | X | V_{IL} | Set Block Lock-Bit Disabled |
| | | V_{IH} | Set Block Lock-Bit Enabled |
| Clear Block Lock-Bits | X | V_{IL} | Clear Block Lock-Bits Disabled |
| | | V_{IH} | Clear Block Lock-Bits Enabled |

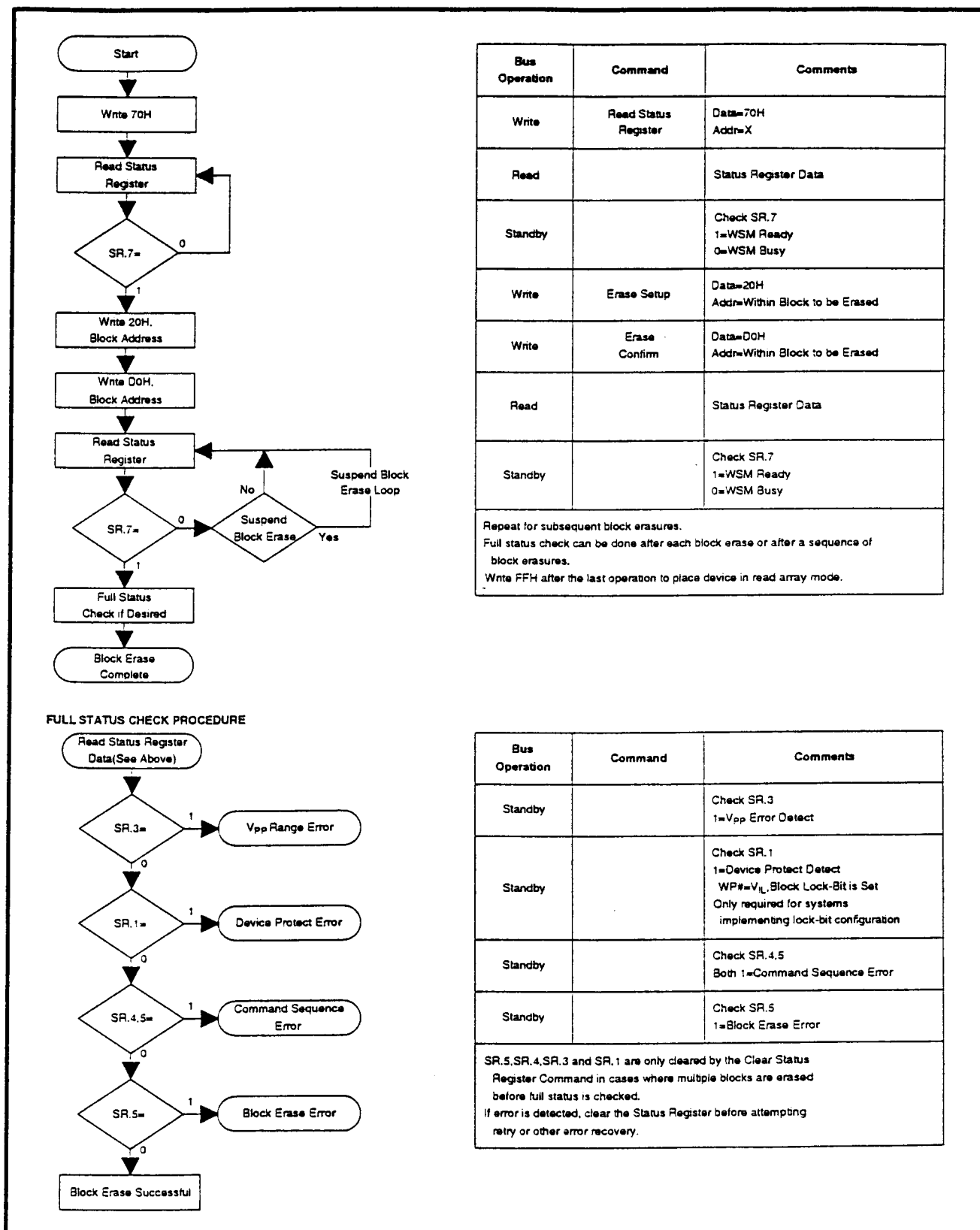
Table 14. Status Register Definition

| WSMS | BESS | ECBLBS | WSBLBS | VPPS | WSS | DPS | R |
|--|------|--------|--------|--|-----|-----|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <p>SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy</p> <p>SR.6 = BLOCK ERASE SUSPEND STATUS 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS 1 = Error in Erase or Clear Block Lock-Bits 0 = Successful Erase or Clear Block Lock-Bits</p> <p>SR.4 = WRITE AND SET BLOCK LOCK-BIT STATUS 1 = Error in Write or Set Block Lock-Bit 0 = Successful Write or Set Block Lock-Bit</p> <p>SR.3 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK</p> <p>SR.2 = WRITE SUSPEND STATUS 1 = Write Suspended 0 = Write in Progress/Completed</p> <p>SR.1 = DEVICE PROTECT STATUS 1 = Block Lock-Bit and/or WP# Lock Detected, Operation Abort 0 = Unlock</p> <p>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS</p> | | | | <p>NOTES:</p> <p>Check STS or SR.7 to determine block erase, full chip erase, (multi) word/byte write or block lock-bit configuration completion. SR.6-0 are invalid while SR.7="0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (multi) word/byte write, block lock-bit configuration or STS configuration attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when V_{PP}≠V_{PPH1}.</p> <p>SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates block lock-bit, and WP# only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set and/or WP# is not V_{IH}. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock-bit status.</p> <p>SR.0 is reserved for future use and should be masked out when polling the status register.</p> | | | |

Table 14.1. Extended Status Register Definition

| SMS | R | R | R | R | R | R | R |
|---|---|---|---|--|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <p>XSR.7 = STATE MACHINE STATUS 1 = Multi Word/Byte Write available 0 = Multi Word/Byte Write not available</p> <p>XSR.6-0=RESERVED FOR FUTURE ENHANCEMENTS</p> | | | | <p>NOTES:</p> <p>After issue a Multi Word/Byte Write command: XSR.7 indicates that a next Multi Word/Byte Write command is available.</p> <p>XSR.6-0 is reserved for future use and should be masked out when polling the extended status register.</p> | | | |

LH28F320S5-L90/12 Smart 5 Flash MEMORY



| Bus Operation | Command | Comments |
|---------------|----------------------|--|
| Write | Read Status Register | Data=70H Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7 1=WSM Ready 0=WSM Busy |
| Write | Erase Setup | Data=20H Addr=Within Block to be Erased |
| Write | Erase Confirm | Data=D0H Addr=Within Block to be Erased |
| Read | | Status Register Data |
| Standby | | Check SR.7 1=WSM Ready 0=WSM Busy |

Repeat for subsequent block erasures.
Full status check can be done after each block erase or after a sequence of block erasures.
Write FFH after the last operation to place device in read array mode.

| Bus Operation | Command | Comments |
|---------------|---------|---|
| Standby | | Check SR.3 1=V _{pp} Error Detect |
| Standby | | Check SR.1 1=Device Protect Detect WP# = V _{pp} Block Lock-Bit is Set Only required for systems implementing lock-bit configuration |
| Standby | | Check SR.4.5 Both 1=Command Sequence Error |
| Standby | | Check SR.5 1=Block Erase Error |

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 6. Automated Block Erase Flowchart

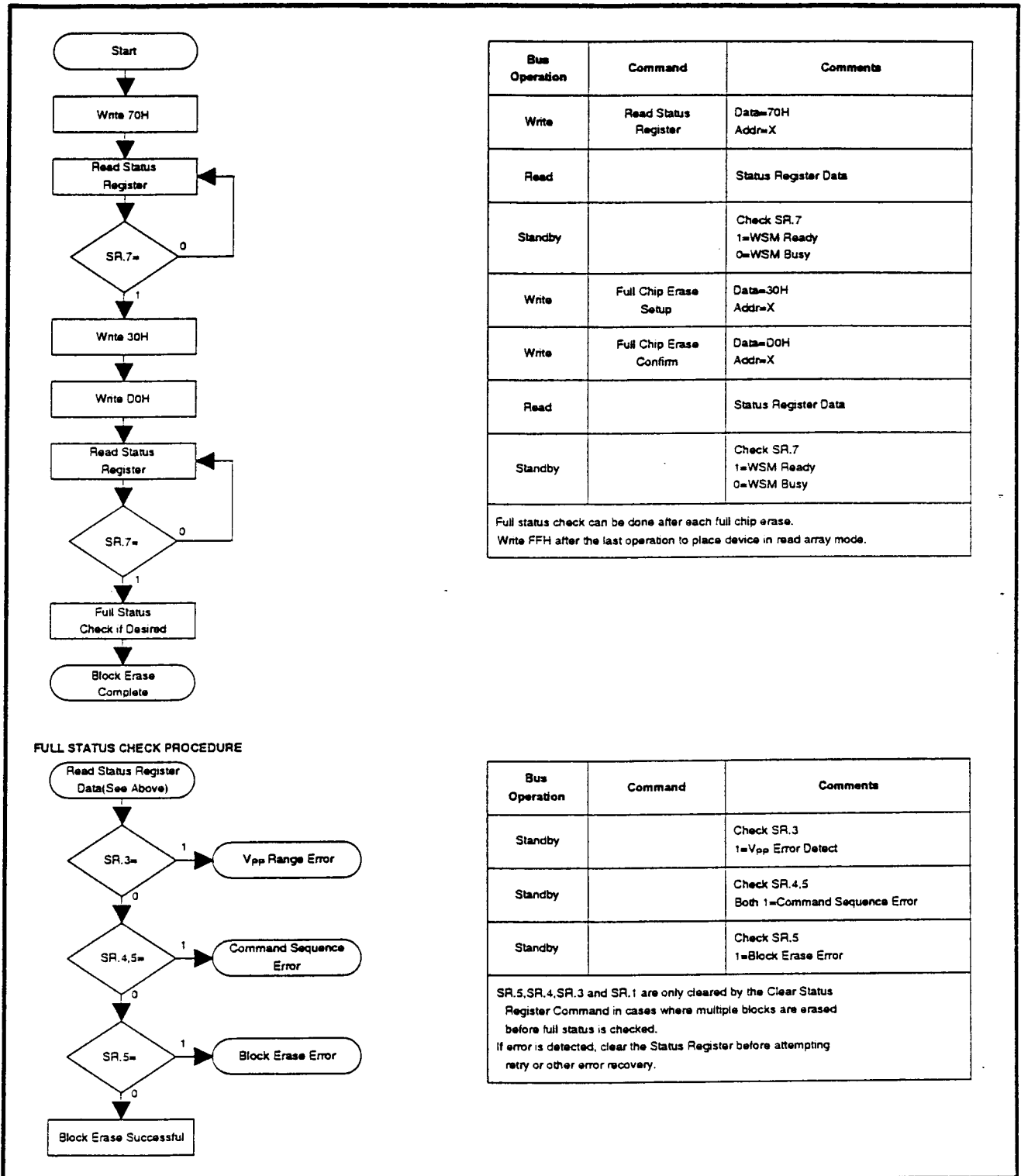
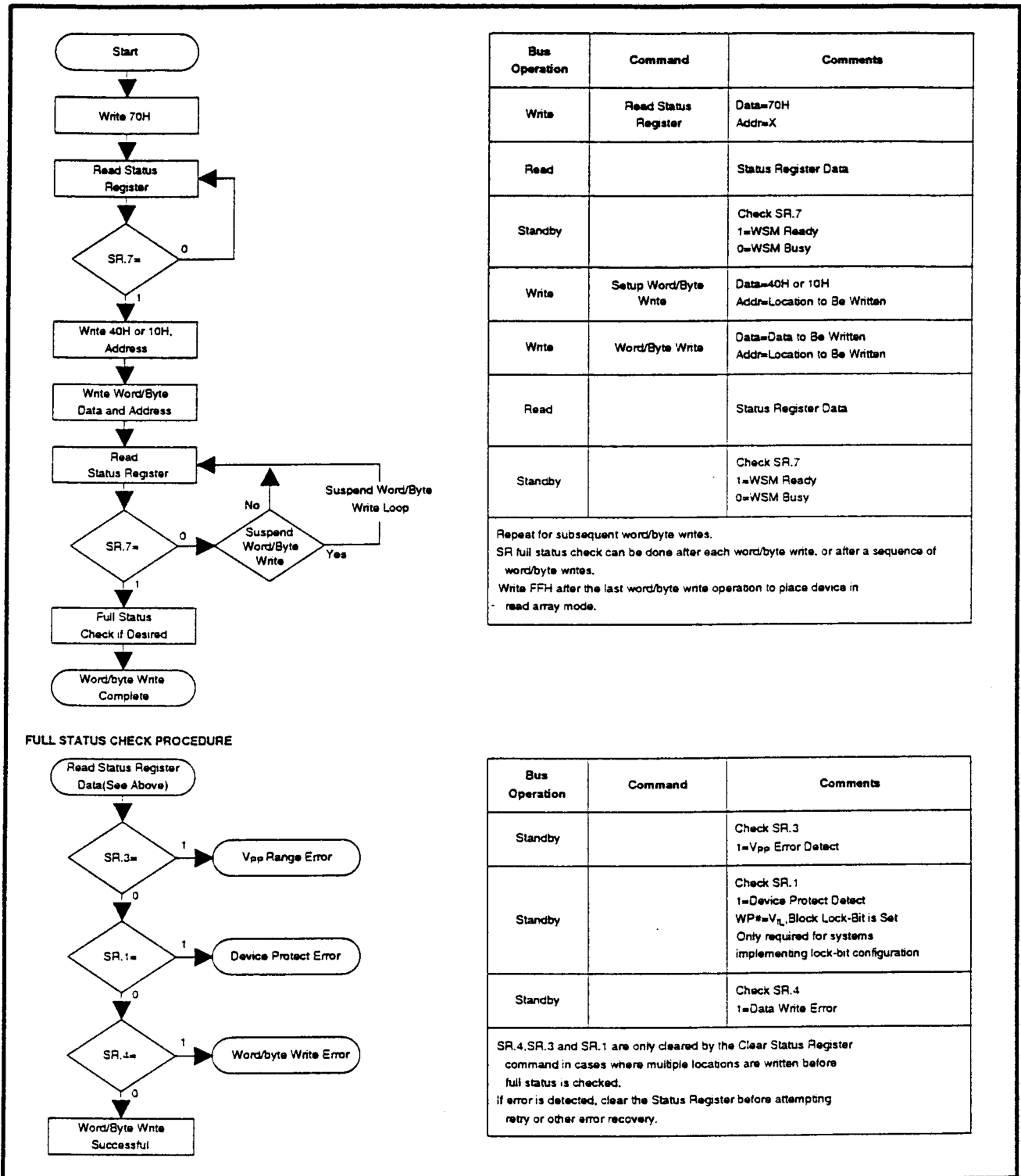


Figure 7. Automated Full Chip Erase Flowchart

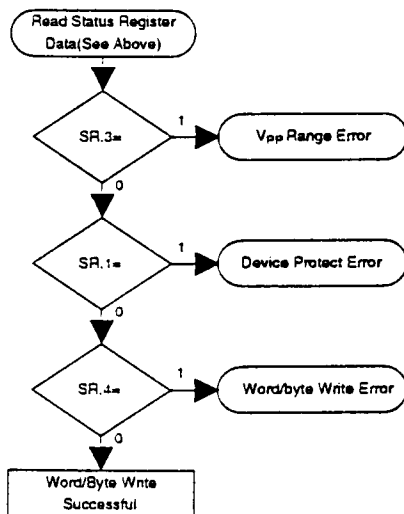
LH28F320S5-L90/12 Smart 5 Flash MEMORY



| Bus Operation | Command | Comments |
|---------------|-----------------------|--|
| Write | Read Status Register | Data=70H Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7 1=WSM Ready 0=WSM Busy |
| Write | Setup Word/Byte Write | Data=40H or 10H Addr=Location to Be Written |
| Write | Word/Byte Write | Data=Data to Be Written Addr=Location to Be Written |
| Read | | Status Register Data |
| Standby | | Check SR.7 1=WSM Ready 0=WSM Busy |

Repeat for subsequent word/byte writes.
 SR full status check can be done after each word/byte write, or after a sequence of word/byte writes.
 Write FFH after the last word/byte write operation to place device in read array mode.

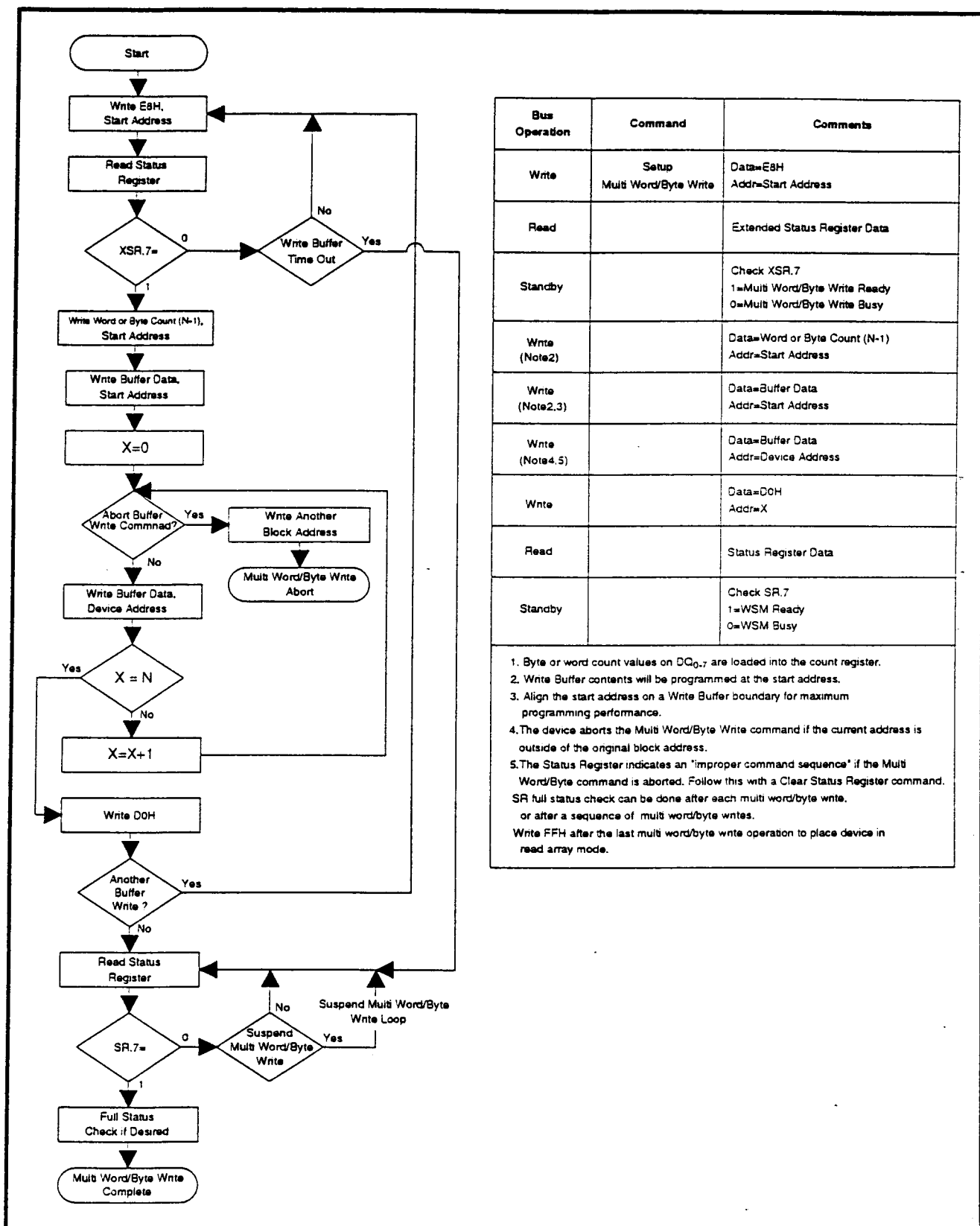
FULL STATUS CHECK PROCEDURE



| Bus Operation | Command | Comments |
|---------------|---------|---|
| Standby | | Check SR.3 1=Vpp Error Detect |
| Standby | | Check SR.1 1=Device Protect Detect WP# = V _{pp} Block Lock-Bit is Set Only required for systems implementing lock-bit configuration |
| Standby | | Check SR.4 1=Data Write Error |

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
 If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 8. Automated Word/byte Write Flowchart



| Bus Operation | Command | Comments |
|-----------------|-----------------------------|--|
| Write | Setup Multi Word/Byte Write | Data=E8H Addr=Start Address |
| Read | | Extended Status Register Data |
| Standby | | Check XSR.7 1=Multi Word/Byte Write Ready 0=Multi Word/Byte Write Busy |
| Write (Note2) | | Data=Word or Byte Count (N-1) Addr=Start Address |
| Write (Note2,3) | | Data=Buffer Data Addr=Start Address |
| Write (Note4,5) | | Data=Buffer Data Addr=Device Address |
| Write | | Data=D0H Addr=X |
| Read | | Status Register Data |
| Standby | | Check SR.7 1=WSM Ready 0=WSM Busy |

1. Byte or word count values on DC_{0,7} are loaded into the count register.
 2. Write Buffer contents will be programmed at the start address.
 3. Align the start address on a Write Buffer boundary for maximum programming performance.
 4. The device aborts the Multi Word/Byte Write command if the current address is outside of the original block address.
 5. The Status Register indicates an 'improper command sequence' if the Multi Word/Byte command is aborted. Follow this with a Clear Status Register command. SR full status check can be done after each multi word/byte write, or after a sequence of multi word/byte writes.
- Write FFH after the last multi word/byte write operation to place device in read array mode.

Figure 9. Automated Multi Word/Byte Write Flowchart

LH28F320S5-L90/12 Smart 5 Flash MEMORY

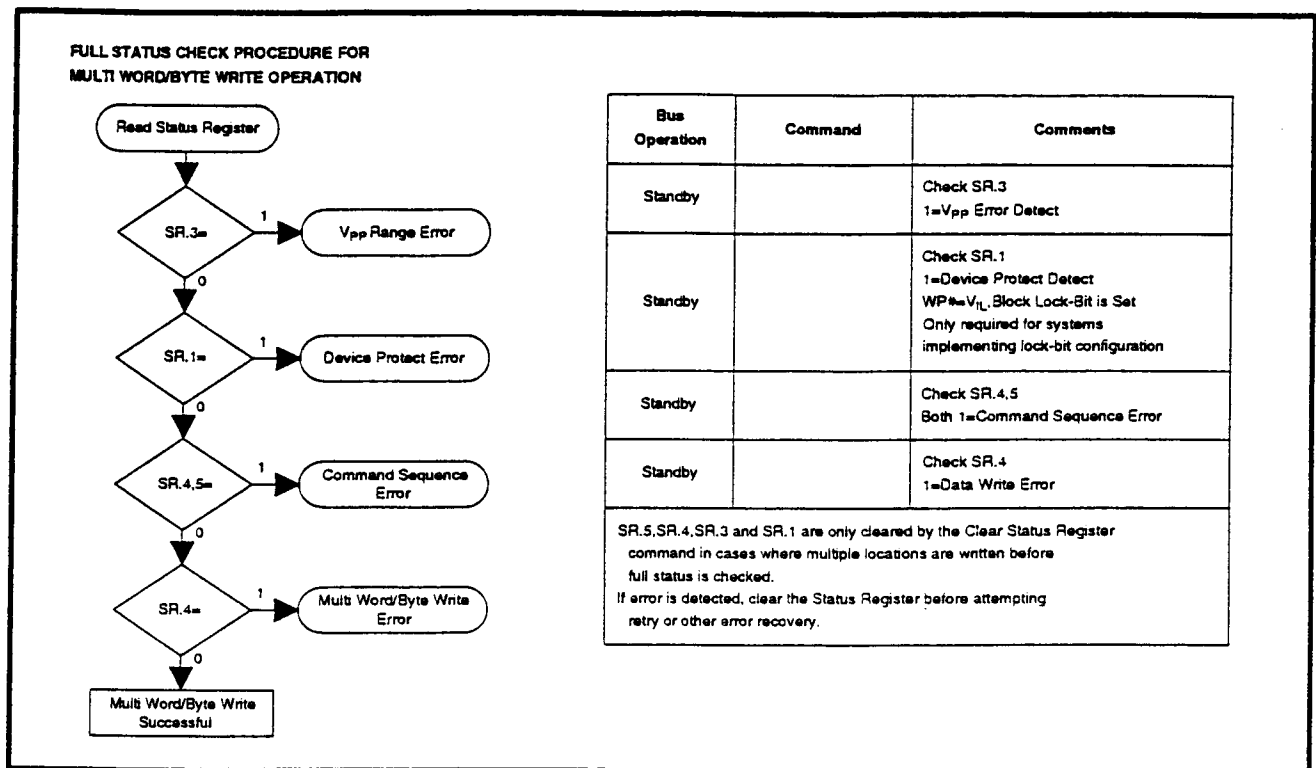


Figure 10. Full Status Check Procedure for Automated Multi Word/Byte Write

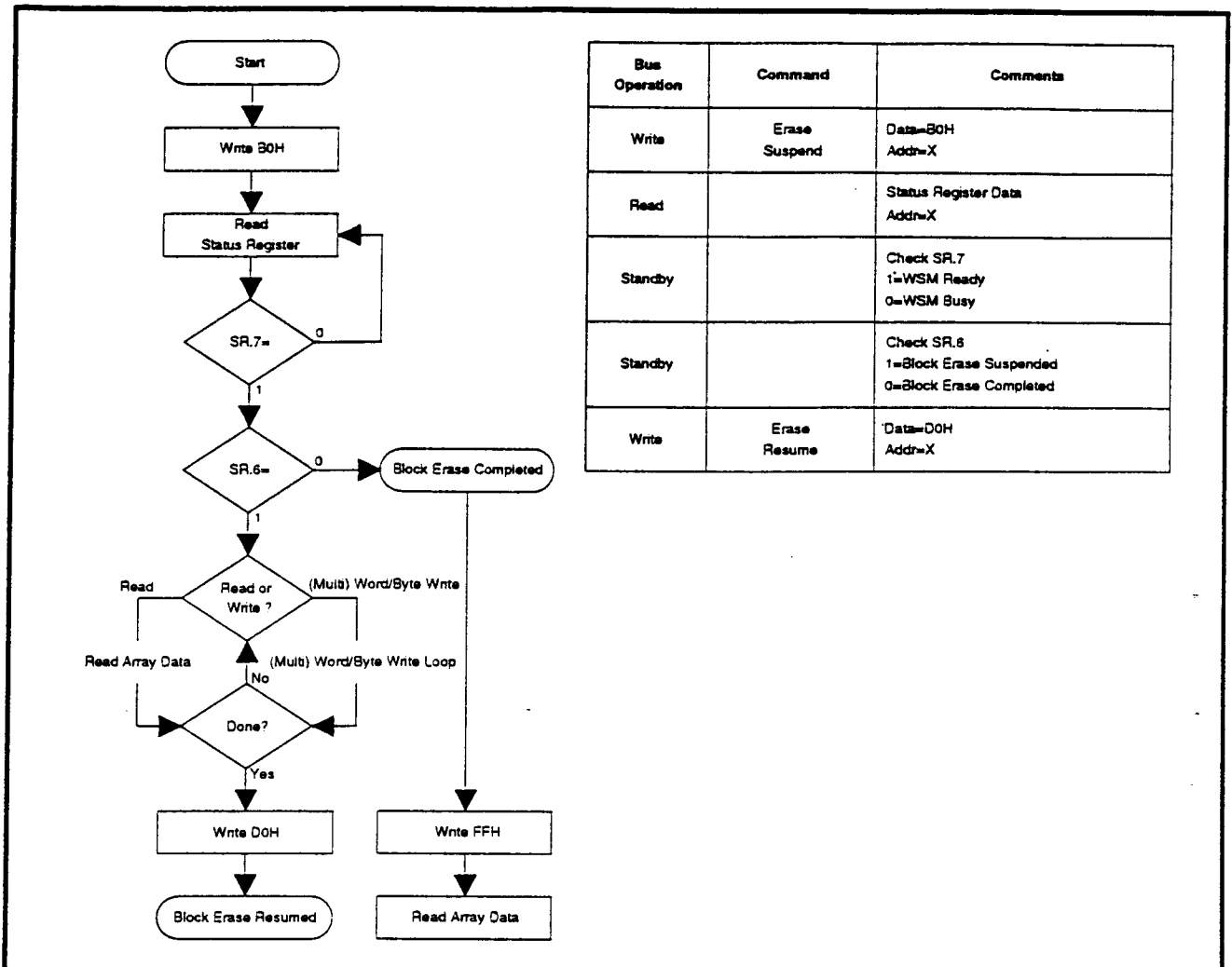


Figure 11. Block Erase Suspend/Resume Flowchart

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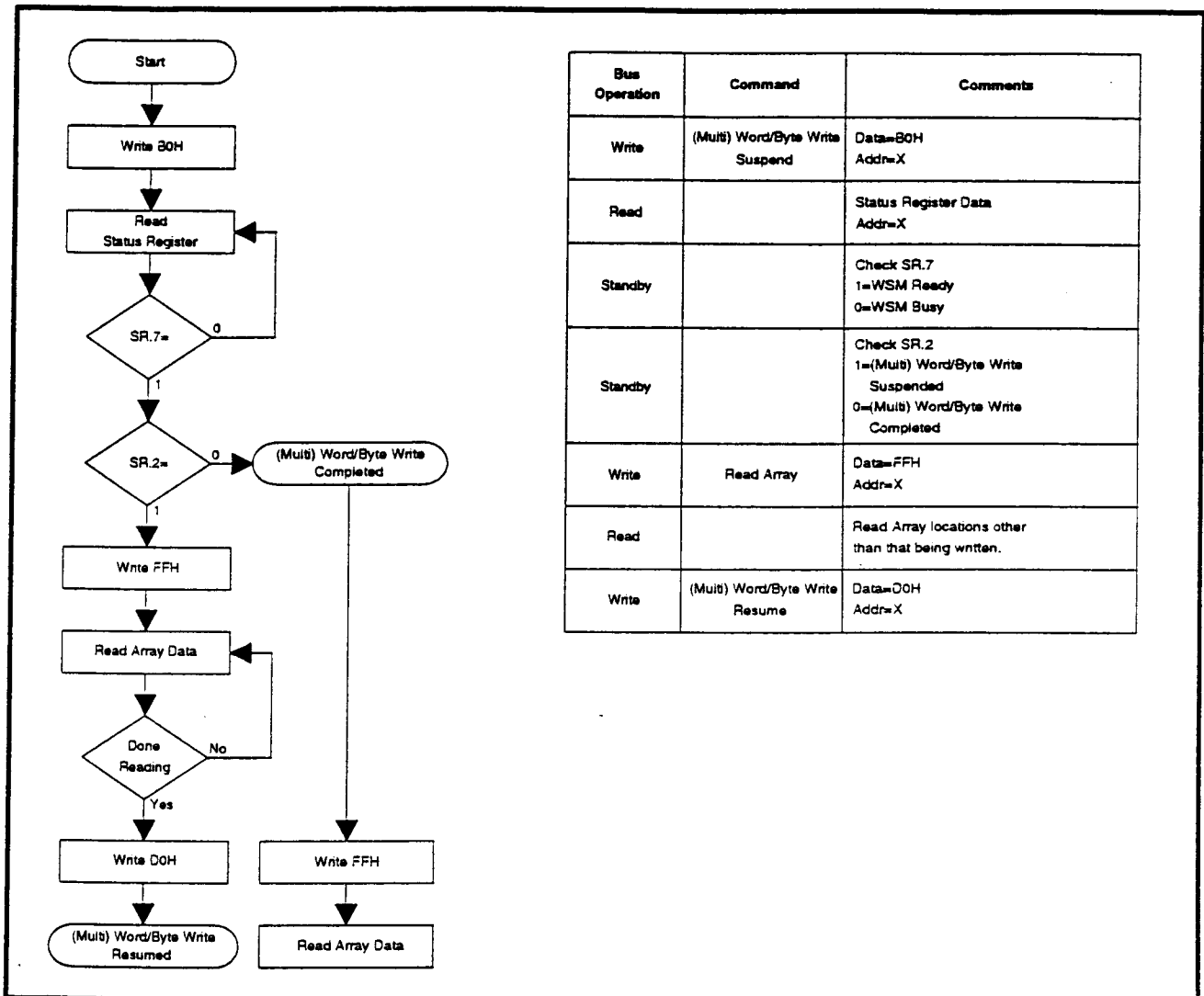


Figure 12. (Multi) Word/Byte Write Suspend/Resume Flowchart

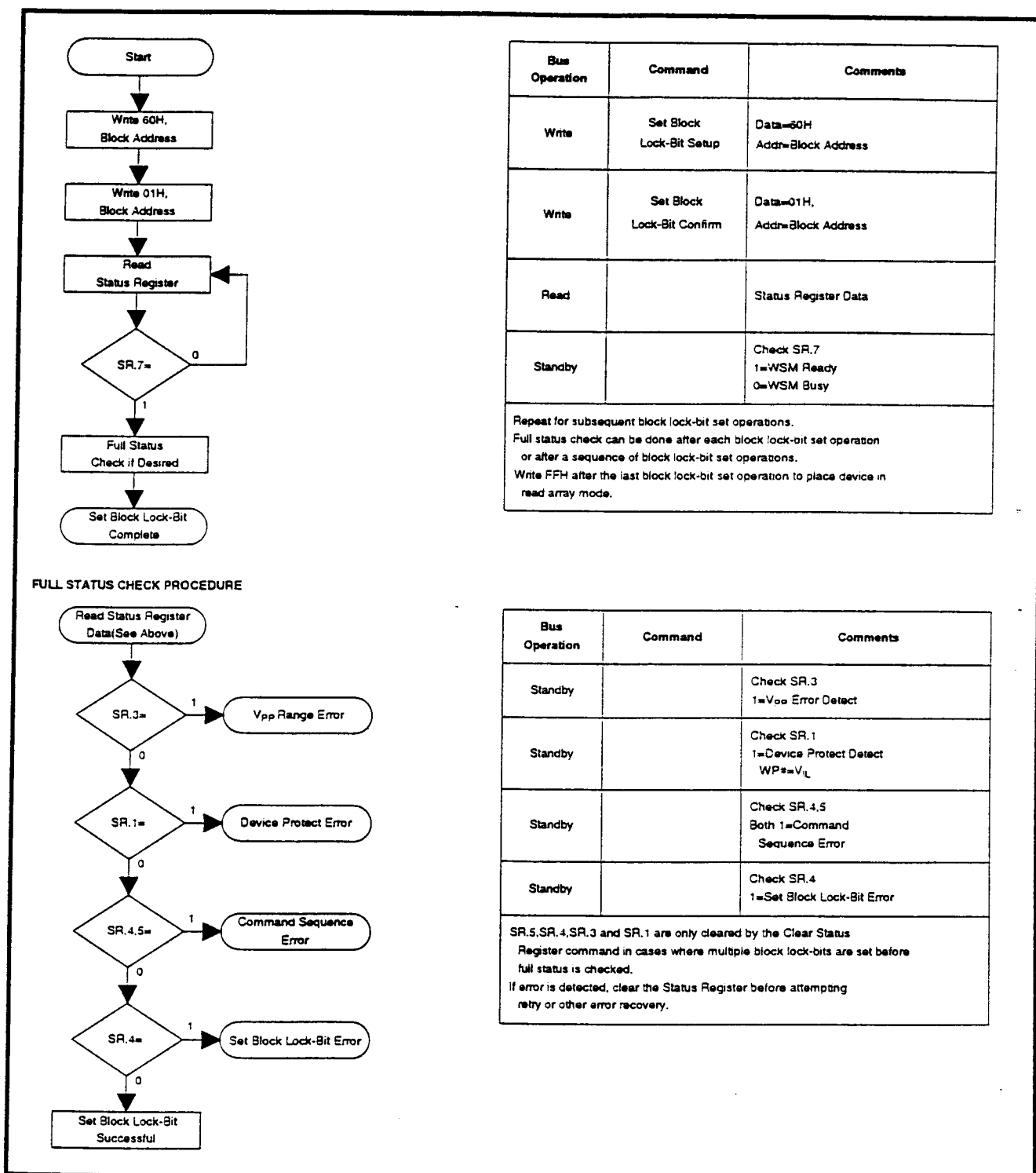


Figure 13. Set Block Lock-Bit Flowchart

LH28F320S5-L90/12 Smart 5 Flash MEMORY

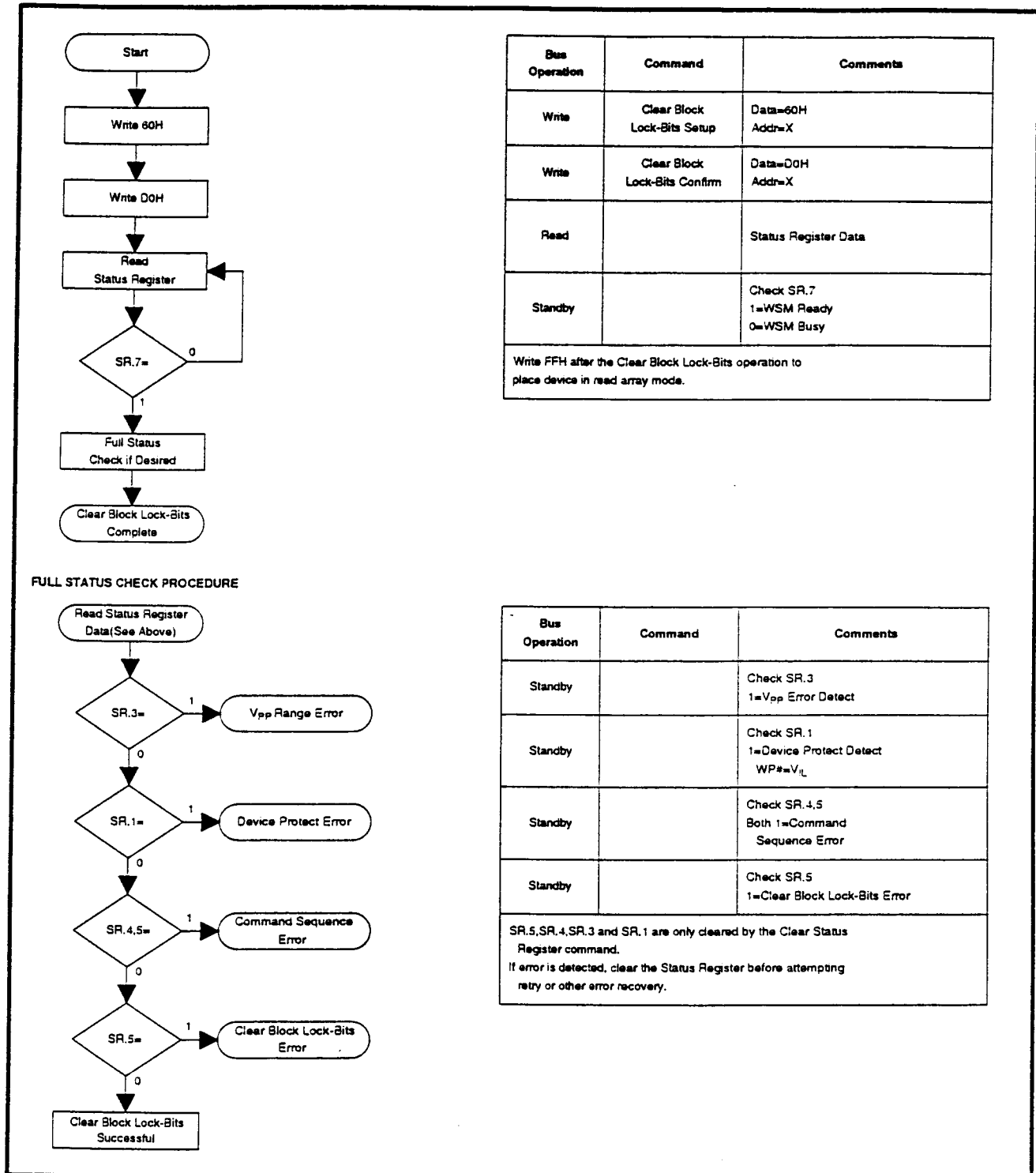


Figure 14. Clear Block Lock-Bits Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-Line control provides for:

- a. Lowest possible memory power dissipation.
- b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 STS and Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration Polling

STS is an open drain output that should be connected to V_{CC} by a pullup resistor to provide a hardware method of detecting block erase, full chip erase, (multi) word/byte write and block lock-bit configuration completion. In default mode, it transitions low after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration commands and returns to V_{OH} when the WSM has finished executing the internal algorithm. For alternate STS pin configurations, see the Configuration command.

STS can be connected to an interrupt input of the system CPU or controller. It is active at all times.

STS, in default mode, is also High-Z when the device is in block erase suspend (with (multi) word/byte write inactive), (multi) word/byte write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μ F ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 μ F electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power supply trace. The V_{PP} pin supplies the memory cell current for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

5.5 V_{CC} , V_{PP} , $RP\#$ Transitions

Block erase, full chip erase, (multi) word/byte write and block lock-bit configuration are not guaranteed if V_{PP} falls outside of a valid V_{PPH1} range, V_{CC} falls outside of a valid $V_{CC1/2}$ range, or $RP\#=V_{IL}$. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If $RP\#$ transitions to V_{IL} during block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, STS(if set to RY/BY# mode) will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or $RP\#$ transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or $CE\#$ transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO} .

After block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, even after V_{PP} transitions down to V_{PPLK} , the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block and full chip erasure, (multi) word/byte writing or block lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC})

powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $WE\#$ and $CE\#$ must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while $RP\#=V_{IL}$ regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering $RP\#$ to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after $RP\#$ is first raised to V_{IH} . See AC Characteristics— Read Only and Write Operations and Figures 18, 19, 20, 21 for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

| | |
|---|---|
| Commercial Operating Temperature | |
| During Read, Erase, Write and | |
| Block Lock-Bit Configuration | 0°C to +70°C ⁽¹⁾ |
| Temperature under Bias | -10°C to +80°C |
| Storage Temperature | -65°C to +125°C |
| Voltage On Any Pin | |
| (except V _{CC} , V _{PP}) | -0.5V to V _{CC} +0.5V ⁽²⁾ |
| V _{CC} Supply Voltage | -0.2V to +7.0V ⁽²⁾ |
| V _{PP} Update Voltage during | |
| Erase, Write and | |
| Block Lock-Bit Configuration | -0.2V to +7.0V ⁽²⁾ |
| Output Short Circuit Current | 100mA ⁽³⁾ |

NOTICE: This datasheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local SHARP Sales office that you have the latest datasheet before finalizing a design.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

| Symbol | Parameter | Min. | Max. | Unit | Test Condition |
|------------------|---|------|------|------|---------------------|
| T _A | Operating Temperature | 0 | +70 | °C | Ambient Temperature |
| V _{CC1} | V _{CC} Supply Voltage (5V±5%) | 4.75 | 5.25 | V | |
| V _{CC2} | V _{CC} Supply Voltage (5V±10%) | 4.50 | 5.50 | V | |

6.2.1 CAPACITANCE⁽¹⁾

T_A=+25°C, f=1MHz

| Symbol | Parameter | Typ. | Max. | Unit | Condition |
|------------------|--------------------|------|------|------|------------------------|
| C _{IN} | Input Capacitance | 7 | 10 | pF | V _{IN} =0.0V |
| C _{OUT} | Output Capacitance | 9 | 12 | pF | V _{OUT} =0.0V |

NOTE:

1. Sampled, not 100% tested.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS

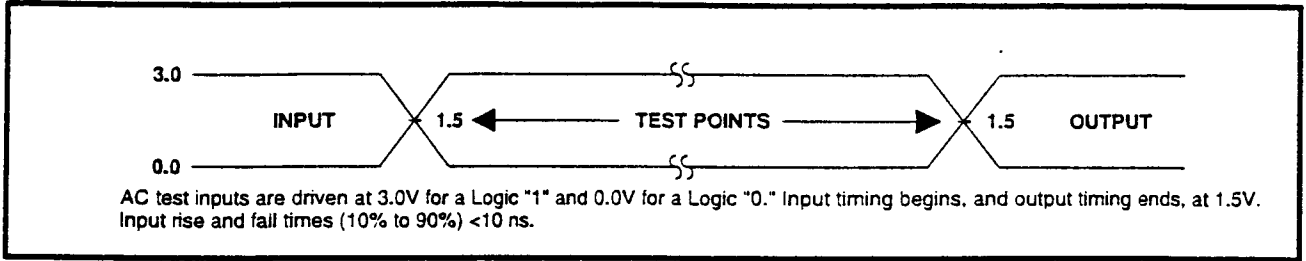


Figure 15. Transient Input/Output Reference Waveform for $V_{CC}=5V\pm 5\%$
(High Speed Testing Configuration)

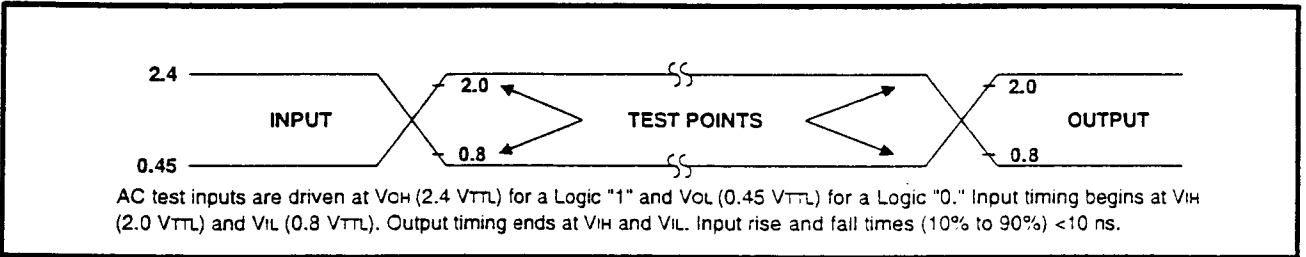


Figure 16. Transient Input/Output Reference Waveform for $V_{CC}=5V\pm 10\%$
(Standard Testing Configuration)

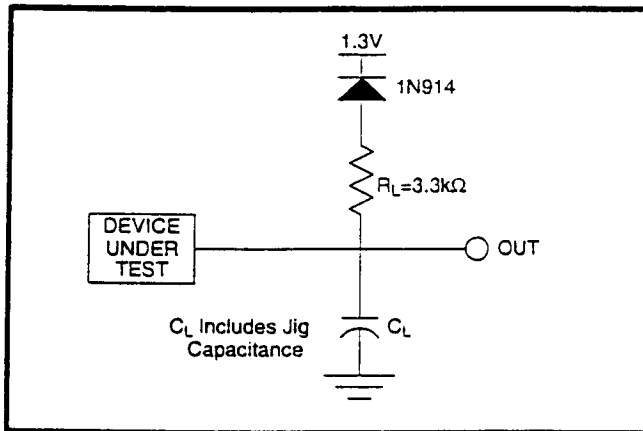


Figure 17. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

| Test Configuration | C_L (pF) |
|---------------------|------------|
| $V_{CC}=5V\pm 5\%$ | 30 |
| $V_{CC}=5V\pm 10\%$ | 100 |

6.2.3 DC CHARACTERISTICS

DC Characteristics

| Symbol | Parameter | Notes | V _{CC} =5V | | Unit | Test Conditions |
|--|--|-------|---------------------|------|------|--|
| | | | Typ. | Max. | | |
| I _{LI} | Input Load Current | 1 | | ±1 | μA | V _{CC} =V _{CC} Max V _{IN} =V _{CC} or GND |
| I _{LO} | Output Leakage Current | 1 | | ±10 | μA | V _{CC} =V _{CC} Max V _{OUT} =V _{CC} or GND |
| I _{CCS} | V _{CC} Standby Current | 1,3,6 | 25 | 100 | μA | CMOS Inputs V _{CC} =V _{CC} Max CE#=RP#=V _{CC} ±0.2V |
| | | | 2 | 4 | mA | TTL Inputs V _{CC} =V _{CC} Max CE#=RP#=V _{IH} |
| I _{CCD} | V _{CC} Deep Power-Down Current | 1 | | 20 | μA | RP#=GND±0.2V I _{OUT} (STS)=0mA |
| I _{CCR} | V _{CC} Read Current | 1,5,6 | | 50 | mA | CMOS Inputs V _{CC} =V _{CC} Max, CE#=GND f=8MHz, I _{OUT} =0mA |
| | | | | 65 | mA | TTL Inputs V _{CC} =V _{CC} Max, CE#=V _{IL} f=8MHz, I _{OUT} =0mA |
| I _{CCW} | V _{CC} Write Current (Multi) W/B Write or Set Block Lock Bit) | 1,7 | | 35 | mA | V _{PP} =5.0V±10% |
| I _{CC E} | V _{CC} Erase Current (Block Erase, Full Chip Erase, Clear Block Lock Bits) | 1,7 | | 30 | mA | V _{PP} =5.0V±10% |
| I _{CCWS} I _{CCES} | V _{CC} Write or Block Erase Suspend Current | 1,2 | 1 | 10 | mA | CE#=V _{IH} |
| I _{PPS} | V _{PP} Standby Current | 1 | ±2 | ±15 | μA | V _{PP} ≤V _{CC} |
| I _{PPR} | V _{PP} Read Current | 1 | 10 | 200 | μA | V _{PP} >V _{CC} |
| I _{PPD} | V _{PP} Deep Power-Down Current | 1 | 0.1 | 5 | μA | RP#=GND±0.2V |
| I _{PPW} | V _{PP} Write Current (Multi) W/B Write or Set Block Lock Bit) | 1,7 | | 80 | mA | V _{PP} =5.0V±10% |
| I _{PPE} | V _{PP} Erase Current (Block Erase, Full Chip Erase, Clear Block Lock Bits) | 1,7 | | 40 | mA | V _{PP} =5.0V±10% |
| I _{PPWS} I _{PPES} | V _{PP} Write or Block Erase Suspend Current | 1 | 10 | 200 | μA | V _{PP} =V _{PPH1} |

LH28F320S5-L90/12 Smart 5 Flash MEMORY

DC Characteristics (Continued)

| Symbol | Parameter | Notes | V _{CC} =5V | | Unit | Test Conditions |
|-------------------|--|-------|----------------------|----------------------|------|---|
| | | | Min. | Max. | | |
| V _{IL} | Input Low Voltage | 7 | -0.5 | 0.8 | V | |
| V _{IH} | Input High Voltage | 7 | 2.0 | V _{CC} +0.5 | V | |
| V _{OL} | Output Low Voltage | 3,7 | | 0.45 | V | V _{CC} =V _{CC} Min I _{OL} =5.8mA |
| V _{OH1} | Output High Voltage (TTL) | 3,7 | 2.4 | | V | V _{CC} =V _{CC} Min I _{OH} =-2.5mA |
| V _{OH2} | Output High Voltage (CMOS) | 3,7 | 0.85 | | V | V _{CC} =V _{CC} Min I _{OH} =-2.5mA |
| | | | V _{CC} -0.4 | | V | V _{CC} =V _{CC} Min I _{OH} =-100μA |
| V _{PPLK} | V _{PP} Lockout during Normal Operations | 4,7 | | 1.5 | V | |
| V _{PPH1} | V _{PP} during Write or Erase Operations | | 4.5 | 5.5 | V | |
| V _{LKO} | V _{CC} Lockout Voltage | | 2.0 | | V | |

NOTES:

- All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A=+25°C. These currents are valid for all product versions (packages and speeds).
- I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
- Includes STS.
- Block erases, full chip erases, (multi) word/byte writes and block lock-bit configurations are inhibited when V_{PP} ≤ V_{PPLK}, and not guaranteed in the range between V_{PPLK}(max) and V_{PPH1}(min) and above V_{PPH1}(max).
- Automatic Power Savings (APS) reduces typical I_{CCR} to 1mA at 5V V_{CC} in static operation.
- CMOS inputs are either V_{CC}±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.
- Sampled, not 100% tested.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS⁽¹⁾

$V_{CC}=5V\pm0.5V, 5V\pm0.25V, T_A=0^{\circ}C$ to $+70^{\circ}C$

| Versions ⁽⁴⁾ | | Notes | LH28F320S5-L90 ⁽⁵⁾ | | LH28F320S5-L100 ⁽⁶⁾ | | LH28F320S5-L120 ⁽⁶⁾ | | Unit |
|-------------------------|---|-------|-------------------------------|-----------------|--------------------------------|------|--------------------------------|------|------|
| | | | $V_{CC}\pm5\%$ | $V_{CC}\pm10\%$ | Min. | Max. | Min. | Max. | |
| Sym. | Parameter | | Min. | Max. | Min. | Max. | Min. | Max. | Unit |
| t_{AVAV} | Read Cycle Time | | 90 | | 100 | | 120 | | ns |
| t_{AVOV} | Address to Output Delay | | | 90 | | 100 | | 120 | ns |
| t_{ELQV} | CE# to Output Delay | 2 | | 90 | | 100 | | 120 | ns |
| t_{PHQV} | RP# High to Output Delay | | | 400 | | 400 | | 400 | ns |
| t_{GLQV} | OE# to Output Delay | 2 | | 30 | | 35 | | 40 | ns |
| t_{ELOX} | CE# to Output in Low Z | 3 | 0 | | 0 | | 0 | | ns |
| t_{EHOZ} | CE# High to Output in High Z | 3 | | 25 | | 30 | | 35 | ns |
| t_{GLOX} | OE# to Output in Low Z | 3 | 0 | | 0 | | 0 | | ns |
| t_{GHOZ} | OE# High to Output in High Z | 3 | | 10 | | 10 | | 15 | ns |
| t_{OH} | Output Hold from Address, CE# or OE# Change, Whichever Occurs First | 3 | 0 | | 0 | | 0 | | ns |
| t_{FLOV} | BYTE# to Output Delay | 3 | | 90 | | 100 | | 120 | ns |
| t_{FHOV} | BYTE# to Output in High Z | 3 | | 25 | | 30 | | 30 | ns |
| t_{ELOZ} | CE# Low to BYTE# High or Low | 3 | | 5 | | 5 | | 5 | ns |
| t_{ELFL} | | | | | | | | | |
| t_{ELFH} | | | | | | | | | |

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to $t_{ELQV}-t_{GLQV}$ after the falling edge of CE# without impact on t_{ELQV} .
3. Sampled, not 100% tested.
4. See Ordering Information for device speeds (valid operational combinations).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

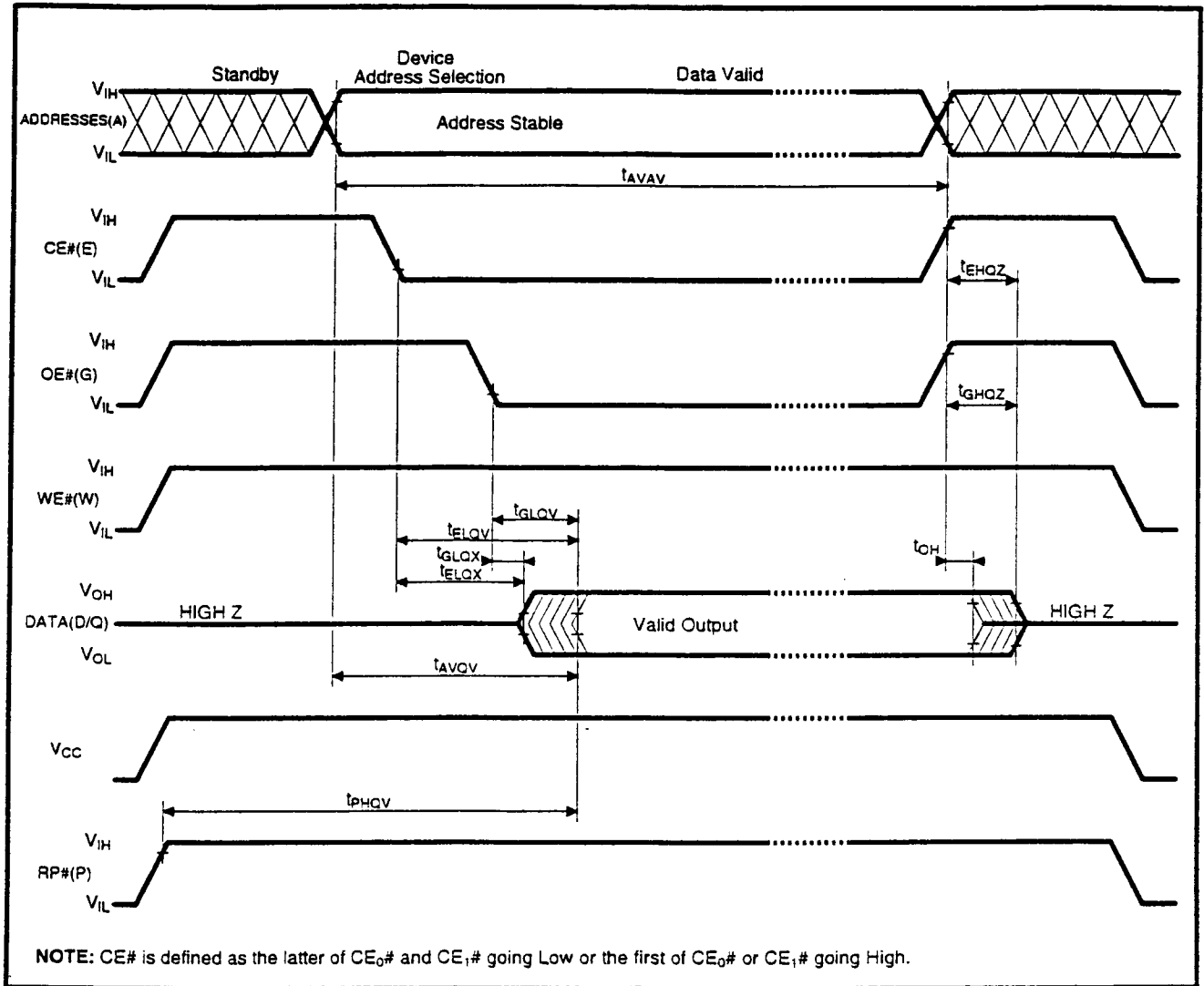


Figure 18. AC Waveform for Read Operations

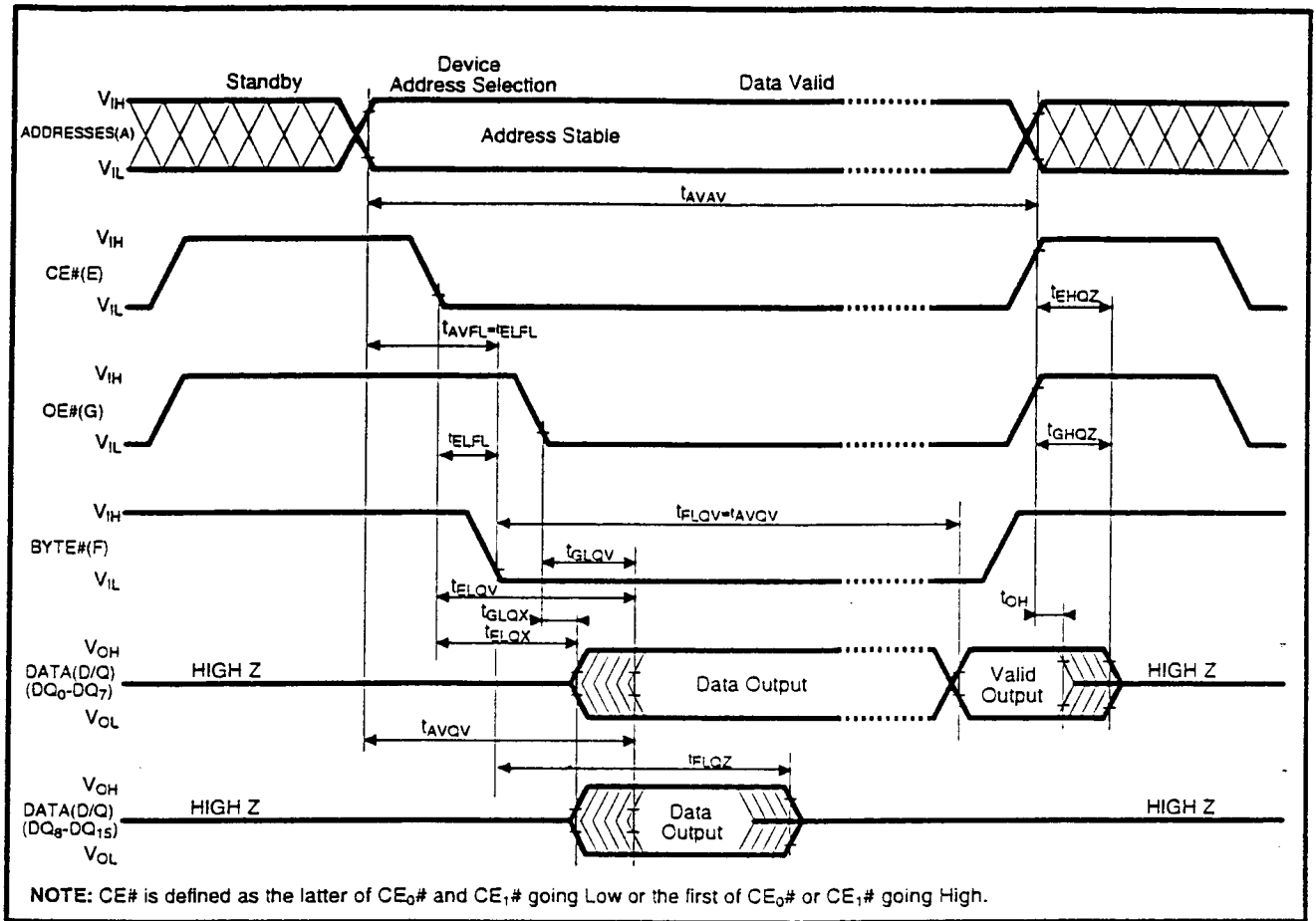


Figure 19. BYTE# Timing Waveforms

LH28F320S5-L90/12 Smart 5 Flash MEMORY

6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS(1)

$V_{CC}=5V\pm 0.5V, 5V\pm 0.25V, T_A=0^{\circ}C$ to $+70^{\circ}C$

| Versions ⁽⁵⁾ | | Notes | LH28F320S5-L90 ⁽⁶⁾ | | LH28F320S5-L100 ⁽⁷⁾ | | LH28F320S5-L120 ⁽⁷⁾ | | Unit |
|-------------------------|--|-------|-------------------------------|------------------|--------------------------------|------|--------------------------------|------|---------|
| | | | $V_{CC}\pm 5\%$ | $V_{CC}\pm 10\%$ | Min. | Max. | Min. | Max. | |
| Sym. | Parameter | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{AVAV} | Write Cycle Time | | 90 | | 100 | | 120 | | ns |
| t_{PHWL} | RP# High Recovery to WE# Going Low | 2 | 1 | | 1 | | 1 | | μs |
| t_{E1WL} | CE# Setup to WE# Going Low | | 10 | | 10 | | 10 | | ns |
| t_{WLWH} | WE# Pulse Width | | 40 | | 40 | | 40 | | ns |
| t_{SHWH} | WP# V_{IH} Setup to WE# Going High | 2 | 100 | | 100 | | 100 | | ns |
| t_{VPWH} | V_{PP} Setup to WE# Going High | 2 | 100 | | 100 | | 100 | | ns |
| t_{AVWH} | Address Setup to WE# Going High | 3 | 40 | | 40 | | 40 | | ns |
| t_{DVWH} | Data Setup to WE# Going High | 3 | 40 | | 40 | | 40 | | ns |
| t_{WHDX} | Data Hold from WE# High | | 5 | | 5 | | 5 | | ns |
| t_{WHAX} | Address Hold from WE# High | | 5 | | 5 | | 5 | | ns |
| t_{WHEH} | CE# Hold from WE# High | | 10 | | 10 | | 10 | | ns |
| t_{WHWL} | WE# Pulse Width High | | 30 | | 30 | | 30 | | ns |
| t_{WHRL} | WE# High to STS Going Low | | | 90 | | 90 | | 90 | ns |
| t_{WHGL} | Write Recovery before Read | | 0 | | 0 | | 0 | | ns |
| t_{QVVL} | V_{PP} Hold from Valid SRD, STS High Z | 2,4 | 0 | | 0 | | 0 | | ns |
| t_{QVSL} | WP# V_{IH} Hold from Valid SRD, STS High Z | 2,4 | 0 | | 0 | | 0 | | ns |

NOTES:

1. Read timing characteristics during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
4. V_{PP} should be held at V_{PPH1} until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5=0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
7. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.

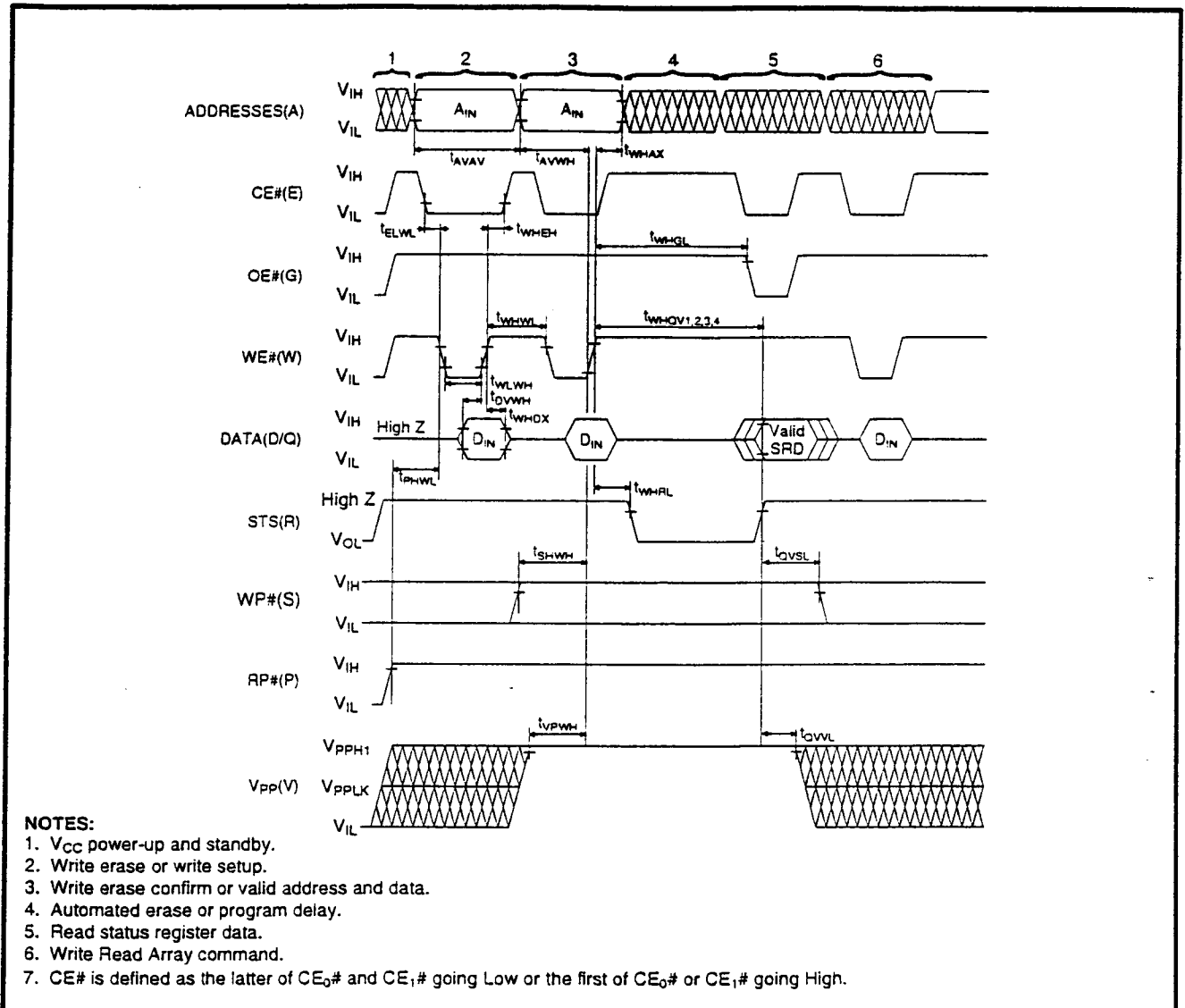


Figure 20. AC Waveform for WE#-Controlled Write Operations

LH28F320S5-L90/12 Smart 5 Flash MEMORY

6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES(1)

$V_{CC}=5V\pm 0.5V, 5V\pm 0.25V, T_A=0^{\circ}C$ to $+70^{\circ}C$

| Versions ⁽⁵⁾ | | Notes | LH28F320S5-L90 ⁽⁶⁾ | | LH28F320S5-L100 ⁽⁷⁾ | | LH28F320S5-L120 ⁽⁷⁾ | | Unit |
|-------------------------|--|-------|-------------------------------|------------------|--------------------------------|------|--------------------------------|------|---------|
| | | | $V_{CC}\pm 5\%$ | $V_{CC}\pm 10\%$ | Min. | Max. | Min. | Max. | |
| Sym. | Parameter | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{AVAV} | Write Cycle Time | | 90 | | 100 | | 120 | | ns |
| t_{PHEL} | RP# High Recovery to CE# Going Low | 2 | 1 | | 1 | | 1 | | μs |
| t_{WLEI} | WE# Setup to CE# Going Low | | 0 | | 0 | | 0 | | ns |
| t_{ELEH} | CE# Pulse Width | | 50 | | 50 | | 50 | | ns |
| t_{SHEH} | WP# V_{IH} Setup to CE# Going High | 2 | 100 | | 100 | | 100 | | ns |
| t_{VPEH} | V_{PP} Setup to CE# Going High | 2 | 100 | | 100 | | 100 | | ns |
| t_{AVEH} | Address Setup to CE# Going High | 3 | 40 | | 40 | | 40 | | ns |
| t_{DVEH} | Data Setup to CE# Going High | 3 | 40 | | 40 | | 40 | | ns |
| t_{EHDX} | Data Hold from CE# High | | 5 | | 5 | | 5 | | ns |
| t_{EHAX} | Address Hold from CE# High | | 5 | | 5 | | 5 | | ns |
| t_{EHWL} | WE# Hold from CE# High | | 0 | | 0 | | 0 | | ns |
| t_{EHEL} | CE# Pulse Width High | | 25 | | 25 | | 25 | | ns |
| t_{EHBI} | CE# High to STS Going Low | | | 90 | | 90 | | 90 | ns |
| t_{EHGI} | Write Recovery before Read | | 0 | | 0 | | 0 | | ns |
| t_{QVVL} | V_{PP} Hold from Valid SRD, STS High Z | 2,4 | 0 | | 0 | | 0 | | ns |
| t_{QVSL} | WP# V_{IH} Hold from Valid SRD, STS High Z | 2,4 | 0 | | 0 | | 0 | | ns |

NOTES:

1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
4. V_{PP} should be held at V_{PPH1} until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5=0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
7. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.

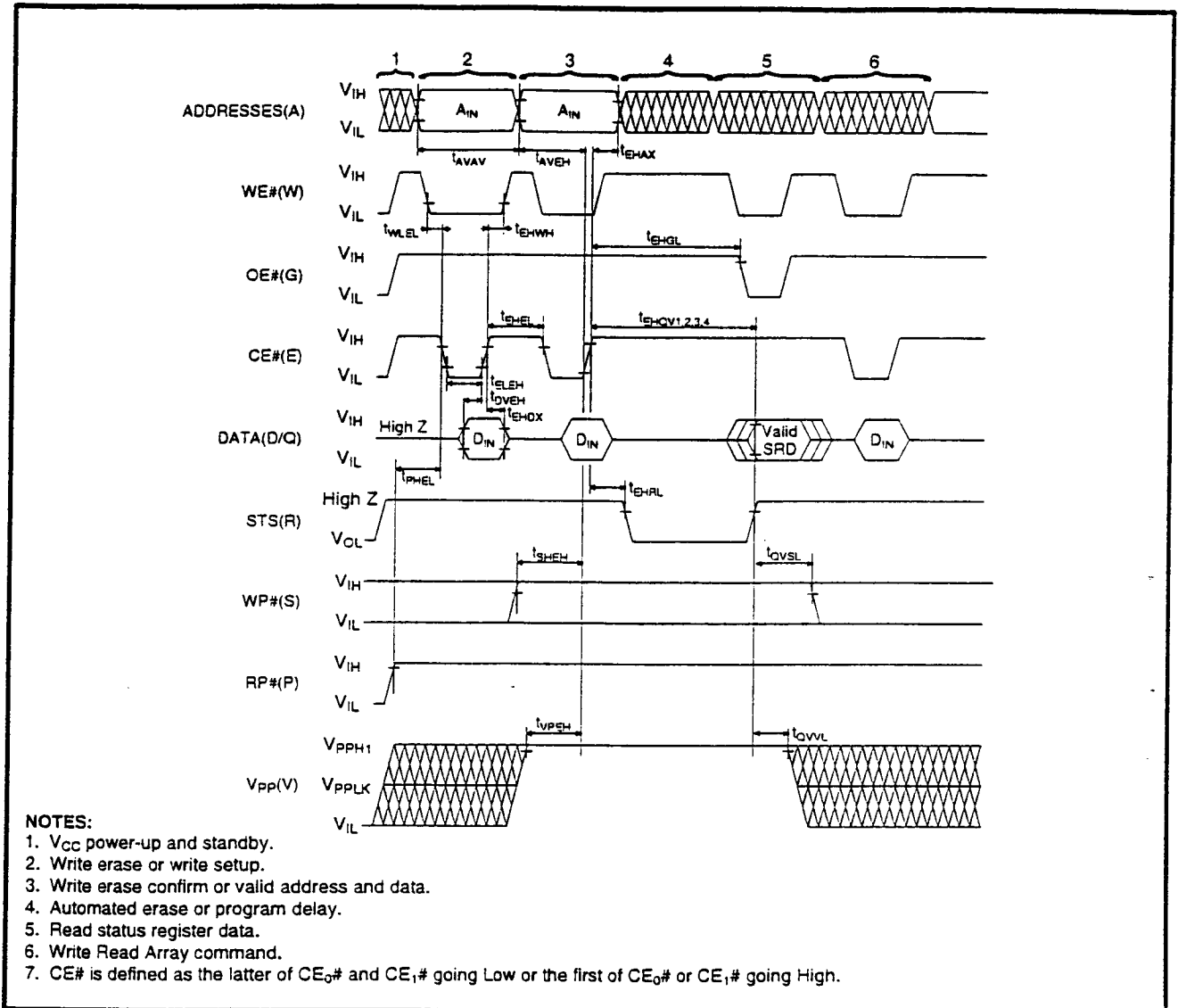


Figure 21. Alternate AC Waveform for CE#-Controlled Write Operations

6.2.7 RESET OPERATIONS

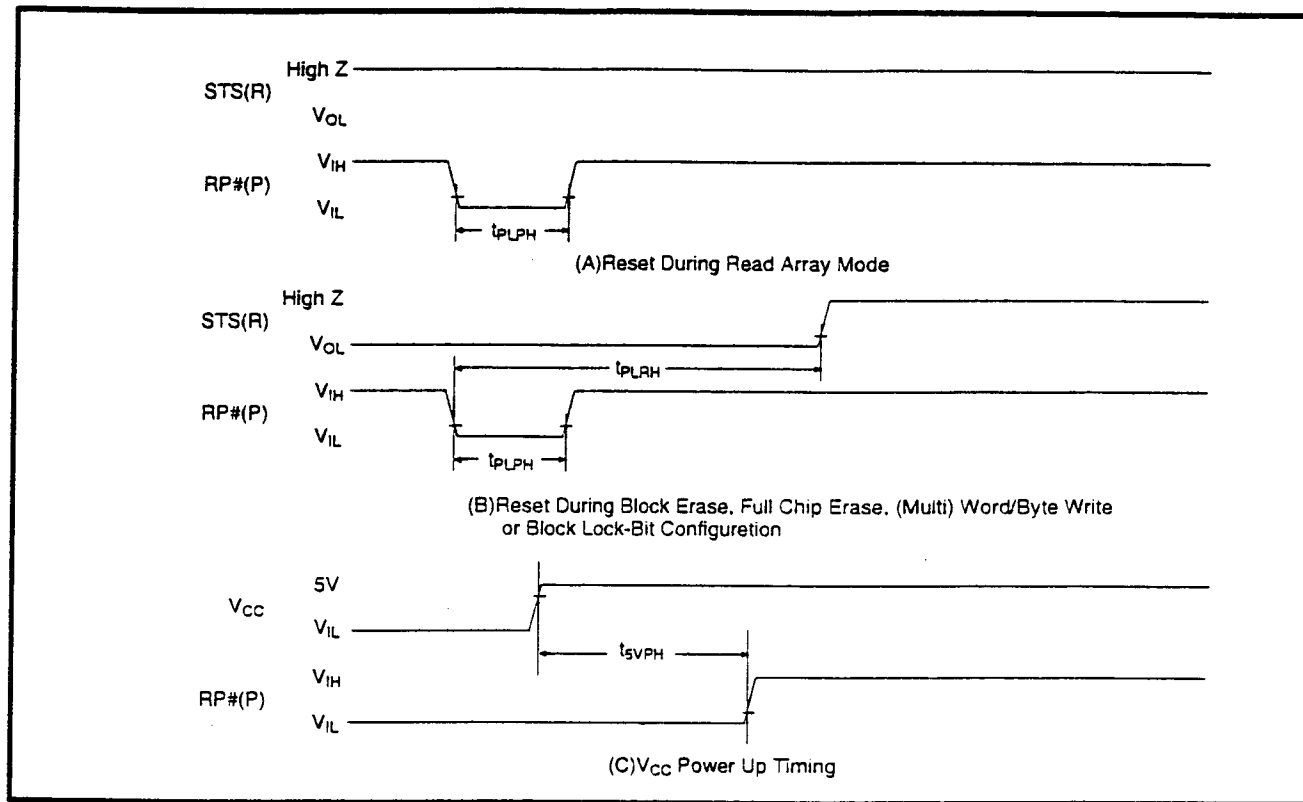


Figure 22. AC Waveform for Reset Operation

Reset AC Specifications⁽¹⁾

| Symbol | Parameter | Notes | V _{CC} =5V | | Unit |
|-------------------|---|-------|---------------------|------|------|
| | | | Min. | Max. | |
| t _{PLPH} | RP# Pulse Low Time (If RP# is tied to V _{CC} , this specification is not applicable) | | 100 | | ns |
| t _{PLRH} | RP# Low to Reset during Block Erase, Full Chip Erase, (Multi) Word/Byte Write or Block Lock-Bit Configuration | 2,3 | | 13.1 | μs |
| t _{SVPH} | V _{CC} at 4.5V to RP# High | 4 | | 50 | μs |

NOTES:

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is not executing, the reset will complete within 100ns.
3. A reset time, t_{PHQV}, is required from the latter of STS going High Z or RP# going high until outputs are valid.
4. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.8 BLOCK ERASE, FULL CHIP ERASE, (MULTI) WORD/BYTE WRITE AND BLOCK LOCK-BIT CONFIGURATION PERFORMANCE(3,4)

$V_{CC}=5V\pm 0.5V$, $5V\pm 0.25V$, $T_A=0^\circ C$ to $+70^\circ C$

| Sym. | Parameter | Notes | $V_{pp}=4.5V-5.5V$ | | | Unit |
|----------------------------|---|-------|--------------------|---------------------|------|---------|
| | | | Min. | Typ. ⁽¹⁾ | Max. | |
| t_{WHQV1} t_{EHQV1} | Word/Byte Write Time (using W/B write, in word mode) | 2 | | 9.24 | TBD | μs |
| t_{WHQV1} t_{EHQV1} | Word/Byte Write Time (using W/B write, in byte mode) | 2 | | 9.24 | TBD | μs |
| | Word/Byte Write Time (using multi word/byte write) | 2 | | 2 | TBD | μs |
| | Block Write Time (using W/B write, in word mode) | 2 | | 0.38 | TBD | sec |
| | Block Write Time (using W/B write, in byte mode) | 2 | | 0.5 | TBD | sec |
| | Block Write Time (using multi word/byte write) | 2 | | 0.13 | TBD | sec |
| t_{WHQV2} t_{EHQV2} | Block Erase Time | 2 | | 0.34 | TBD | sec |
| | Full Chip Erase Time | | | 21.8 | TBD | sec |
| t_{WHQV3} t_{EHQV3} | Set Block Lock-Bit Time | 2 | | 9.24 | TBD | μs |
| t_{WHQV4} t_{EHQV4} | Clear Block Lock-Bits Time | 2 | | 0.34 | TBD | sec |
| t_{WHRH1} t_{EHRH1} | Write Suspend Latency Time to Read | | | 5.6 | 7 | μs |
| t_{WHRH2} t_{EHRH2} | Erase Suspend Latency Time to Read | | | 9.4 | 13.1 | μs |

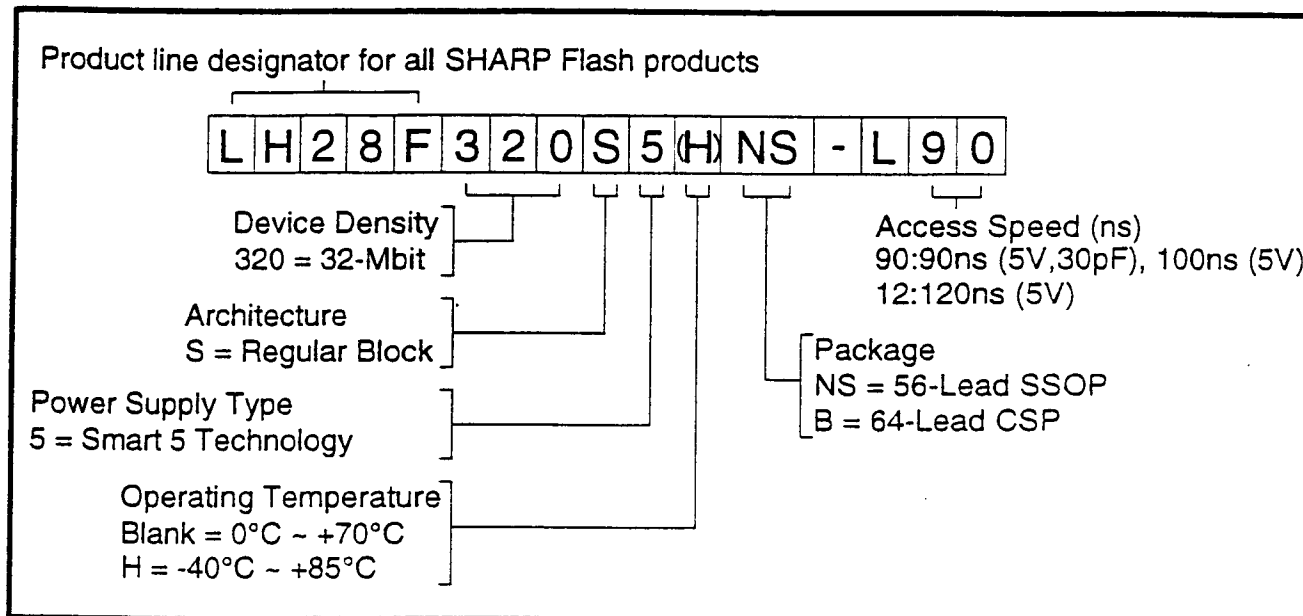
NOTES:

1. Typical values measured at $T_A=+25^\circ C$ and nominal voltages. Assumes corresponding block lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.

LH28F320S5-L90/12 Smart 5 Flash MEMORY

7 ADDITIONAL INFORMATION

7.1 Ordering Information



| Option | Order Code | Valid Operational Combinations | |
|--------|-----------------|---|--|
| | | V _{CC} =5.0±10% 100pF load, TTL I/O Levels | V _{CC} =5.0±5% 30pF load, 1.5V I/O Levels |
| 1 | LH28F320S5X-L90 | LH28F320S5-L100 | LH28F320S5-L90 |
| 2 | LH28F320S5X-L12 | LH28F320S5-L120 | |

LH28F320S5-L90/12, 32M, Smart 5, Flash, Flash File, CFI, ETOX Non Volatile