

SANYO

No. ※5399

LC361000AMLL, ATLL, ARLL-70X/10X**1 MEG (131072 words × 8 bits) SRAM**

Preliminary

Overview

The LC361000AMLL, ATLL, and ARLL are 131072 words × 8 bits asynchronous silicon gate CMOS static RAMs. These SRAMs have two chip enable pins ($\overline{CE1}$ and $\overline{CE2}$) for controlling the device selected/unselected state and one output enable pin (\overline{OE}) for output control and feature high speed, low power, and wide temperature range. This makes these SRAMs optimal for systems that require high speed, low power, and battery backup, and they furthermore allow easy expansion of memory capacity.

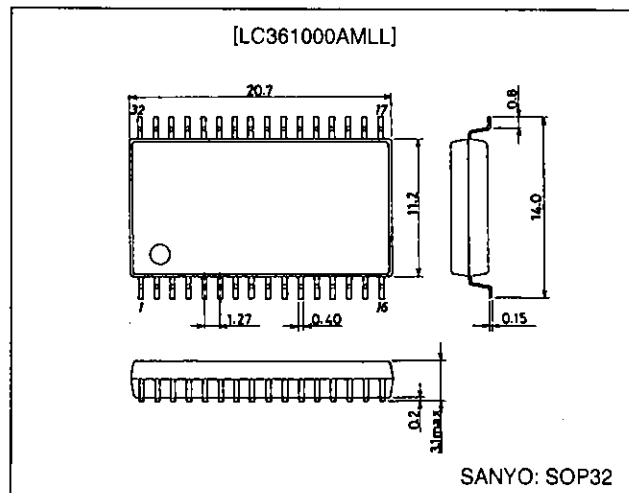
Features

- Access time
 - 70 ns (max.): LC361000AMLL, ATLL, ARLL-70X
 - 100 ns (max.): LC361000AMLL, ATLL, ARLL-10X
- Low current drain
 - During standby
 - 2.0 μA (max.)/ $T_a = 25^\circ\text{C}$
 - 4.0 μA (max.)/ $T_a = -20$ to $+40^\circ\text{C}$
 - 20.0 μA (max.)/ $T_a = -20$ to $+70^\circ\text{C}$
 - 40.0 μA (max.)/ $T_a = -20$ to $+85^\circ\text{C}$
 - During data retention
 - 1.2 μA (max.)/ $T_a = 25^\circ\text{C}$
 - 2.4 μA (max.)/ $T_a = -20$ to $+40^\circ\text{C}$
 - 12.0 μA (max.)/ $T_a = -20$ to $+70^\circ\text{C}$
 - 24.0 μA (max.)/ $T_a = -20$ to $+85^\circ\text{C}$
 - During operation (DC)
 - 15 mA (max.)
- Single 5 V power supply: 5 V $\pm 10\%$
- Wide range of operating temperature: -20 to 85°C
- Data retention supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, with three output states
- Package
 - SOP 32-pin (525 mil) plastic package: LC361000AMLL
 - TSOP 32-pin (8 mm × 20 mm) plastic package, normal: LC361000ATLL
 - TSOP 32-pin (8 mm × 20 mm) plastic package, reversed: LC361000ARLL

Package Dimensions

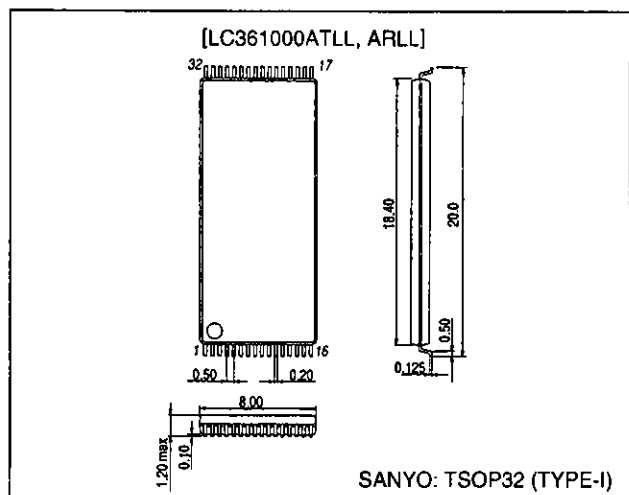
unit: mm

3205-SOP32



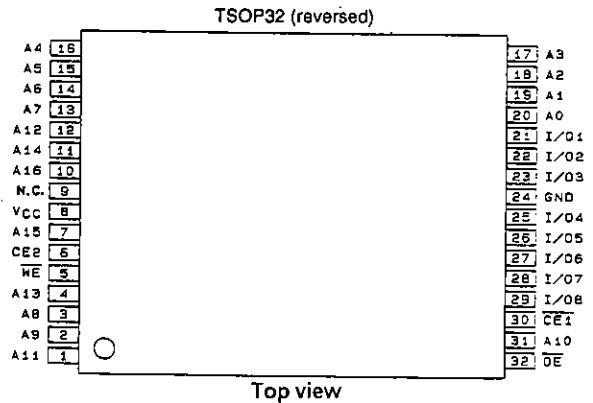
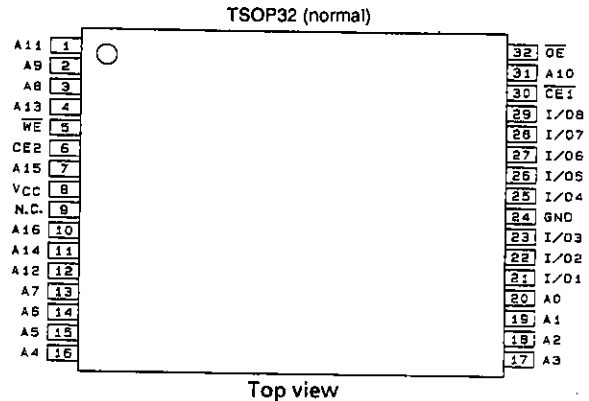
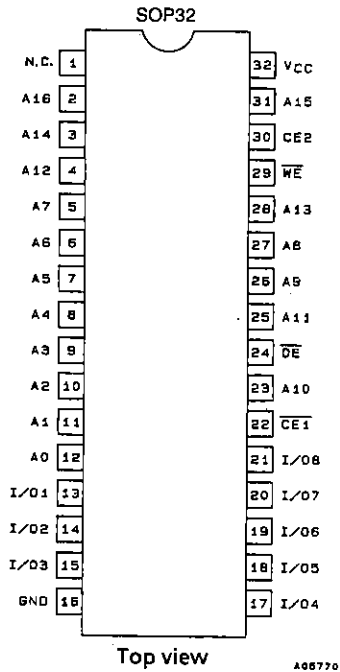
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3224-TSOP32

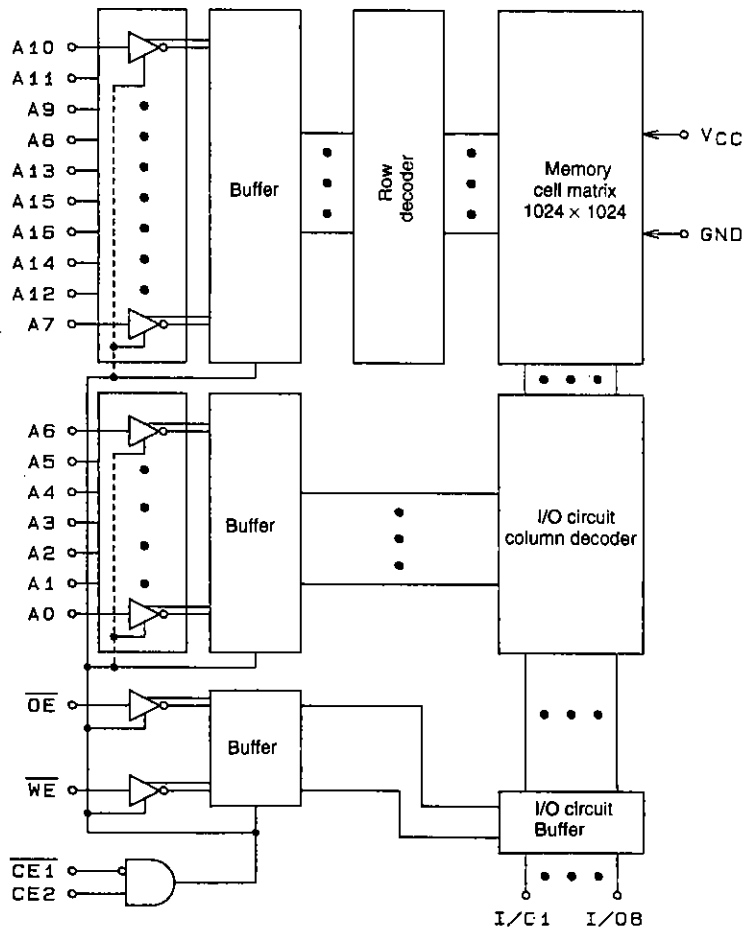


LC361000AMLL, ATLL, ARLL-70X/10X

Pin Assignments



Block Diagram



LC361000AMLL, ATLL, ARL-70X/10X

Pin Functions

A0 to A16	Address inputs
\overline{WE}	Read/write control Input
\overline{OE}	Output enable input
CE1, CE2	Chip enable input
I/O1 to I/O8	Data Input/output
V _{CC} , GND	Power supply pins

Function Logic

Mode	CE1	CE2	\overline{OE}	\overline{WE}	I/O	Supply current
Read cycle	L	H	L	H	Data output	I _{CCA}
Write cycle	L	H	X	L	Data input	I _{CCA}
Output disable	L	H	H	H	High impedance	I _{CCA}
Nonselect	H	X	X	X	High impedance	I _{CCS}
	X	L	X	X	High impedance	I _{CCS}

X: H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Ratings	Unit
Maximum supply voltage	V _{CC max}	7.0	V
Input pin voltage	V _{IN}	-0.5* to V _{CC} +0.5	V
I/O pin voltage	V _{I/O}	-0.5* to V _{CC} +0.5	V
Allowable power dissipation	Pd max	0.7	W
Operating temperature	T _{opr}	-20 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C

Note: * -3.0 V when pulse width is less than 50 ns.

Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at Ta = -20 to +85°C

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high level voltage	V _{IH}	2.2		V _{CC} +0.3	V
Input low level voltage	V _{IL}	-0.3*		+0.8	V

Note: * -3.0 V when pulse width is less than 50 ns.

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DC Electrical Characteristics at Ta = -20 to +85°C

Parameter	Symbol	Conditions	min	typ*	max	Unit
Operating supply current (DC)	I _{CCA1}	V _{CE1} ≤ 0.2 V, V _{CE2} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V, I _{I/O} = 0 mA			10	mA
	I _{CCA2}	V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0 mA		7	15	mA
Average operating supply current	I _{CCA3}	V _{CE1} = V _{IL} , V _{CE2} = V _{IH} , I _{I/O} = 0 mA, min cycle	70 ns	40	80	mA
			100 ns	35	60	
Standby supply current	I _{CCS1}	(V _{CE2} ≤ 0.2 V) or (V _{CE1} ≥ V _{CC} - 0.2 V, V _{CE2} ≥ V _{CC} - 0.2 V or V _{CE2} ≤ 0.2 V)	-20 to +85°C		40	μA
			-20 to +70°C		20	
			-20 to +40°C		4	
			25°C	0.7	2	
	I _{CCS2}	V _{CE2} = V _{IL} or V _{CE1} = V _{IH}		0.6	3	mA
Input leakage current	I _{LI}	V _{IN} = 0 to V _{CC}	-1		+1	μA
I/O leakage current	I _{LO}	V _{CE1} = V _{IH} or V _{CE2} = V _{IL} or V _{OE} = V _{IH} or V _{WE} = V _{IL} , I _{I/O} = 0 to V _{CC}	-1		+1	μA
Output high level voltage	V _{OH}	I _{OH} = -1.0 mA	2.4			V
Output low level voltage	V _{OL}	I _{OL} = 2.1 mA			0.4	V

Note: * Reference value at V_{CC} = 5 V, Ta = 25°C.

Input/Output Capacitances at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input capacitance	C _{IN}	V _{IN} = 0 V			7	pF
Input/output capacitance	C _{I/O}	V _{I/O} = 0 V			8	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at Ta = -20 to +85°C, V_{CC} = 5 V ±10%

AC Test Conditions

Parameter	Conditions
Input pulse voltage level	0.6 V, 2.4 V
Input rise and fall time	5 ns
Input and output timing level	1.5 V
Output load	1 TTL gate + C _L = 100 pF (70 ns/100 ns) (including scope and jig capacitances)

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Read Cycle

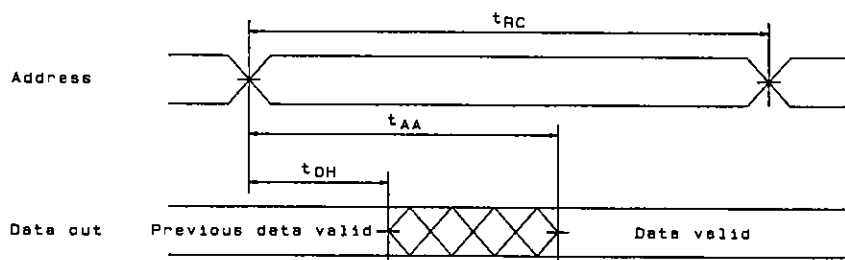
Parameter	Symbol	LC361000AMLL, ATLL, ARLL				Unit
		-70X		-10X		
		min	max	min	max	
Read cycle time	t_{RC}	70		100		ns
Address access time	t_{AA}		70		100	ns
$\overline{CE1}$ access time	t_{CA1}		70		100	ns
CE2 access time	t_{CA2}		70		100	ns
\overline{OE} access time	t_{OA}		40		50	ns
Output hold time	t_{OH}	10		10		ns
$\overline{CE1}$ output enable time	t_{COE1}	10		10		ns
CE2 output enable time	t_{COE2}	10		10		ns
\overline{OE} output enable time	t_{OOE}	5		5		ns
$\overline{CE1}$ output disable time	t_{COD1}		25		35	ns
CE2 output disable time	t_{COD2}		25		35	ns
\overline{OE} output disable time	t_{OOD}		25		35	ns

Write Cycle

Parameter	Symbol	LC361000AMLL, ATLL, ARLL				Unit
		-70X		-10X		
		min	max	min	max	
Write cycle time	t_{WC}	70		100		ns
Address valid to end of write	t_{AW}	60		70		ns
Address setup time	t_{AS}	0		0		ns
Write pulse width	t_{WP}	50		70		ns
$\overline{CE1}$ setup time	t_{CW1}	60		70		ns
CE2 setup time	t_{CW2}	60		70		ns
Write recovery time	t_{WR}	5		5		ns
$\overline{CE1}$ write recovery time	t_{WR1}	0		0		ns
CE2 write recovery time	t_{WR2}	0		0		ns
Data setup time	t_{DS}	30		40		ns
Data hold time	t_{DH}	0		0		ns
$\overline{CE1}$ data hold time	t_{DH1}	0		0		ns
CE2 data hold time	t_{DH2}	0		0		ns
\overline{WE} output enable time	t_{WOE}	10		10		ns
\overline{WE} output disable time	t_{WOD}		25		30	ns

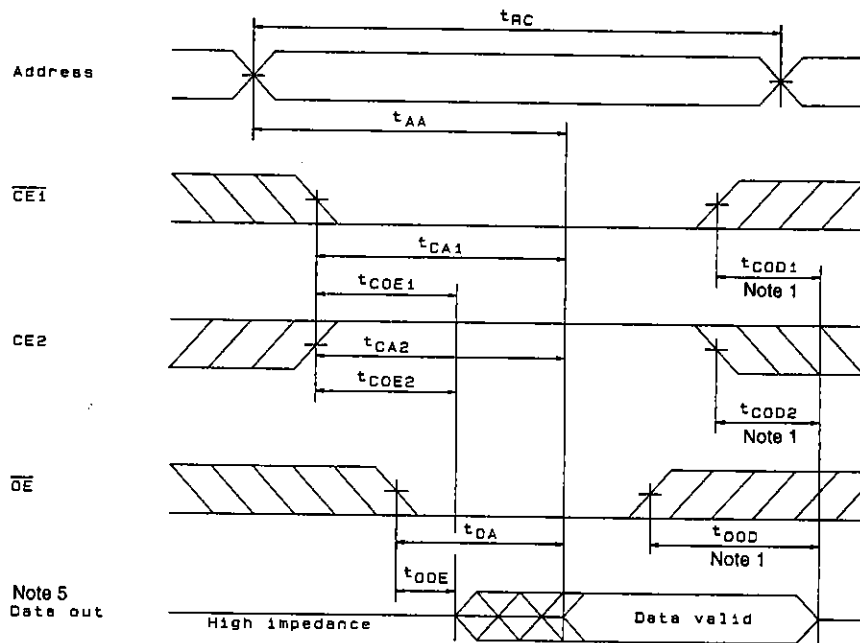
Timing Chart

Read Cycle (1): $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



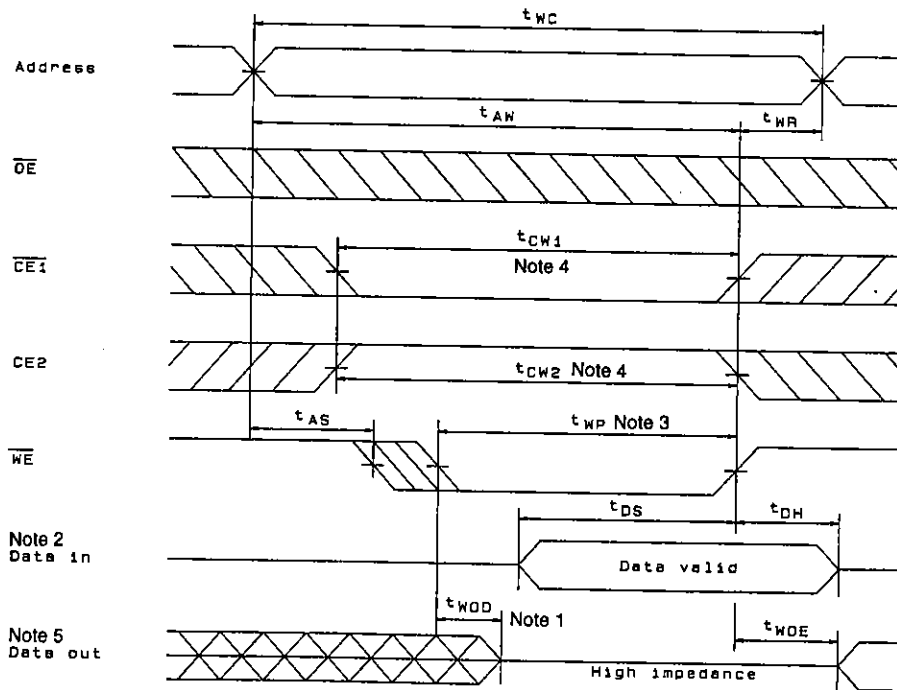
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Read Cycle (2): $\overline{WE} = V_{IH}$



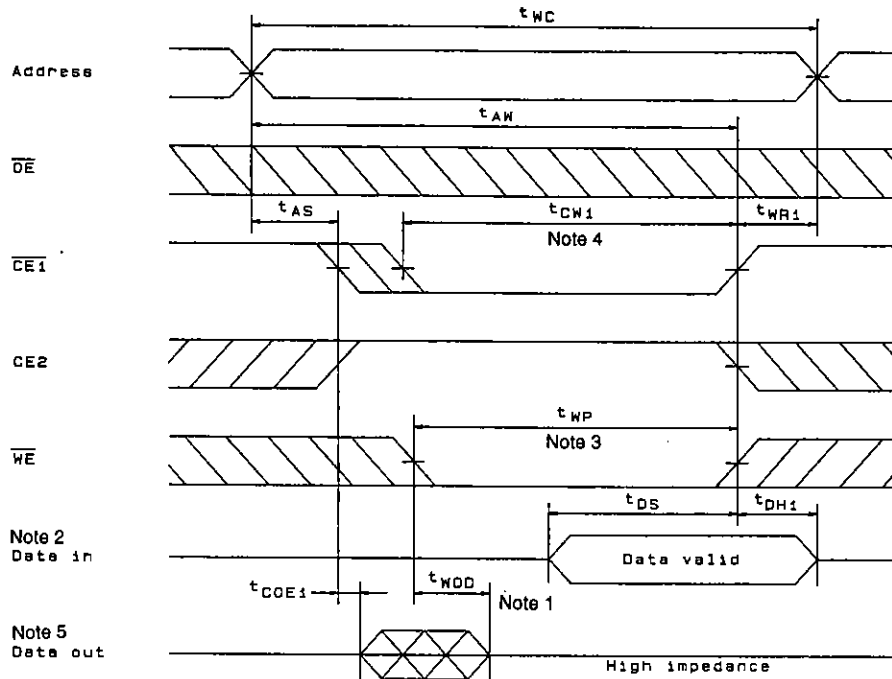
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Write Cycle (1): \overline{WE} control (Note 6)



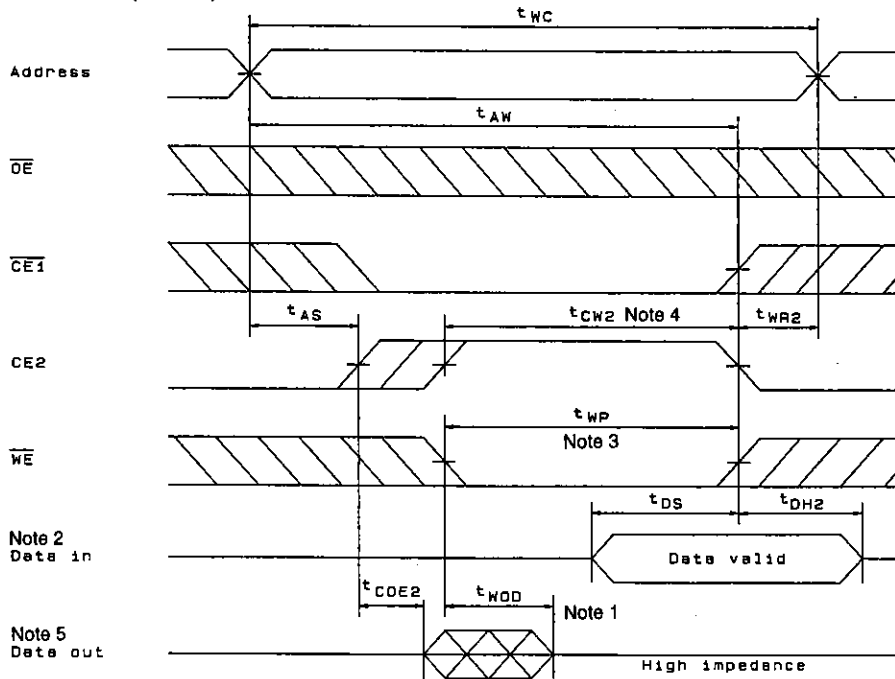
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Write Cycle (2): $\overline{CE1}$ control (Note 6)



Write Cycle (3): $\overline{CE2}$ control (Note 6)

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- Note: 1. t_{COD1} , t_{COD2} , t_{OOD} , and t_{WOD} are stipulated as the times until the outputs reach the high-impedance state, and are not determined by the output voltage levels.
2. Reverse phase signals must not be applied externally when the data outputs are in the output state.
3. t_{WP} is defined as the period when $\overline{CE1}$ and \overline{WE} are low and $\overline{CE2}$ is high, from the falling edge of \overline{WE} until either a rising edge of $\overline{CE1}$ or \overline{WE} or a falling edge of $\overline{CE2}$, whichever of these happens first.
4. t_{WC1} and t_{WC2} are defined as the periods when $\overline{CE1}$ and \overline{WE} are low and $\overline{CE2}$ is high, from either a falling edge of $\overline{CE1}$ or a rising edge of $\overline{CE2}$, until a rising edge of $\overline{CE1}$ or \overline{WE} , or a falling edge of $\overline{CE2}$, whichever happens first.
5. The data outputs will be in the high-impedance state if either \overline{OE} is high, $\overline{CE1}$ is high, $\overline{CE2}$ is low, or \overline{WE} is low.
6. If \overline{OE} goes high during a write cycle, the data outputs will go to the high-impedance state.

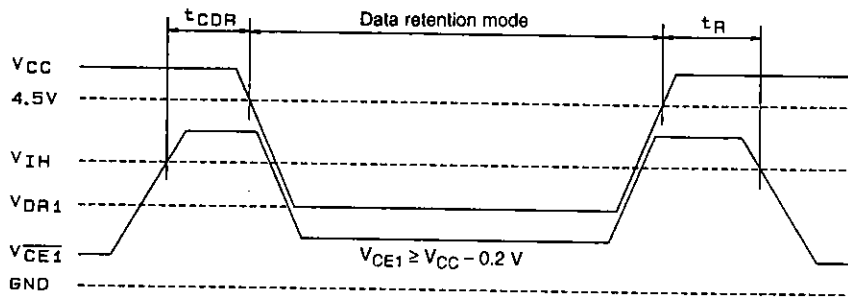
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Data Retention Characteristics at $T_a = -20$ to $+85^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ*	max	Unit
Data retention supply voltage	V_{DR1}	$V_{CE1} \geq V_{CC} - 0.2 \text{ V}$, $V_{CE2} \geq V_{CC} - 0.2 \text{ V}$, or $V_{CE2} \leq 0.2 \text{ V}$	2.0		5.5	V
	V_{DR2}	$V_{CE2} \leq 0.2 \text{ V}$	2.0		5.5	V
Data retention supply current	I_{CCDR1}	$V_{CC} = 3.0 \text{ V}$, $V_{CE1} \geq V_{CC} - 0.2 \text{ V}$, $V_{CE2} \geq V_{CC} - 0.2 \text{ V}$, or $V_{CE2} \leq 0.2 \text{ V}$	-20 to $+85^\circ\text{C}$		24	μA
			-20 to $+70^\circ\text{C}$		12	
			-20 to $+40^\circ\text{C}$		2.4	
			25 $^\circ\text{C}$	0.4	1.2	
	I_{CCDR2}	$V_{CC} = 3.0 \text{ V}$, $V_{CE2} \leq 0.2 \text{ V}$	-20 to $+85^\circ\text{C}$		24	μA
			-20 to $+70^\circ\text{C}$		12	
			-20 to $+40^\circ\text{C}$		2.4	
			25 $^\circ\text{C}$	0.4	1.2	
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		5			ms

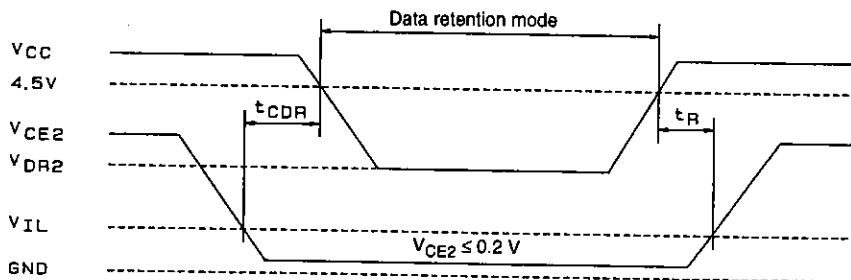
Note: * Reference value at $T_a = 25^\circ\text{C}$.

Data Retention Waveforms (1): (CE1 control)



Data Retention Waveforms (2): (CE2 control)

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