Advanced Power MOSFET

IRLZ14A

FEATURES

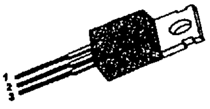
- Logic-Level Gate Drive
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 µA (Max.) @ V_{DS} = 60V
- Lower $R_{DS(ON)}$: 0.122 Ω (Typ.)

BV_{DSS} = 60 V

$R_{DS(on)}$ = 0.155 Ω

I_D = 10 A

TO-220



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic		Value	Units
V_{DSS}	Drain-to-Source Voltage		60	V
I_D	Continuous Drain Current (T_C=25°C)		10	A
	Continuous Drain Current (T_C=100°C)		7	
I_{DM}	Drain Current-Pulsed	①	35	A
V_{GS}	Gate-to-Source Voltage		±•0	V
E_{AS}	Single Pulsed Avalanche Energy	②	86	mJ
I_{AR}	Avalanche Current	①	10	A
E_{AR}	Repetitive Avalanche Energy	①	3.1	mJ
dv/dt	Peak Diode Recovery dv/dt	③	5.5	V/ns
P_D	Total Power Dissipation (T_C=25°C)		31	W
	Linear Derating Factor		0.21	• •°C
T_J , T_{STG}	Operating Junction and Storage Temperature Range		- 55 to +175	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds		300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	4.84	°C/W
$R_{\theta CS}$	Case-to-Sink	0.5	--	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

SAMSUNG ELECTRONICS

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	60	–	–	V	V_{GS}=0V,I_D=250 μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	–	0.047	–	V/°C	I_D=250 μA *See Fig 7*
$V_{GS(th)}$	Gate Threshold Voltage	1.0	–	2.0	V	V_{DS}=5V,I_D=250 μA
I_{GSS}	Gate-Source Leakage , Forward	–	–	100	nA	V_{GS}=20V
	Gate-Source Leakage , Reverse	–	–	-100		V_{GS}=-20V
I_{DSS}	Drain-to-Source Leakage Current	–	–	10	μA	V_{DS}=60V
		–	–	100		V_{DS}=48V,T_C=150°C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	–	–	0.155	Ω	V_{GS}=5V,I_D=5A ④
g_{fs}	Forward Transconductance	–	5.5	–	℧	V_{DS}=30V,I_D=5A ④
C_{iss}	Input Capacitance	–	265	345	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz *See Fig 5*
C_{oss}	Output Capacitance	–	100	115		
C_{rss}	Reverse Transfer Capacitance	–	37	45		
$t_{d(on)}$	Turn-On Delay Time	–	10	30	ns	V_{DD}=30V,I_D=10A, R_G=12 Ω *See Fig 13* ④ ⑤
t_r	Rise Time	–	16	45		
$t_{d(off)}$	Turn-Off Delay Time	–	21	55		
t_f	Fall Time	–	15	40		
Q_g	Total Gate Charge	–	7.2	10	nC	V_{DS}=48V,V_{GS}=5V, I_D=10A *See Fig 6 & Fig 12* ④ ⑤
Q_{gs}	Gate-Source Charge	–	2.6	–		
Q_{gd}	Gate-Drain("Miller") Charge	–	3.2	–		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	–	–	10	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	–	–	35		
V_{SD}	Diode Forward Voltage ④	–	–	1.5	V	T_J=25°C,I_S=10A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	–	50	–	ns	T_J=25°C,I_F=10A
Q_{rr}	Reverse Recovery Charge	–	0.075	–	μC	di_F/dt=100A/μs ④

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperatur
② L=1mH, I_{AS}=10A, V_{DD}=25V, R_G=27Ω, Starting T_J=25°C
③ $I_{SD} \le$ 10A, di/dt ≤200A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J=25 °C
④ Pulse Test : Pulse Width = 250 μs, Duty Cycle ≤2%
⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

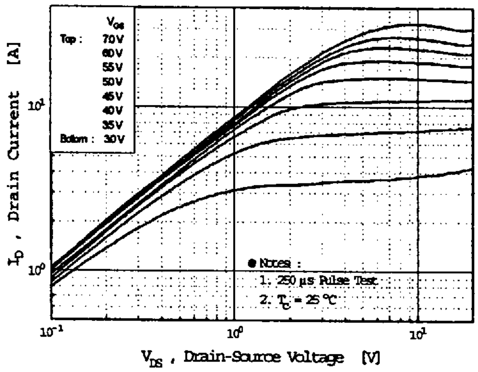


Fig 2. Transfer Characteristics

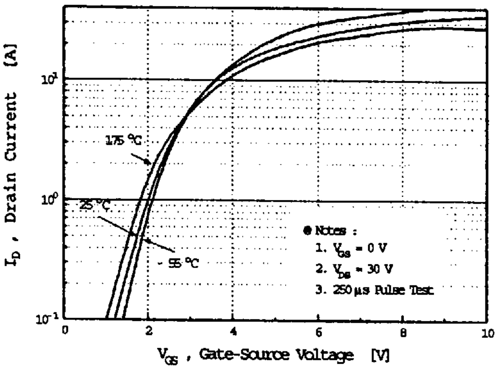


Fig 3. On-Resistance vs. Drain Current

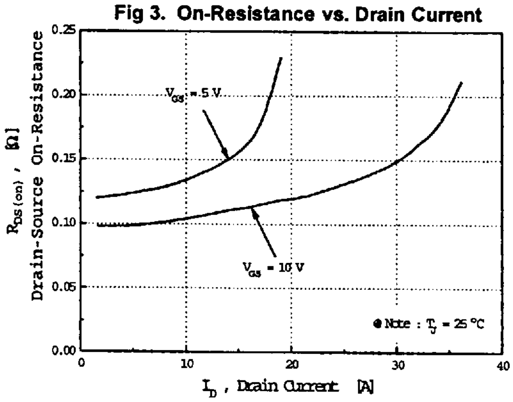


Fig 4. Source-Drain Diode Forward Voltage

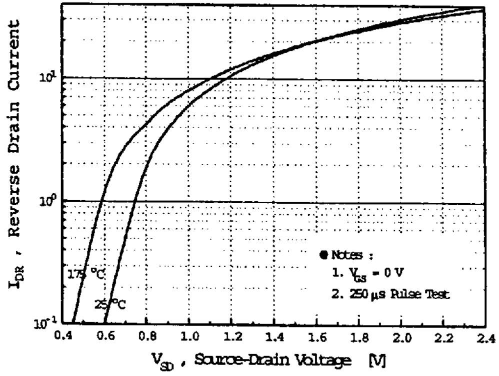


Fig 5. Capacitance vs. Drain-Source Voltage

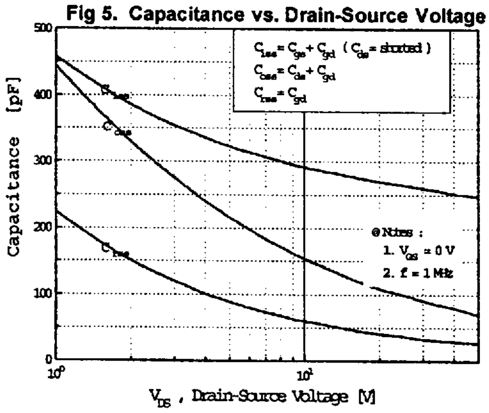


Fig 6. Gate Charge vs. Gate-Source Voltage

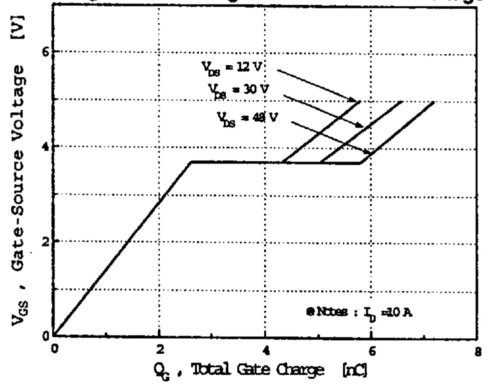


Fig 7. Breakdown Voltage vs. Temperature

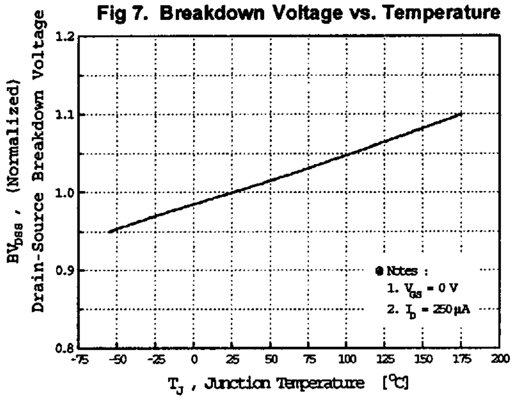


Fig 8. On-Resistance vs. Temperature

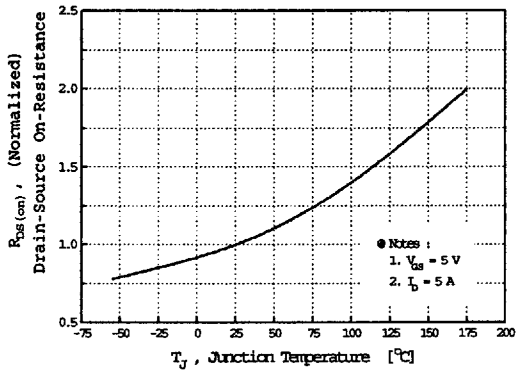


Fig 9. Max. Safe Operating Area

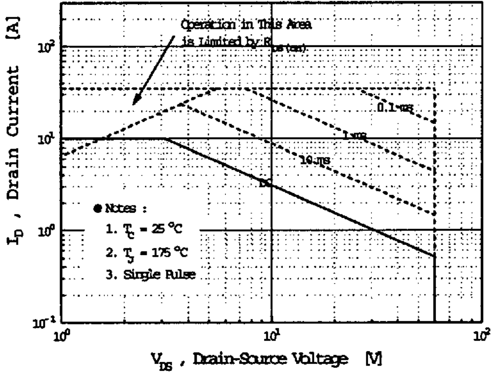


Fig 10. Max. Drain Current vs. Case Temperature

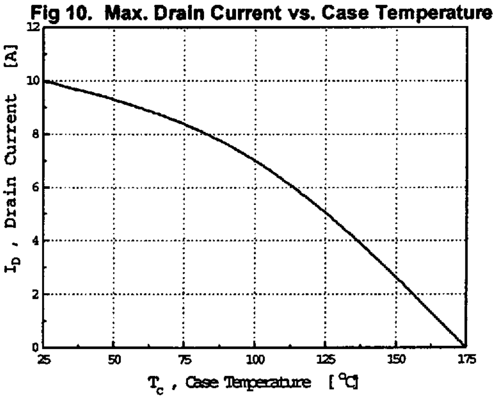


Fig 11. Thermal Response

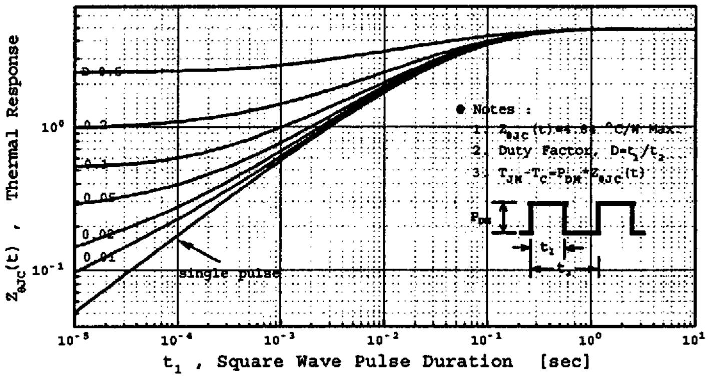


Fig 12. Gate Charge Test Circuit & Waveform

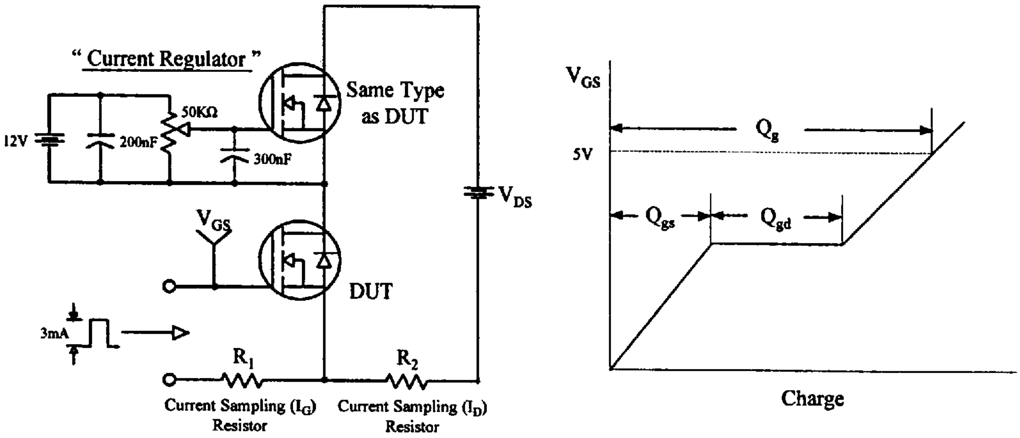


Fig 13. Resistive Switching Test Circuit & Waveforms

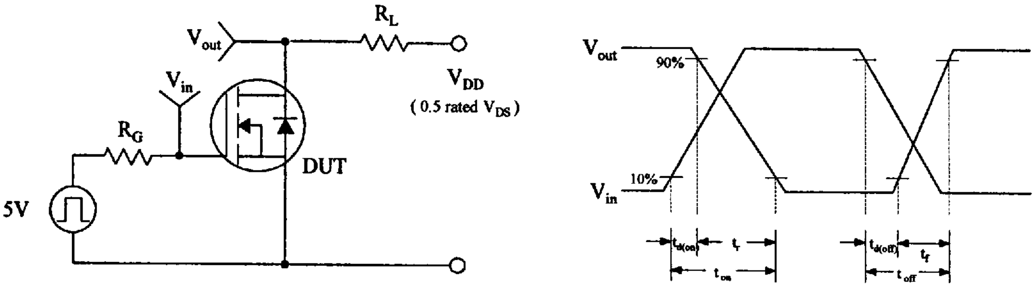


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

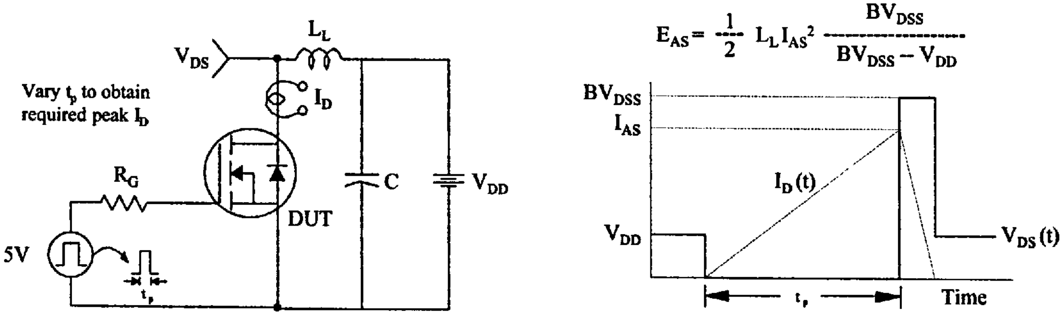
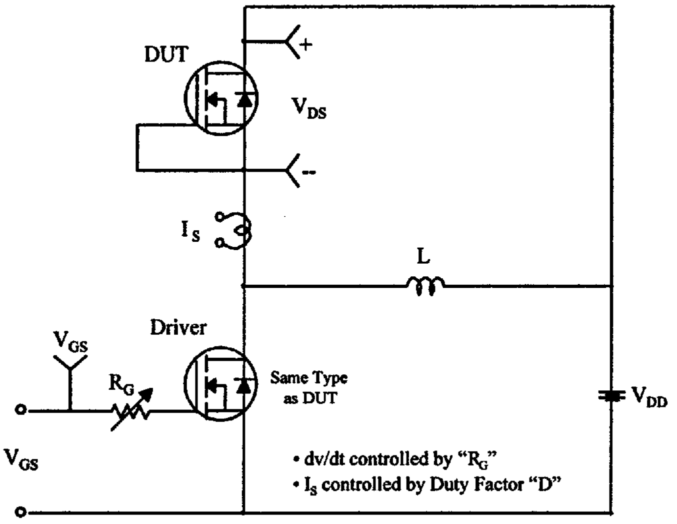
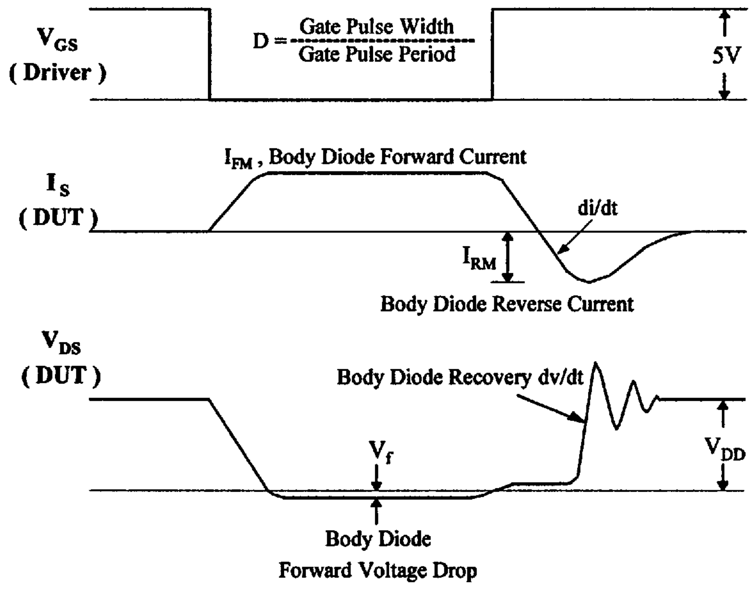


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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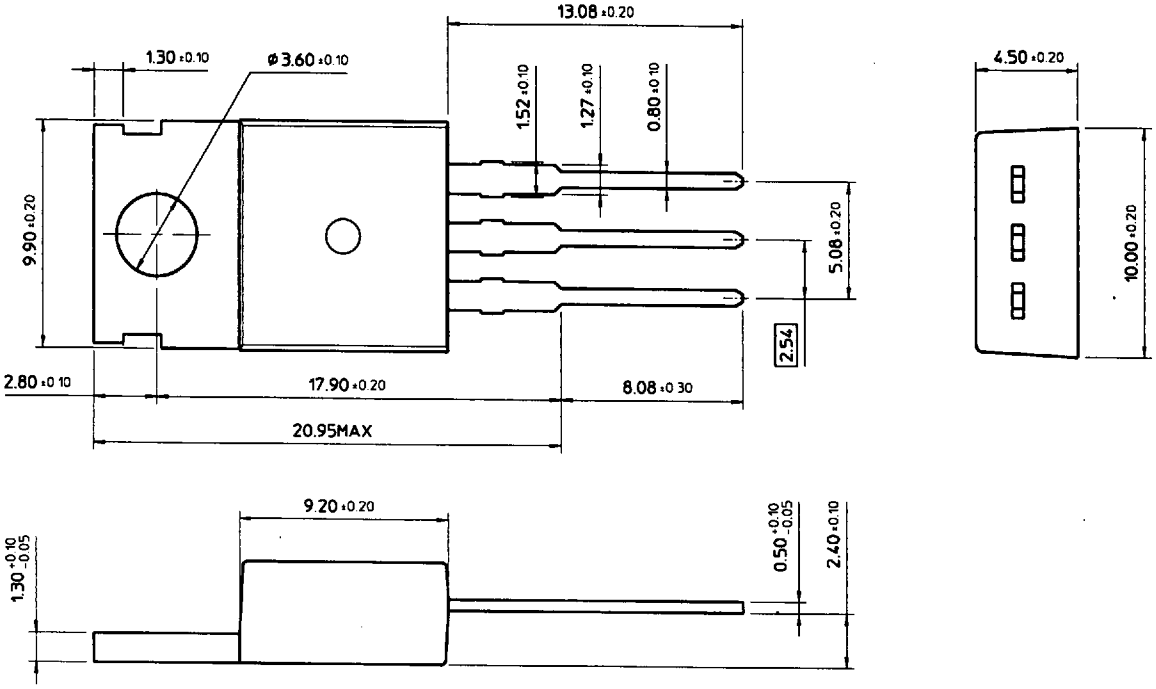
TO-220 (1)



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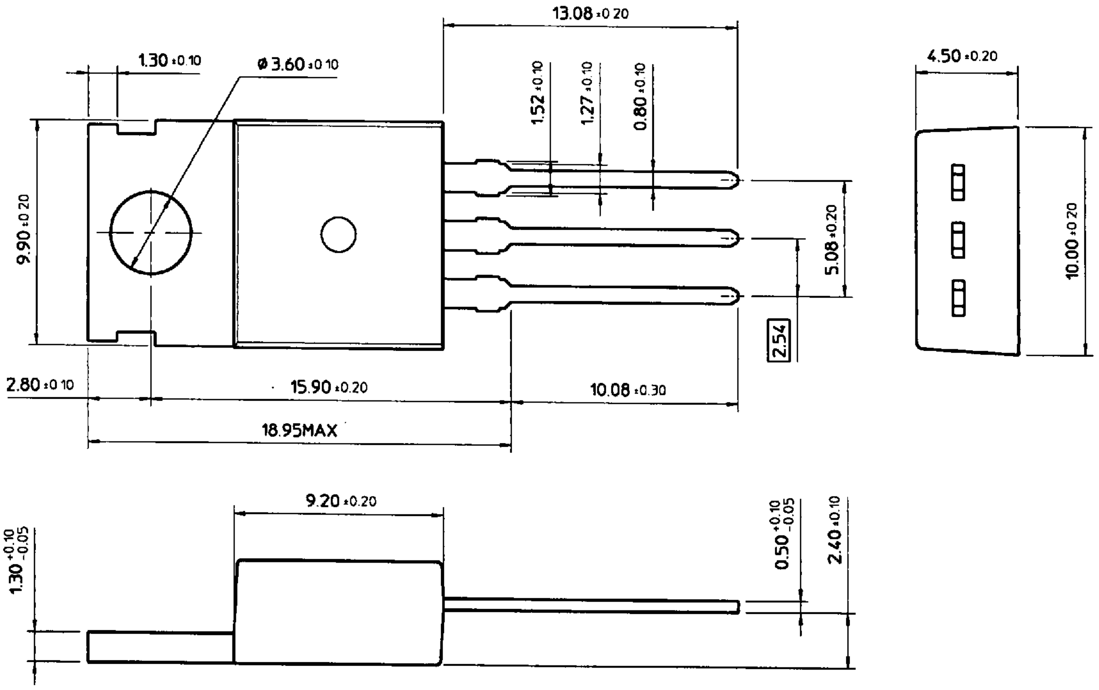

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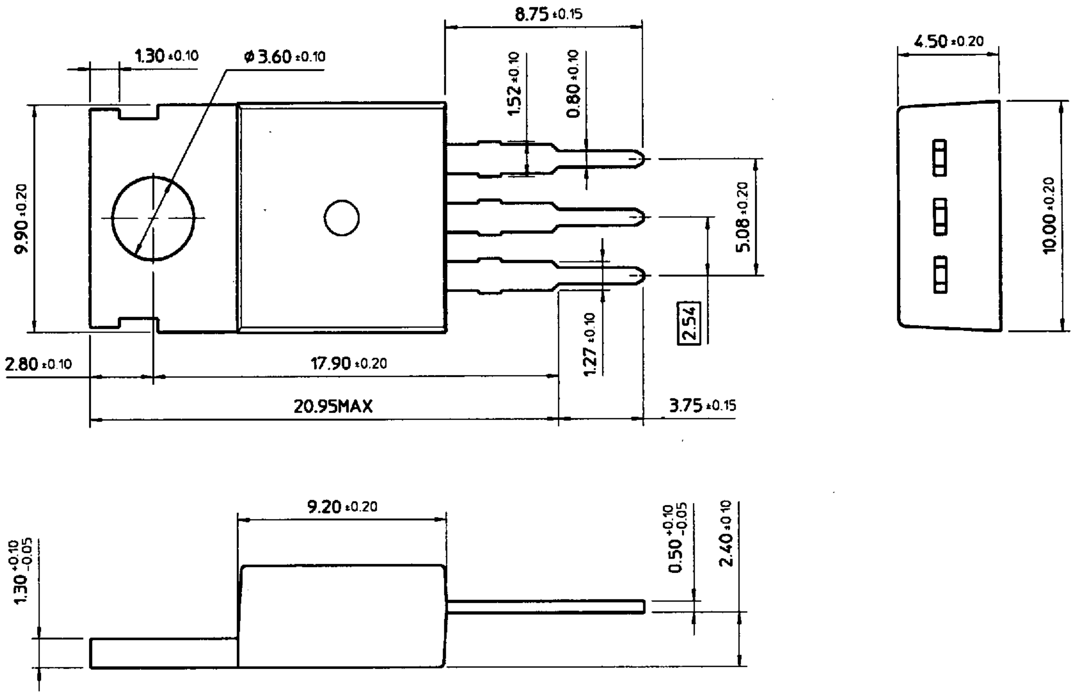

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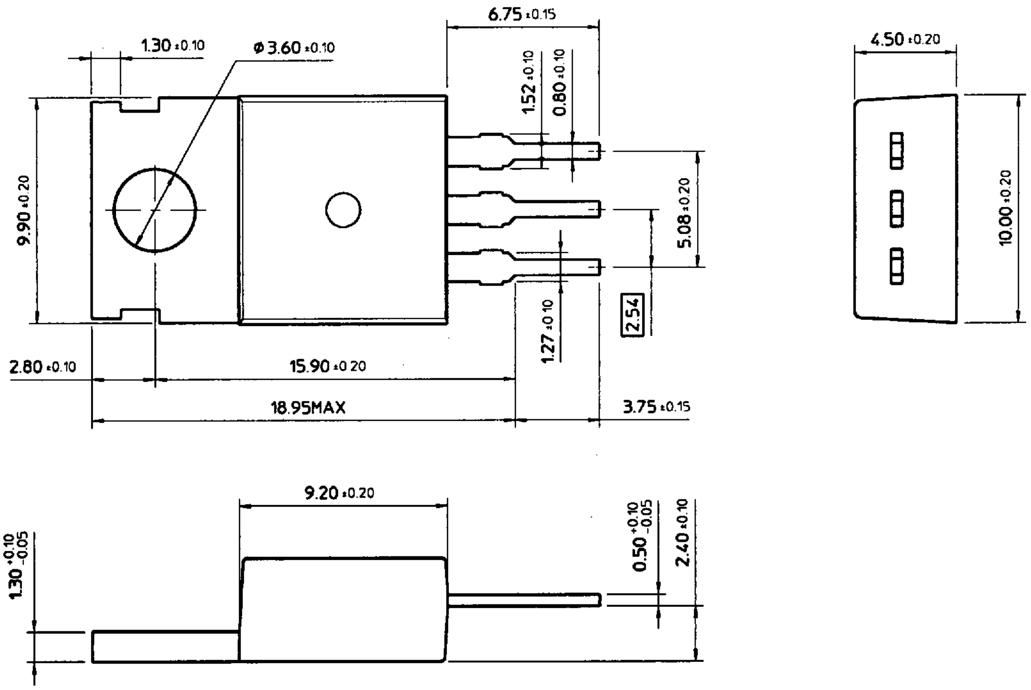

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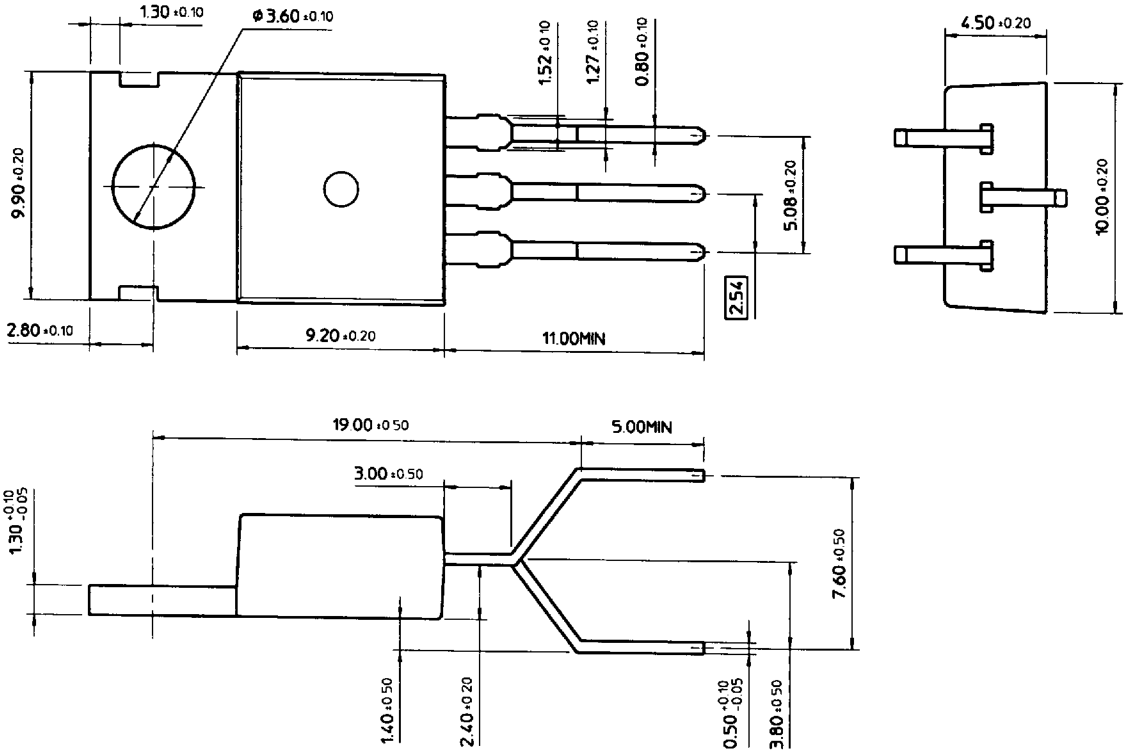
1.30±0.10
Φ3.60±0.10
1.52±0.10
1.27±0.10
0.80±0.10
4.50±0.20
9.90±0.20
5.08±0.20
10.00±0.20
2.54
2.80±0.10
9.20±0.20
11.00MIN
19.00±0.50
5.00MIN
3.00±0.50
1.30 +0.10 -0.05
7.60±0.50
1.40±0.50
2.40±0.20
0.50 +0.10 -0.05
3.80±0.50

NOTE