128Mx72 bits
PC133 SDRAM Registered DIMM
with PLL, based on 64Mx4 SDRAM with LVTTL, 4 banks & 8K Refresh
HYM72V12C736B(L)S4 Series

DESCRIPTION

The HYM72V12C736B(L)S4 Series are 128Mx72bits ECC Synchronous DRAM Modules. The modules are composed of thirty six 64Mx4bits CMOS Synchronous DRAMs in 400mil 54pin TSOP-II stack package, one 2Kbit EEPROM in 8pin TSSOP package on a 168pin glass-epoxy printed circuit board. One 0.22uF and one 0.0022uF decoupling capacitors per each SDRAM are mounted on the PCB.

The HYM72V12C736B(L)S4 Series are Dual In-line Memory Modules suitable for easy interchange and addition of 1Gbytes memory. The HYM72V12C736B(L)S4 Series are fully synchronous operation referenced to the positive edge of the clock . All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

FEATURES

- PC133MHz support
- 168pin SDRAM Registered DIMM
- Serial Presence Detect with EEPROM
- 1.70” (43.18mm) Height PCB with double sided components
- Single 3.3±0.3V power supply
- All device pins are compatible with LVTTL interface
- Data mask function by DQM
- SDRAM internal banks : four banks
- Module bank : two physical banks
- Auto refresh and self refresh
- 8192 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4 or 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

ORDERING INFORMATION

Part No.	Clock Frequency	Internal Bank	Ref.	Power	SDRAM Package	Plating
HYM72V12C736BS4-K	133MHz	4 Banks	8K	Normal	TSOP-II	Gold
HYM72V12C736BS4-H						
HYM72V12C736BLS4-K				Low Power		
HYM72V12C736BLS4-H						

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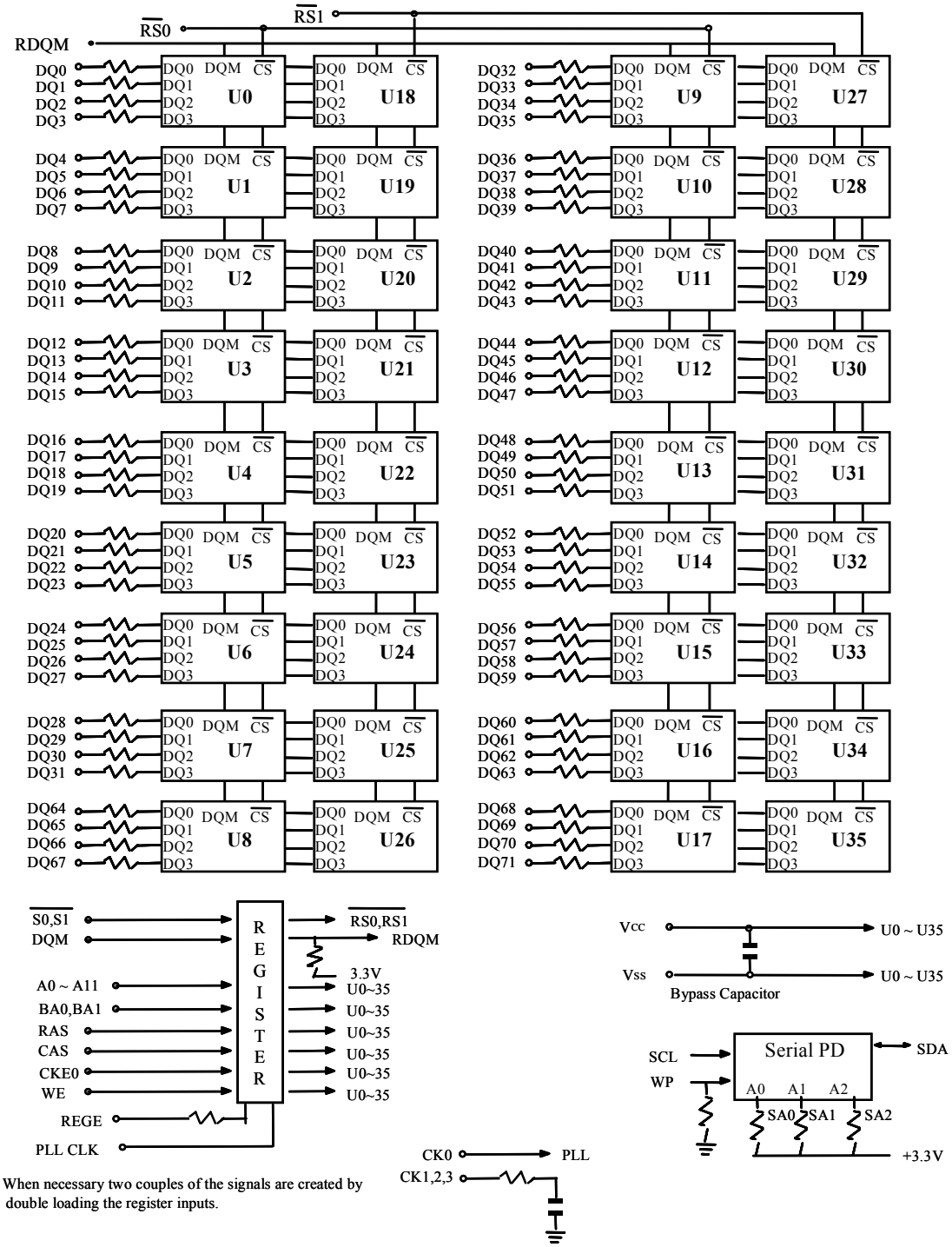
PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CK0	Clock Inputs	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE0	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
/S0 ~ /S3	Chip Select	Enables or disables all inputs except CK, CKE and DQM
BA0, BA1	SDRAM Bank Address	Selects bank to be activated during /RAS activity Selects bank to be read/written during /CAS activity
A0 ~ A12	Address	Row Address : RA0 ~ RA12, Column Address : CA0 ~ CA9, CA11 Auto-precharge flag : A10
/RAS, /CAS, /WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation Refer function truth table for details
REGE	Register Enable	Register Enable pin which permits the DIMM to operateion in Buffered Mode when REGE input is Low, in Registered Mode when REGE input is High
DQM0 ~ 7	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ63	Data Input/Output	Multiplexed data input / output pin
VCC	Power Supply (3.3V)	Power supply for internal circuits and input buffers
VSS	Ground	Ground
SCL	SPD Clock Input	Serial Presence Detect Clock input
SDA	SPD Data Input/Output	Serial Presence Detect Data input/output
SA0~2	SPD Address Input	Serial Presence Detect Address Input
WP	Write Protect for SPD	Write Protect for Serial Presence Detect on DIMM
ID1~3	Identification Detect	Commend Interval, Read Precharge Timing, Power Detect
NC	No Connection	No connection

PIN ASSIGNMENTS

FRONT SIDE		BACK SIDE		FRONT SIDE		BACK SIDE	
PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VSS	85	VSS	41	VCC	125	NC
2	DQ0	86	DQ32	42	CK0	126	A12
3	DQ1	87	DQ33	43	VSS	127	VSS
4	DQ2	88	DQ34	44	NC	128	CKE0
5	DQ3	89	DQ35	45	/S2	129	/S3
6	VCC	90	VCC	46	DQM2	130	DQM6
7	DQ4	91	DQ36	47	DQM3	131	DQM7
8	DQ5	92	DQ37	48	NC	132	NC
9	DQ6	93	DQ38	49	VCC	133	VCC
10	DQ7	94	DQ39	50	NC	134	NC
Architecture Key				51	NC	135	NC
				52	CB2	136	CB6
11	DQ8	95	DQ40	53	CB3	137	CB7
12	VSS	96	VSS	54	VSS	138	VSS
13	DQ9	97	DQ41	55	DQ16	139	DQ48
14	DQ10	98	DQ42	56	DQ17	140	DQ49
15	DQ11	99	DQ43	57	DQ18	141	DQ50
16	DQ12	100	DQ44	58	DQ19	142	DQ51
17	DQ13	101	DQ45	59	VCC	143	VCC
18	VCC	102	VCC	60	DQ20	144	DQ52
19	DQ14	103	DQ46	61	NC	145	NC
20	DQ15	104	DQ47	62	NC	146	NC
21	CB0	105	CB4	63	NC	147	REGE
22	CB1	106	CB5	64	VSS	148	VSS
23	VSS	107	VSS	65	DQ21	149	DQ53
24	NC	108	NC	66	DQ22	150	DQ54
25	NC	109	NC	67	DQ23	151	DQ55
26	VCC	110	VCC	68	VCC	152	VCC
27	/WE	111	/CAS	69	DQ24	153	DQ56
28	DQM0	112	DQM4	70	DQ25	154	DQ57
29	DQM1	113	DQM5	71	DQ26	155	DQ58
30	/S0	114	/S1	72	DQ27	156	DQ59
31	NC	115	/RAS	73	VCC	157	VCC
32	VSS	116	VSS	74	DQ28	158	DQ60
33	A0	117	A1	75	DQ29	159	DQ61
34	A2	118	A3	76	DQ30	160	DQ62
35	A4	119	A5	77	DQ31	161	DQ63
36	A6	120	A7	78	VSS	162	VSS
37	A8	121	A9	79	CK2	163	*CK3
38	A10/AP	122	BA0	80	NC	164	NC
39	BA1	123	A11	81	WP	165	SA0
40	VCC	124	VCC	82	SDA	166	SA1
Voltage Key				83	SCL	167	SA2
				84	VCC	168	VCC

BLOCK DIAGRAM



SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION		VALUE		NOTE
		-K	-H	-K	-H	
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes		80h		
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes		08h		
BYTE2	Fundamental Memory Type	SDRAM		04h		
BYTE3	# of Row Addresses on This Assembly	13		0Dh		1
BYTE4	# of Column Addresses on This Assembly	11		0Bh		
BYTE5	# of Module Banks on This Assembly	2 Bank		02h		
BYTE6	Data Width of This Assembly	72 Bits		48h		
BYTE7	Data Width of This Assembly (Continued)	-		00h		
BYTE8	Voltage Interface Standard of This Assembly	LVTTL		01h		
BYTE9	SDRAM Cycle Time @/CAS Latency=3	7.5ns	7.5ns	75h	75h	
BYTE10	Access Time from Clock @/CAS Latency=3	5.4ns	5.4ns	54h	54h	
BYTE11	DIMM Configuration Type	ECC		02h		
BYTE12	Refresh Rate/Type	7.8125us / Self Refresh Supported		82h		
BYTE13	Primary SDRAM Width	x4		04h		
BYTE14	Error Checking SDRAM Width	x4		04h		
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD = 1 CLK		01h		
BYTE16	Burst Lenth Supported	1,2,4,8,Full Page		8Fh		2
BYTE17	# of Banks on Each SDRAM Device	4 Banks		04h		
BYTE18	SDRAM Device Attributes, /CAS Lataency	/CAS Latency=2,3		06h		
BYTE19	SDRAM Device Attributes, /CS Lataency	/CS Latency=0		01h		
BYTE20	SDRAM Device Attributes, /WE Lataency	/WE Latency=0		01h		
BYTE21	SDRAM Module Attributes	Registered/Buffered inputs, with PLL		1Fh		
BYTE22	SDRAM Device Attributes, General	+/- 10% voltage tolerence, Burst Read Single Bit Write, Precharge All, Auto Precharge, Early RAS Precharge		0Eh		
BYTE23	SDRAM Cycle Time @/CAS Latency=2	7.5ns	10ns	75h	A0h	
BYTE24	Access Time from Clock @/CAS Latency=2	5.7ns	6ns	54h	60h	
BYTE25	SDRAM Cycle Time @/CAS Latency=1	-	-	00h	00h	
BYTE26	Access Time from Clock @/CAS Latency=1	-	-	00h	00h	
BYTE27	Minimum Row Precharge Time (tRP)	15ns	20ns	0Fh	14h	
BYTE28	Minimum Row Active to Row Active Delay (tRRD)	15ns	15ns	0Fh	0Fh	
BYTE29	Minimum /RAS to /CAS Delay (tRCD)	15ns	20ns	0Fh	14h	
BYTE30	Minimum /RAS Pulse Width (tRAS)	45ns	45ns	2Dh	2Dh	
BYTE31	Module Bank Density	512MB		80h		
BYTE32	Command and Address Signal Input Setup Time	1.5ns	1.5ns	15h	15h	
BYTE33	Command and Address Signal Input Hold Time	0.8ns	0.8ns	08h	08h	
BYTE34	Data Signal Input Setup Time	1.5ns	1.5ns	15h	15h	
BYTE35	Data Signal Input Hold Time	0.8ns	0.8ns	08h	08h	
BYTE36 ~61	Superset Information (may be used in future)	-		00h		
BYTE62	SPD Revision	Intel SPD 1.2B		12h		3, 8
BYTE63	Checksum for Byte 0~62	-		DDh	1Eh	
BYTE64	Manufacturer JEDEC ID Code	Hynix JEDED ID		ADh		
BYTE65 ~71	....Manufacturer JEDEC ID Code	Unused		FFh		
BYTE72	Manufacturing Location	Hynix (Korea Area) HSA (United States Area) HSE (Europe Area) HEJ (Japan Area) HSS(Singapore) ASIA Area		0*h 1*h 2*h 3*h 4*h 5*h		9

Continued

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION		VALUE		NOTE
		-K	-H	-K	-H	
BYTE73	Manufacturer's Part Number (Component)	7 (SDRAM)		37h		4, 5
BYTE74	Manufacturer's Part Number (256Mb based)	2		32h		4, 5
BYTE75	Manufacturer's Part Number (Voltage Interface)	V (3.3V, LVTTL)		56h		4, 5
BYTE76	Manufacturer's Part Number (Memory Width)	1		31h		4, 5
BYTE77	....Manufacturer's Part Number (Memory Width)	2		32h		4, 5
BYTE78	Manufacturer's Part Number (Module Type)	C		43h		4, 5
BYTE79	Manufacturer's Part Number (Data Width)	7		37h		4, 5
BYTE80	....Manufacturer's Part Number (Data Width)	3		33h		4, 5
BYTE81	Manufacturer's Part Number (Refresh, SDRAM Bank)	6 (8K Refresh, 4Banks)		36h		4, 5
BYTE82	Manufacturer's Part Number(Manufacturing Site)	B		42h		4, 5
BYTE83	Manufacturer's Part Number (Package Type)	S		53h		4, 5
BYTE84	Manufacturer's Part Number (Component Configuration)	4 (x4 based)		34h		4, 5
BYTE85	Manufacturer's Part Number (Hyphent)	- (Hyphen)		2Dh		4, 5
BYTE86	Manufacturer's Part Number (Min. Cycle Time)	K	H	4Bh	48h	4, 5
BYTE86 ~90	Manufacturer's Part Number	Blanks		20h		4, 5
BYTE91	Revision Code (for Component)	Process Code		-		4, 6
BYTE92	....Revision Code (for PCB)	Process Code		-		4, 6
BYTE93	Manufacturing Date	Year		-		3, 6
BYTE94	....Manufacturing Date	Work Week		-		3, 6
BYTE95 ~98	Assembly Serial Number	Serial Number		-		6
BYTE99 ~125	Manufacturer Specific Data (may be used in future)	None		00h		
BYTE126	System Frequency Support	refer to note 7		64h		7, 8
BYTE127	Intel Specification Details for 100MHz Support	Refer to Note7		8Fh	8Fh	7, 8
BYTE128 ~256	Unused Storage Locations	-		00h		

Note :
1. The bank address is excluded
2. 1, 2, 4, 8 for Interleave Burst Type
3. BCD adopted
4. ASCII adopted
5. Basically Hynix writes Part No. except for 'HYM' in Byte 73~90 to use the limited 18 bytes from byte 73 to byte 90
6. Not fixed but dependent
7. CK0 connected to DIMM, TBD junction temp, CL2(3) support, Intel defined Concurrent Auto Precharge support
8. Refer to Intel SPD Specification 1.2B
9. Refer to Hynix web site

Byte 82~ 87 for L-Part

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION		VALUE		NOTE
		-K	-H	-K	-H	
BYTE82	Manufacturer's Part Number(Manufacturing Site)	B		42h		4, 5
BYTE83	Manufacturer's Part Number (Power)	L		4Ch		4, 5
BYTE84	Manufacturer's Part Number (Package Type)	S		53h		4, 5
BYTE85	Manufacturer's Part Number (Component Configuration)	4 (x4 based)		34h		4, 5
BYTE86	Manufacturer's Part Number (Hyphent)	- (Hyphen)		2Dh		4, 5
BYTE87	Manufacturer's Part Number (Min. Cycle Time)	K	H	4Bh	48h	4, 5

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1,2
Input Low voltage	VIL	-0.3	0	0.8	V	1,3

Note :
1.All voltages are referenced to VSS = 0V
2.VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3.VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

AC OPERATING TEST CONDITION (TA=0 to 70°C, VDD=3.3±0.3V, VSS=0V)

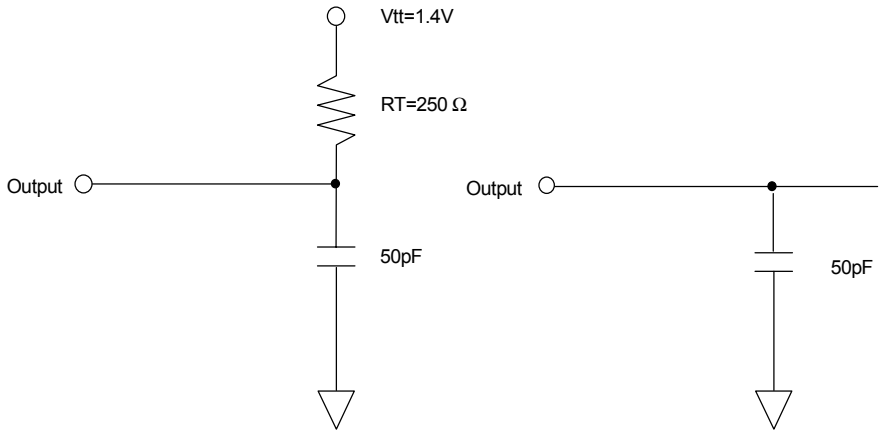
Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note :
1.Output load to measure access times is equivalent to two TTL gates and one capacitor (50pF). For details, refer to AC/DC output load circuit

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	-K/H		Unit
			Min	Max	
Input Capacitance	CK0	C_{I1}	-	20	pF
	CKE0	C_{I2}	-	20	pF
	/S0, /S1, /S2, /S3	C_{I3}	-	20	pF
	A0~12, BA0, BA1	C_{I4}	-	20	pF
	/RAS, /CAS, /WE	C_{I5}	-	20	pF
	DQM0~DQM7	C_{I6}	-	20	pF
Data Input / Output Capacitance	DQ0 ~ DQ63	$C_{I/O}$	-	20	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit

AC Output Load Circuit

DC CHARACTERISTICS I (TA=0 to 70°C, V_{DD}=3.3±0.3V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	I_{LI}	-10	10	uA	1
Output Leakage Current	I_{LO}	-1	1	uA	2
Output High Voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +4mA

Note :
1.V_{IN} = 0 to 3.6V, All other pins are not tested under V_{IN} =0V
2.D_{OUT} is disabled, V_{OUT}=0 to 3.6

DC CHARACTERISTICS II

Parameter	Symbol	Test Condition		Speed -K	Speed -H	Unit	Note
Operating Current	I_{DD1}	Burst length=1, One bank active $t_{RC} \geq t_{RC}$(min), I_{OL}=0mA		**2760**		mA	1
Precharge Standby Current in Power Down Mode	I_{DD2P}	CKE ≤ V_{IL}(max), t_{CK} = min		420		mA	
	I_{DD2PS}	CKE ≤ V_{IL}(max), t_{CK} = ∞		76			
Precharge Standby Current in Non Power Down Mode	I_{DD2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = min Input signals are changed one time during 2clks. All other pins ≥ V_{DD}-0.2V or ≤ 0.2V		1100		mA	
	I_{DD2NS}	CKE ≥ V_{IH}(min), t_{CK} = ∞ Input signals are stable.		360			
Active Standby Current in Power Down Mode	I_{DD3P}	CKE ≤ V_{IL}(max), t_{CK} = min		282		mA	
	I_{DD3PS}	CKE ≤ V_{IL}(max), t_{CK} = ∞		108			
Active Standby Current in Non Power Down Mode	I_{DD3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = min Input signals are changed one time during 2clks. All other pins ≥ V_{DD}-0.2V or ≤ 0.2V		1020		mA	
	I_{DD3NS}	CKE ≥ V_{IH}(min), t_{CK} = ∞ Input signals are stable.		450		mA	
Burst Mode Operating Current	I_{DD4}	$t_{CK} \geq t_{CK}$(min), I_{OL}=0mA All banks active		**3500**		mA	1
Auto Refresh Current	I_{DD5}	$t_{RRC} \geq t_{RRC}$(min), All banks active		**4800**		mA	2
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	Normal	550		mA	3
			Low power	156		mA	4

Note :
1. I_{DD1} and I_{DD4} depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
3. HYM72V12C736BS4 - K/H
4. HYM72V12C736BLS4 - K/H

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-K		-H		Unit	Note
			Min	Max	Min	Max		
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	tCK3	7.5	1000	7.5	1000	ns	
	$\overline{CAS}$ Latency = 2	tCK2	7.5		10		ns	
Clock High Pulse Width		tCHW	2.5	-	2.5	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	2.5	-	ns	1
Access Time From Clock	$\overline{CAS}$ Latency = 3	tAC3	-	5.4	-	5.4	ns	2
	$\overline{CAS}$ Latency = 2	tAC2	-	5.4	-	6	ns	
Data-Out Hold Time		tOH	2.7	-	2.7	-	ns	
Data-Input Setup Time		tDS	1.5	-	1.5	-	ns	1
Data-Input Hold Time		tDH	0.8	-	0.8	-	ns	1
Address Setup Time		tAS	1.5	-	1.5	-	ns	1
Address Hold Time		tAH	0.8	-	0.8	-	ns	1
CKE Setup Time		tCKS	1.5	-	1.5	-	ns	1
CKE Hold Time		tCKH	0.8	-	0.8	-	ns	1
Command Setup Time		tCS	1.5	-	1.5	-	ns	1
Command Hold Time		tCH	0.8	-	0.8	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	1	-	ns	
CLK to Data Output in High-Z Time	$\overline{CAS}$ Latency = 3	tOHZ3	2.7	5.4	2.7	5.4	ns	
	$\overline{CAS}$ Latency = 2	tOHZ2	2.7	5.4	3	6	ns	

Note :

1. In Registered DIMM, data is delayed an additional clock cycle due to the register (this is, Device CL + 1 = DIMM CL)
2. Assume tR / tF (input rise and fall time) is 1ns, If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter
3. Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v
   If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter

AC CHARACTERISTICS II

Parameter		Symbol	-K		-H		Unit	Note
			Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	60	-	65	-	ns	
	Auto Refresh	tRRC	60	-	65	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	15	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	45	100K	45	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	15	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	15	-	15	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	CLK	
Data-In to Precharge Command		tDPL	2	-	2	-	CLK	
Data-In to Active Command		tDAL	5	-	5	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	CLK	
Precharge to Data Output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ3	3	-	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ2	2	-	2	-	CLK	
Power Down Exit Time		tPDE	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	ms	

Note :
1. Timing delay due to the register is considered in a registered DIMM
2. A new command can be given tRRC after self refresh exit

DEVICE OPERATING OPTION TABLE

HYM72V12C736B(L)S4-K

	$\overline{\text{CAS}}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	2CLKs	2CLKs	6CLKs	8CLKs	2CLKs	5.4ns	2.7ns
125MHz(8ns)	2CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

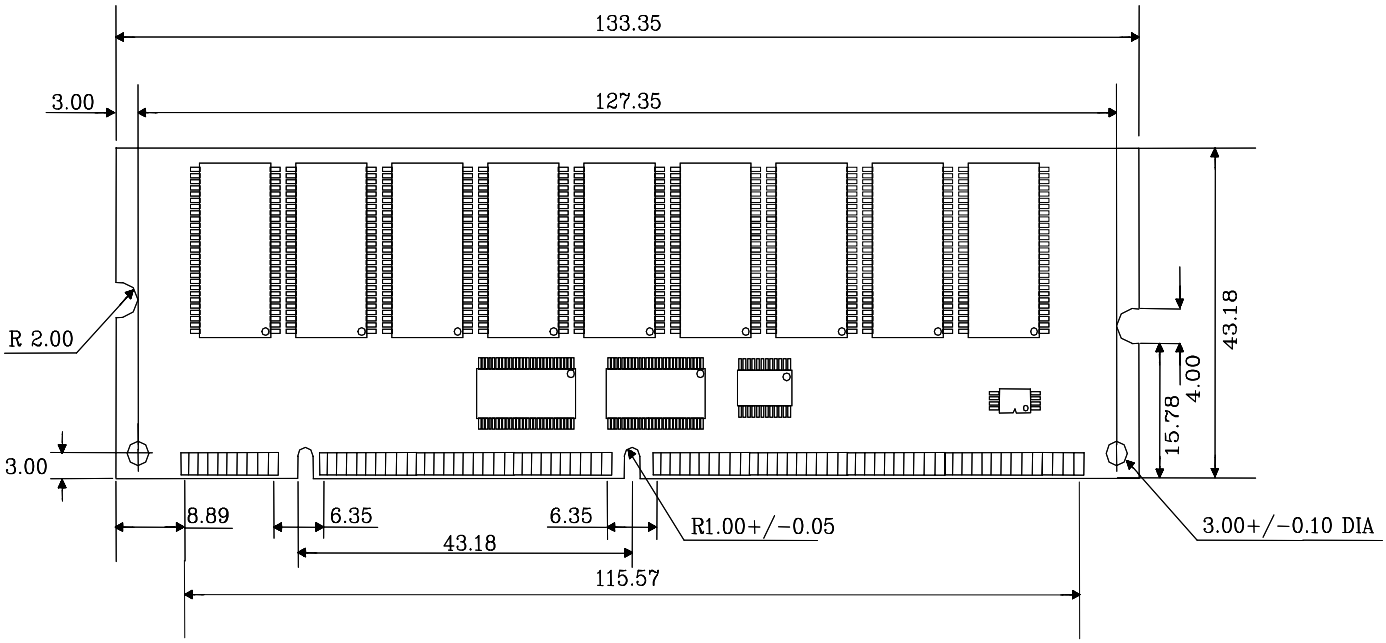
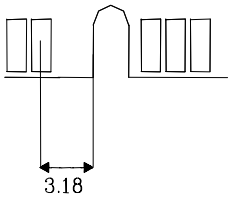
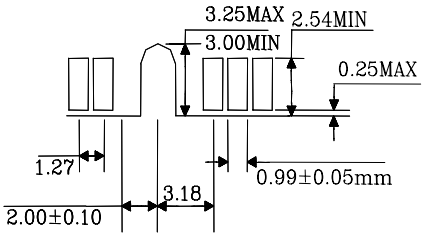
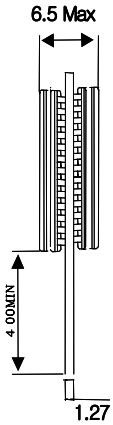
HYM72V12C736B(L)S4-H

	$\overline{\text{CAS}}$ Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

Note : DIMM/CAS Latency = Device CL + 1 (Registered Mode)

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/ AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Burst-Read-Single-WRITE		H	X	L	L	L	H	X	A9 Pin High (Other Pins OP code)			
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note :
1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation

PACKAGE DEMENSION