## 256K × 9-Bit Dynamic RAM Module — HYM 39500S-80

**Advance Information**

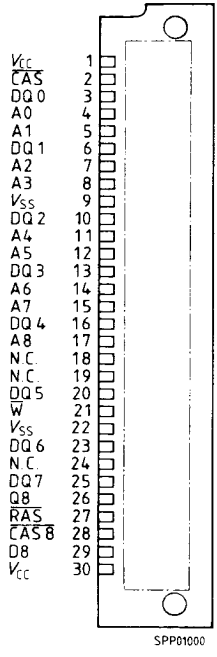
- 262 144 words by 9-bit organization
- Fast access and cycle time
  80 ns access time
  150 ns cycle time
- Fast page mode capability with
  55 ns cycle time
- Single + 5 V (± 10 %) supply
- Common $\overline{CAS}$ control for eight common data-in and data-out lines
- Low power dissipation
  max. 1100 mW active
  CMOS – 31.5 mW standby
  TTL – 52.5 mW standby
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only-refresh, hidden-refresh
- Separate $\overline{CAS}$ control for ninth bit
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single in-Line Memory Module (L-SIM-30-600)
- Pin configuration and outline dimensions according to JEDEC MO-064 with 15.24 mm module height
- Utilizes two 256K × 4 DRAMs in SOJ and one 256K × 1 DRAM in PL-CC-packages
- 512 refresh cycles/8 ms

The HYM 39500S-80 is a 2 Mbit RAM module organized as 262 144 words by 9-bit in a 30-pin single in-line package comprising two HYB 514256AJ 256K × 4 DRAMs in SOJ package and one 256K × 1 DRAM in PL-CC-package mounted together with three 0.2 µF multilayer ceramic decoupling capacitors on a PC board.
A common $\overline{CAS}$ controls for eight common data-in and data-out lines. Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{CAS8}$.
The common I/O feature on the HYM 39500S-80 dictates the use of early write cycles to prevent contention on D and Q.

## Ordering Information

| Type | Ordering code | Package | Description |
|---|---|---|---|
| HYM 39500S-80 | Q67100-Q484 | L-SIM-30-600<br>JEDEC MO-064 | DRAM module<br>(80 ns access time) |

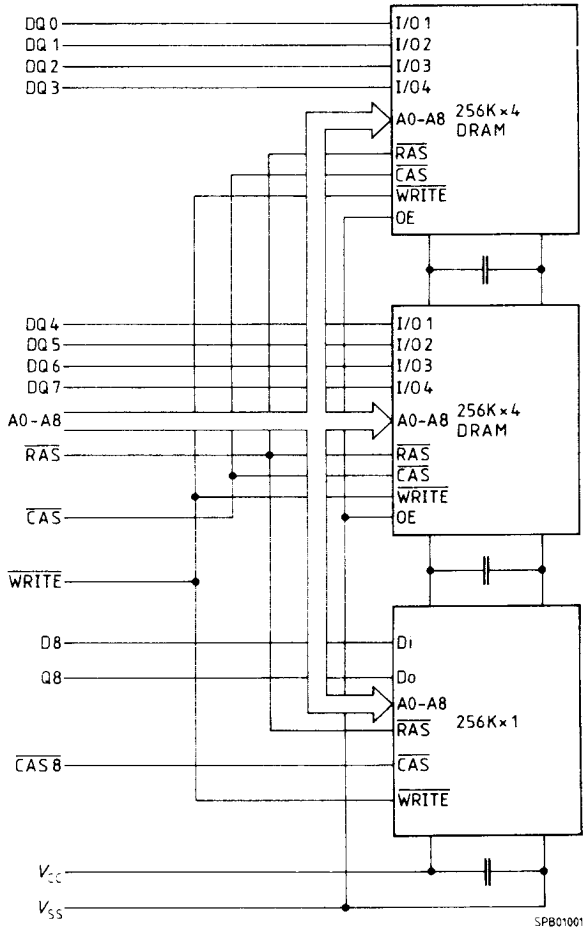
### Pin Configuration




### Pin Names

| | |
|---|---|
| A0-A8 | Address Inputs |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| WRITE | Read/Write Input |
| DQ0-DQ7 | Data Input/Output |
| D8 | Data In |
| Q8 | Data Out |
| CAS8 | Column Address Strobe |
| $V_{CC}$ | Power Supply (+ 5 V) |
| $V_{SS}$ | Ground (0 V) |
| N.C. | No Connection |

## Block Diagram



## Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperatur ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 1.7 W
Data out current (short circuit) ..... 50 mA

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC Characteristics

$T_A$ = 0 to 70 °C, $V_{SS}$ = 0V, $V_{CC}$ = 5V ± 10%

| Symbol | Parameter | Limit values | | Unit | Test condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| $V_{IH}$ | Input high voltage | 2.4 | 6.5 | V | – |
| $V_{IL}$ | Input low voltage | – 1.0 | 0.8 | V | – |
| $V_{OH}$ | Output high voltage ($I_{OUT}$ = – 5mA) | 2.4 | – | V | – |
| $V_{OL}$ | Output low voltage ($I_{OUT}$ = 4.2mA) | – | 0.4 | V | – |
| $I_{I(L)}$ | Input leakage current (0 V ≤ $V_{IN}$ ≤ 6.5 V, all other pins = 0V) | – 20 | 20 | µA | – |
| $I_{O(L)}$ | Output leakage current (DO is disabled, 0 V ≤ $V_{OUT}$ ≤ 5.5V) | – 20 | 20 | µA | – |
| $I_{CC1}$ | Average $V_{CC}$ supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: $t_{RC}$ = $t_{RC}$ min.) | – | 190 | mA | 1) 2) 3) |
| $I_{CC2}$ | Standby $V_{CC}$ supply current ($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | – | 7.5 | mA | 1) |
| $I_{CC3}$ | Average $V_{CC}$ supply current, during $\overline{RAS}$ only refresh cycles: ($\overline{RAS}$ cycling, $\overline{CAS}$ = $V_{IH}$, $t_{RC}$ = $t_{RC}$ min.) | – | 190 | mA | 1) 2) 3) |
| $I_{CC4}$ | Average $V_{CC}$ supply current, during $\overline{RAS}$ only fast page mode: ($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ address cycling, $t_{RC}$ = $t_{RC}$ min.) | – | 140 | mA | 1) 2) 3) |
| $I_{CC5}$ | Standby $V_{CC}$ supply current ($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ – 0.2 V) | – | 4.5 | mA | – |
| $I_{CC6}$ | Average $V_{CC}$ supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: ($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC}$ = $t_{RC}$ min.) | – | 190 | mA | 1) |

Notes see page 175.

## AC Characteristics

$T_A$ = 0 to 70°C, $V_{CC}$ = 5V ± 10%, $t_T$ = 5ns

| Symbol | Parameter | | Limit values | | Unit |
|---|---|---|---|---|---|
| | | | min. | max. | |
| $t_{RC}$ | Random read or write cycle time | | 150 | – | ns |
| $t_{PC}$ | Fast page mode cycle time | | 55 | – | ns |
| $t_{RAC}$ | Access time from $\overline{RAS}$ | 6) 11) | – | 80 | ns |
| $t_{CAC}$ | Access time from $\overline{CAS}$ | 6) 11) | – | 20 | ns |
| $t_{AA}$ | Access time from column address | 6) 12) | – | 40 | ns |
| $t_{CPA}$ | Access time from $\overline{CAS}$ precharge | 6) | – | 50 | ns |
| $t_{CLZ}$ | $\overline{CAS}$ to output in low-Z | 6) | 0 | – | ns |
| $t_{OFF}$ | Output buffer turn-off delay | 7) | 0 | 20 | ns |
| $t_T$ | Transition time (rise and fall) | 5) | 3 | 50 | ns |
| $t_{RP}$ | $\overline{RAS}$ precharge time | | 60 | – | ns |
| $t_{RAS}$ | $\overline{RAS}$ pulse width | | 80 | 10000 | ns |
| $t_{RASP}$ | $\overline{RAS}$ pulse width (fast page mode) | | 80 | 16000 | ns |
| $t_{RSH}$ | $\overline{RAS}$ hold time | | 25 | – | ns |
| $t_{CSH}$ | $\overline{CAS}$ hold time | | 80 | – | ns |
| $t_{CAS}$ | $\overline{CAS}$ pulse width | | 25 | 10000 | ns |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ delay time | 11) | 25 | 60 | ns |
| $t_{RAD}$ | $\overline{RAS}$ to column address delay time | 12) | 20 | 40 | ns |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ precharge time | | 15 | – | ns |
| $t_{CP}$ | $\overline{CAS}$ precharge time (fast page mode) | | 10 | – | ns |
| $t_{ASR}$ | Row address setup time | | 0 | – | ns |
| $t_{RAH}$ | Row address hold time | | 15 | – | ns |
| $t_{ASC}$ | Column address setup time | | 0 | – | ns |
| $t_{CAH}$ | Column address hold time | | 15 | – | ns |
| $t_{AR}$ | Column address hold time referenced to $\overline{RAS}$ | | 65 | – | ns |

Notes see page 175.

## AC Characteristics (cont'd)

| Symbol | Parameter | | Limit values | | Unit |
|---|---|---|---|---|---|
| | | | min. | max. | |
| $t_{RAL}$ | Column address to $\overline{RAS}$ lead time | | 40 | – | ns |
| $t_{RCS}$ | Read command setup time | | 0 | – | ns |
| $t_{RCH}$ | Read command hold time | 8) | 0 | – | ns |
| $t_{RRH}$ | Read command hold time referenced to $\overline{RAS}$ | 8) | 0 | – | ns |
| $t_{WCH}$ | Write command hold time | | 15 | – | ns |
| $t_{WCR}$ | Write command hold time referenced to $\overline{RAS}$ | | 65 | – | ns |
| $t_{WP}$ | Write command pulse width | | 15 | – | ns |
| $t_{RWL}$ | Write command to $\overline{RAS}$ lead time | | 25 | – | ns |
| $t_{CWL}$ | Write command to $\overline{CAS}$ lead time | | 25 | – | ns |
| $t_{DS}$ | Data setup time | 9) | 0 | – | ns |
| $t_{DH}$ | Data hold time | 9) | 15 | – | ns |
| $t_{DHR}$ | Data hold time referenced to $\overline{RAS}$ | | 65 | – | ns |
| $t_{REF}$ | Refresh period | | – | 8 | ms |
| $t_{WCS}$ | Write command setup time | | 0 | – | ns |
| $t_{CSR}$ | $\overline{CAS}$ setup time (CBR cycle) | | 10 | – | ns |
| $t_{CHR}$ | $\overline{CAS}$ hold time (CBR cycle) | | 30 | – | ns |
| $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ precharge time | | 0 | – | ns |
| $t_{CPN}$ | $\overline{CAS}$ precharge time | | 15 | – | ns |

Notes see page 175.

## Capacitance

$T_A$ = 0 to 70 °C, $V_{CC}$ = 5V ± 10%, $f$ = 1 MHz

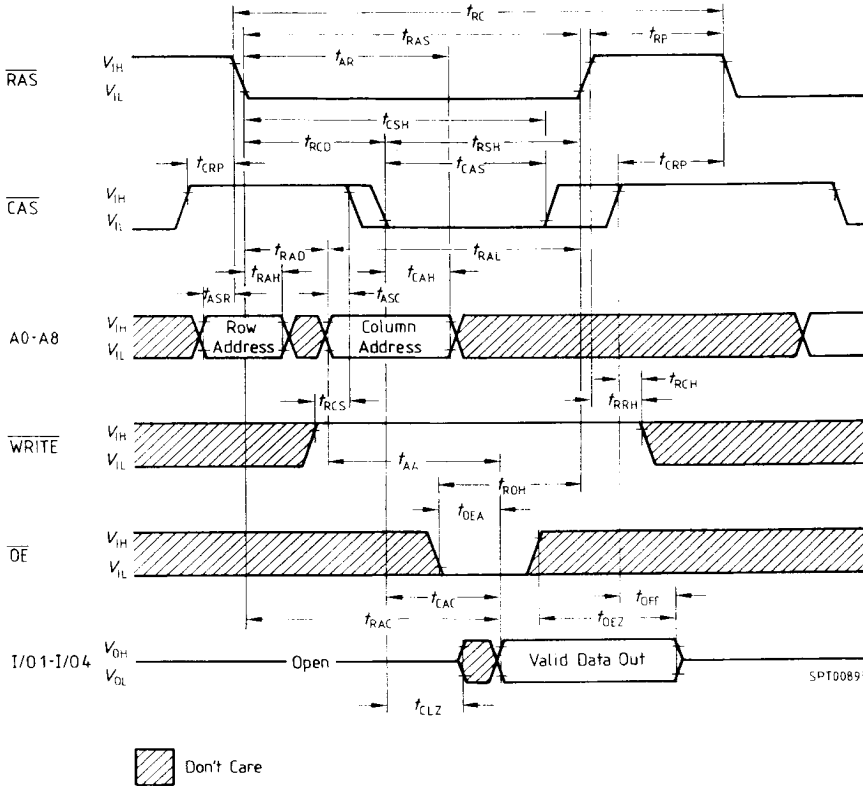
| Symbol | Parameter | Limit values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| $C_{I1}$ | Input capacitance (A0 to A8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) | – | 25 | pF |
| $C_{I2}$ | Input capacitance | – | 10 | pF |
| $C_{IO}$ | I/O capacitance (D0 to D7) | – | 10 | pF |
| $C_O$ | Output capacitance | – | 10 | pF |

**Notes for pages 172 to 174**

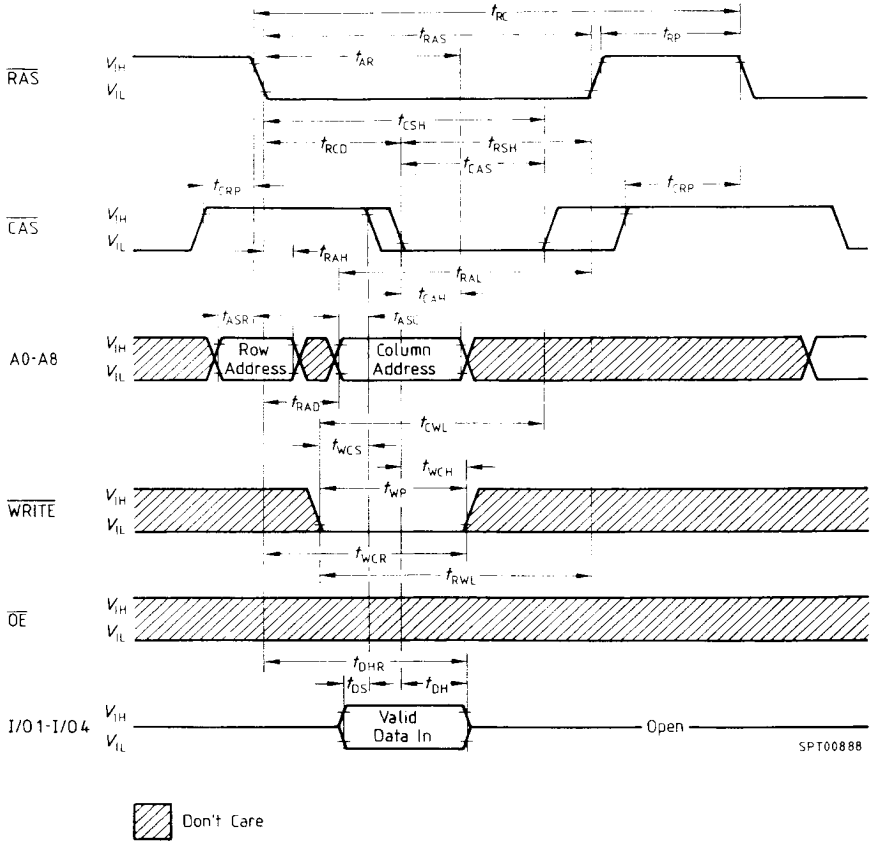
1) All voltages are referenced to $V_{SS}$.
2) $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ depend on cycle rate.
3) $I_{CC1}$ and $I_{CC4}$ depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.
5) $V_{IH}$ (min.) and $V_{IL}$ (max.) are reference levels for measuring timing of input signals. Transition times are also measured between $V_{IH}$ and $V_{IL}$.
6) Measured with a load equivalent of 2 TTL loads and 100pF.
7) $t_{OFF}$ (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
10) $t_{WCS}$ is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open (high impedance).
11) Operation within the $t_{RCD}$ (max.) limit ensures that $t_{RAC}$ (max.) can be met. $t_{RCD}$ (max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max.) limit, then access time is controlled by $t_{CAC}$.
12) Operation within the $t_{RAD}$ (max.) limit ensures that $t_{RAC}$ (max.) can be met. $t_{RAD}$ (max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max.) limit, then access time is controlled by $t_{AA}$.

**Waveformes**

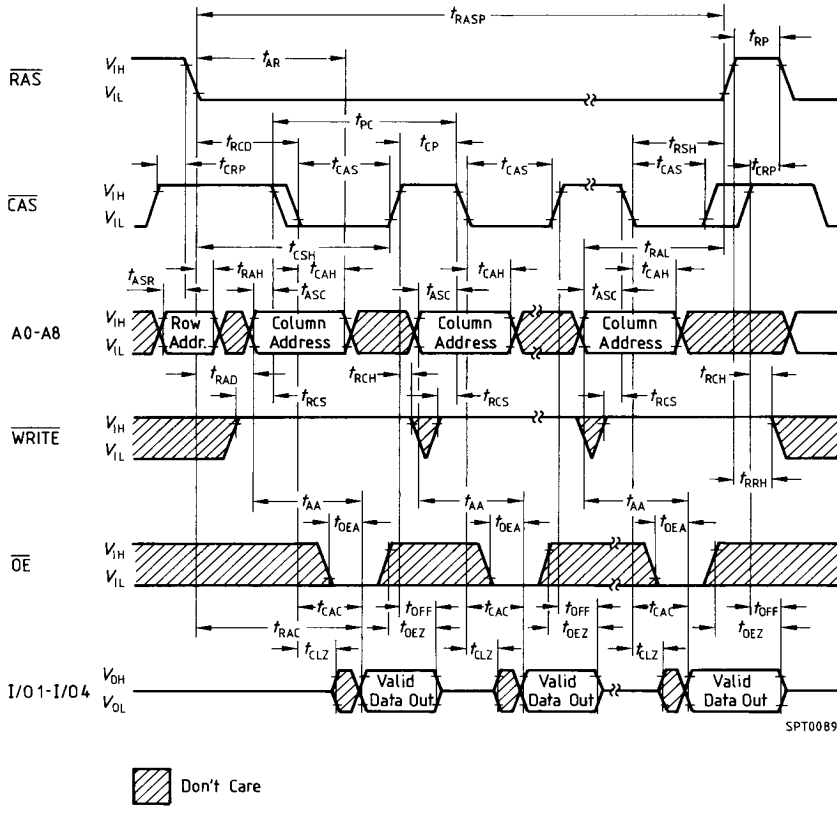
**Read Cycle**



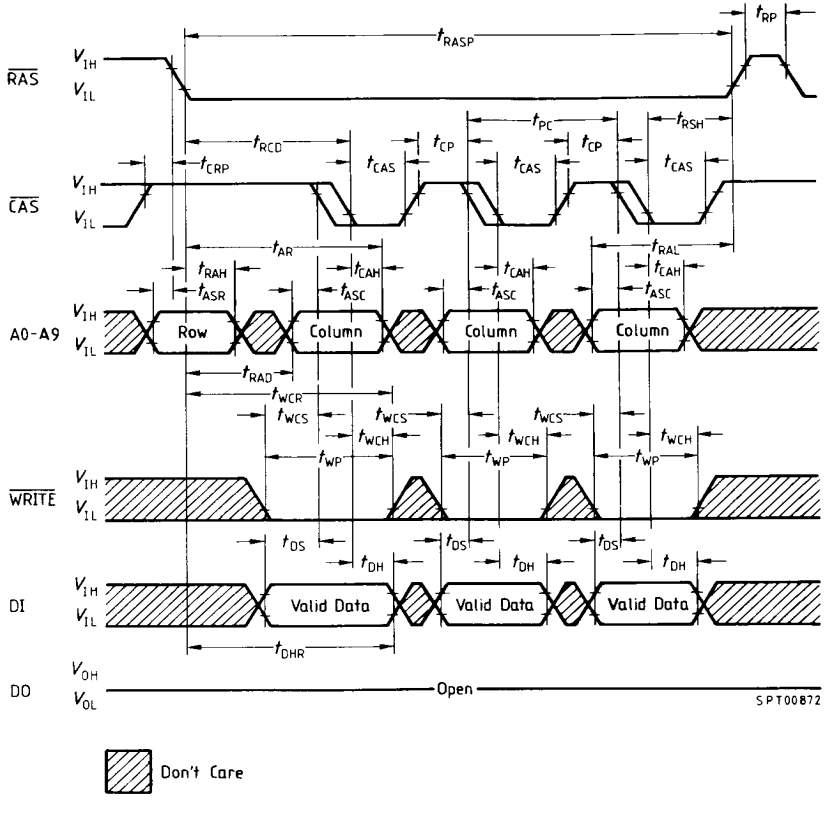
## Write Cycle (early write)



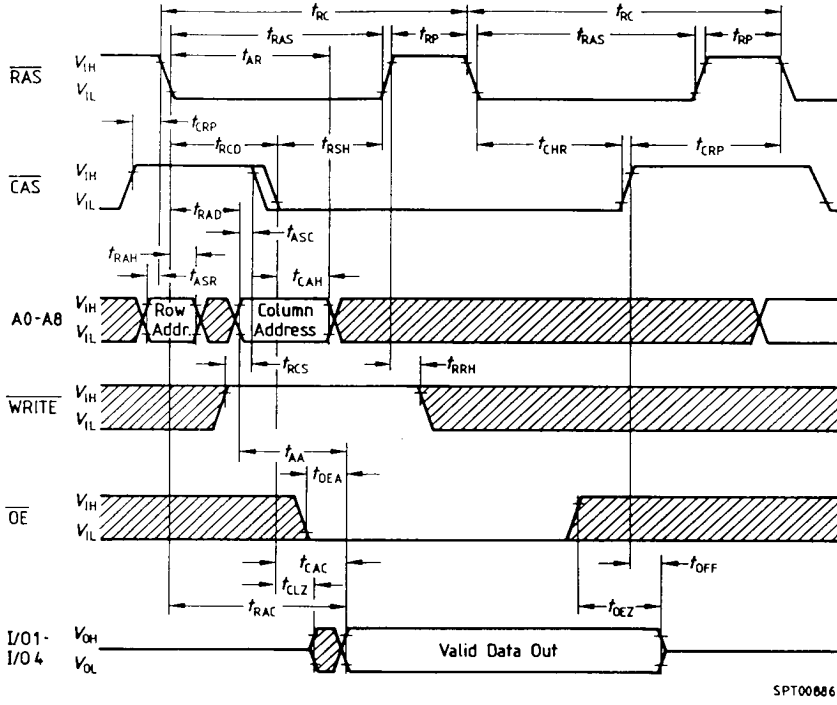
## Fast Page Mode Read Cycle



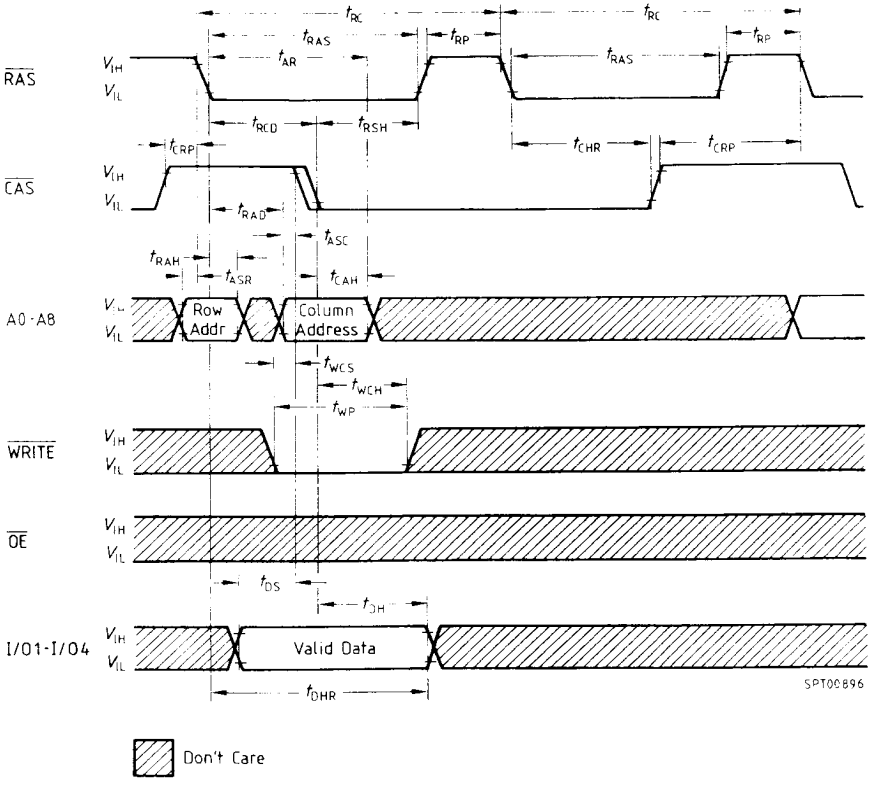
## Fast Page Mode Write Cycle (early write)



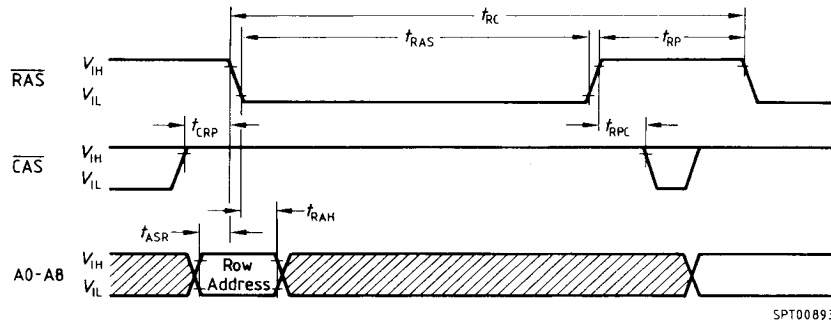
## Hidden Refresh Cycle (Read)



## Hidden Refresh Cycle (Write)

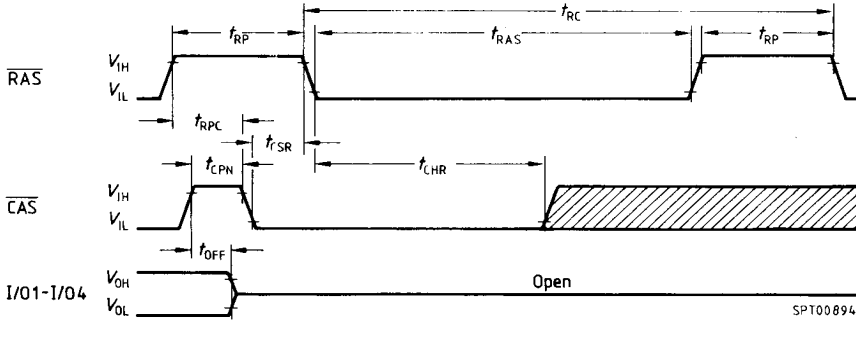


## RAS-Only Refresh Cycle




Don't Care  Note: $\overline{WRITE}$, $\overline{OE}$ = Don't Care

## CAS-Before-RAS Refresh Cycle




Note: $\overline{WRITE}$, $\overline{OE}$, A0-A8 = Don't Care