Marconi
Electronic Devices

5μm CELLMOS DESIGN SYSTEM

FEATURES

* Oxide isolated CMOS technology
* 5 micron design rules
* Typical gate delays 8nS — system speeds of 20 MHz achieved
* 3 - 10V operating voltage range
* 5μW/MHz power dissipation per active gate
* Input/output latch-up immunity 100mA
* Comprehensive CAD design system
* ROM, RAM and Analog functions available

SYSTEM DESCRIPTION

An integrated circuit built using the Marconi's 'CELLMOS' system comprises a 'core' area containing the cells implementing the required logical function, surrounded by a peripheral area containing input and output buffers.

The cells in the core are designed to have a common cell height, the cell width varying depending on the complexity of the cell. The cell width is usually the minimum possible, though this is, in some cases, increased to achieve adequate drive capability. The cells and the interconnect between cells are placed on a regular grid in such a way that design rule infringement is impossible.

A range of standard input and output buffers are available for use in the peripheral areas. These, and the interconnect from them to the core area, are placed on the same grid as the core area for the same reason.

The cell layout method eliminates design faults, giving a much better chance of first time success than with other design methodologies which involve significant human judgement. However, the normal constraints of logic design apply. Circuits must be designed with due attention to race hazards, timing considerations, and testability. Good digital design technique combined with the use of our simulation software and cell libraries, gives the highest probability of first time design success.

A major feature of Marconi's CELLMOS system is its facility to implement analog functions and digital functions on the same chip. Analog switches, analog comparator, voltage reference and operational amplifier are all now available as standard cells and complemented with a range of capacitors and resistors.

Special cells may be configured by Marconi for non-standard functions. For example, special input/output cells could be designed on request. These are not part of the current characterized cell library and naturally would require both additional funding and longer prototype and preproduction scheduling.

Marconi's 'CELLMOS' system runs on Silvar Lisco's CAL-MP layout software with CASS or Mentor Graphic's IDEA series for schematic capture. Simulation is performed using GenRad's HILO-2. This powerful software suite together with Marconi cell libraries can be supplied through Marconi for customers who wish to design their own circuits.

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Integrated Circuits

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ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vdd	11	volts
Positive voltage on any pin		Vdd + 0.3	volts
Negative voltage on any pin		Vss − 0.3	volts
Current through any I/O pin		±10	mA
Power dissipation		Package dependent	

Note: Exceeding the 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only and functional performance under these conditions for extended periods may adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Operating supply voltage	3V − 10V	
Storage temperature*	−65°C to 150°C	
Operating ambient temperature*		
Military	−55°C to +125°C	*Package dependent
Industrial	−40°C to +85°C	
Commercial	0°C to +70°C	

D.C. ELECTRICAL CHARACTERISTICS at 5V and 25°C

Symbol	Parameter	Limit	
Iin	Input leakage	1.0μA/gate	Typically <<100nA
Idd	Static supply current	100μA max	Typically <200nA/1000 gates
STANDARD CMOS INPUTS: BUFFERED			
Vih	Input high volts	3.5V min	
Vil	Input low volts	1.5V max	
STANDARD TTL INPUTS			
Vih	Input high volts	2.0V min	
Vil	Input low volts	0.8V max	
STANDARD CMOS OUTPUTS			
Voh	Output high volts	4.5V min	R_L = 50 Kohms C_L = 50 pF
Vol	Output low volts	0.5V max	R_L = 50 Kohms C_L = 50 pF
STANDARD TTL OUTPUTS			
Voh	Output high volts	2.4V min	at Ioh = −1mA
Vol	Output low volts	0.4V max	at Iol = 2mA

Note: The above data is for Marconi standard input and output cells. For data on 'special cells' please refer to our CELLMOS design namual.

A.C. ELECTRICAL CHARACTERISTICS at 5V and 25°C

Cell name	Function		O/P edge	Inherent delay	Per 1pF load
CIO1	CMOS input/output		rising	12nS	0.85nS
			falling	18nS	0.5nS
NOR2	2 input NOR		rising	7.5nS	18.5nS
			falling	5.5nS	11.5nS
RDT	Reset D type	CK - QB	rising	21.5nS	36.5nS
			falling	26.5nS	36.5nS
	Data set up time	18.5nS			
	Data hold time	15.0nS			

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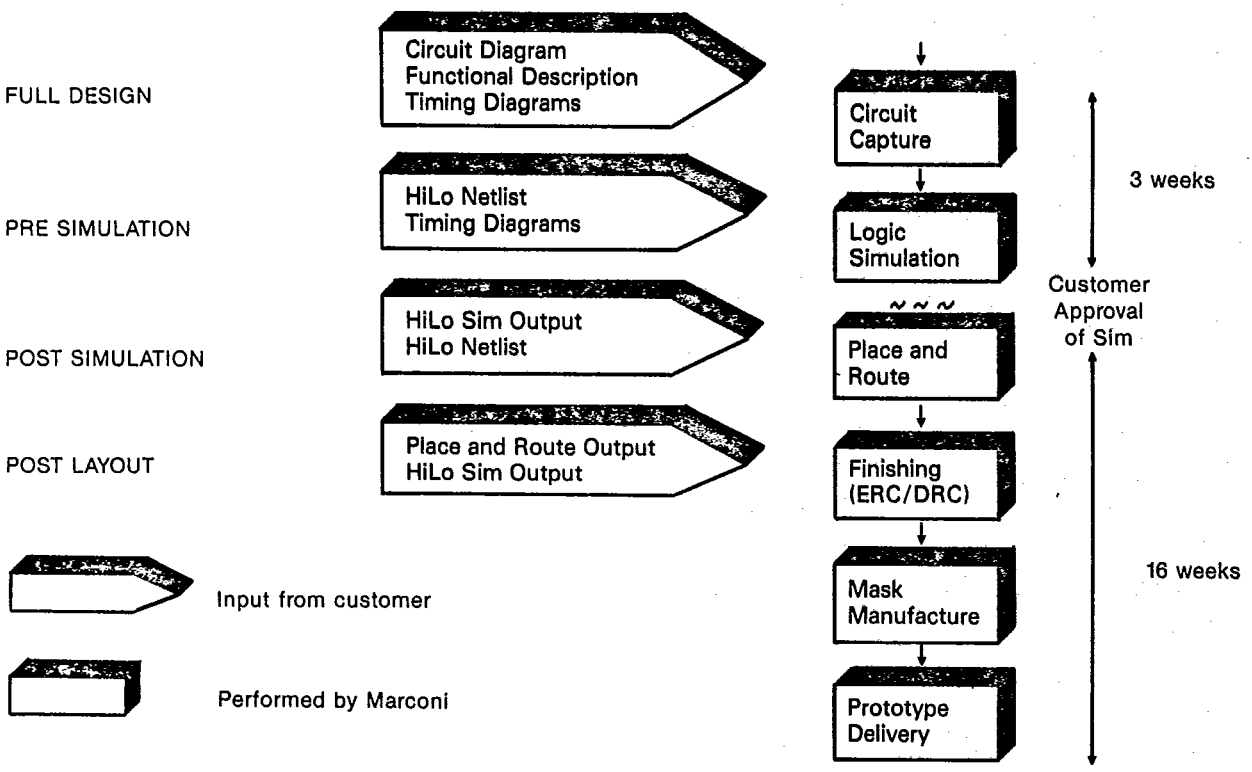
DEVELOPMENT INTERFACES



For further more detailed information on Marconi's design interfaces and CAD software please refer to our semi-custom CAD data sheet.

PACKAGE OPTIONS AVAILABLE AS STANDARD

CERAMIC DIL	14	16	18	20	24	28	40	48	
CERDIP	14	16	18	20	24	28	40	48	
PLASTIC DIL	14	16	18	20	24	28	40		
PLASTIC SO	16L								
PIN GRID ARRAY	68	84	120	144					
CERAMIC LCC	20	28	[40]	44	[48]	68	84		[ ] have 0.040" centers, others have 0.050"
PLASTIC LCC	28	44	68	84					
EPIC (PCB) LCC	40								
CERQUAD	44	68	84						

Marconi has a wide range of packages offered as standard as shown above. If, however, you have a packaging requirement not on this table a Marconi applications engineer will be happy to discuss your needs.

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CELL LIBRARY QUICK GUIDE

Name	Description	Cell width
COMBINATIONAL GATES		
INVB	Fast inverter	4
INV	Inverter	3
BUFF	Non-inverting buffer	4
NAND2	2 input NAND	4
NAND3	3 input NAND	5
NAND4	4 input NAND	6
AND2	2 input AND	5
AND3	3 input AND	6
AND4	4 input AND	7
NOR2	2 input NOR	4
NOR3	3 input NOR	5
NOR4	4 input NOR	6
OR2	2 input OR	5
OR3	3 input OR	6
OR4	4 input OR	7
ANDNOR	2+2 input AND/NOR	6
ANDOR	2+2 input AND/OR	8
ORNAND	2+2 input OR/NAND	6
ORAND	2+2 input OR/AND	8
O2NA1	OR2/AND1 invert gate	6
O2A1	OR2/AND1 gate	7
O2NA2	OR2/AND2 invert gate	6
O2A2	OR2/AND2 gate	8
O3NA1	OR3/AND1 invert gate	7
O3A1	OR3/AND1 gate	8
A2NO1	AND2/OR1 invert gate	6
A2O1	AND2/OR1 gate	8
A2NO2	AND2/OR2 invert gate	6
A2O2	AND2/OR2 gate	8
A3NO1	AND3/OR1 invert gate	7
A3O1	AND3/OR1 gate	8
EXNOR	Exclusive NOR	8
EXOR	Exclusive OR	7
SEL2	Select 1 of 2	8
SEL2INV	Select 1 of 2 (Inv)	7
ARITHMETIC		
FAD	Full adder	17
SIMPLE LATCHES		
NASR	NAND set-reset latch	6
NOSR	NOR set-reset latch	6
NO2SR	NOR set-reset latch (2 INPUT)	7
NA2SR	NAND set-reset latch (2 INPUT)	7
CLOCK LATCHES		
DL	D-latch	12
DLH	Transparent high level latch	12

CELL LIBRARY QUICK GUIDE

Name	Description	Cell width
EDGE TRIGGERED LATCHES		
RETS	Edge triggered latch with reset	19
SRETS	Edge triggered latch with set and reset	21
MASTER-SLAVE FLIP-FLOPS		
DT	D-Type	18
D2T	Dual input D-type	27
SDT	Set D-type	21
RDT	Reset D-type	19
SRDT	Set/reset D-type	21
TOGGLE FLIP-FLOPS		
RTT	Reset T-type	19
SRTT	Set/reset T-type	21
RTTTOG	Reset T-type with low level toggl enable	24
RTTTOGH	Reset T-type with high level toggle enable	24
INVERTING TRI-STATE BUFFERS		
TRINV	Tri-state inverting buffer	5
TRINVL	Tri-state inverter with low level enable	5

ANALOG CELLS

	Resistors (2K ohms to 350K ohms)
	Capacitors
AVABS	Voltage reference
AVRNP3	Bias generator
AOP1	Operational amplifier
ABUF1	Output buffer
ACMP1	Analog comparator
ANSW*	Analog switches
ARCOSC	RC oscillator/monostable

INPUT OUTPUT AND PERIPHERAL CELLS

INPUT/OUTPUT		
CIO1	CMOS input/output	
TIO1	TTL input/output	
INPUTS		
TTLIN	TTL input buffer	5
SCHMITT	SCHMITT input buffer	11
DIP	Direct input (protection circuit only)	
OUTPUTS		
TRIOP	Tri-state I/O buffer (This is a core cell used with peripheral cell ZOP)	12
POWER SUPPLY PADS		
VDD	Vdd pad	
VSS	Vss pad	