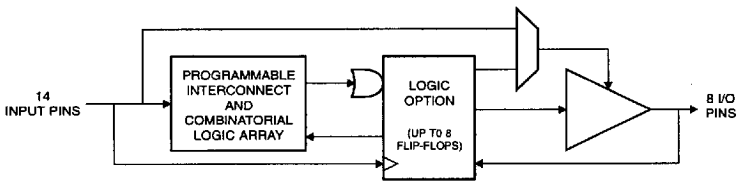
Features

- User-Controlled Power Down Pin
- Low Voltage Equivalent of ATF20V8B
- Operates down to 2.7 V
- Edge-Sensing Zero Standby Power (10 µA Typical)
- Ideal For Battery Powered Systems
  - Emulates Many 24-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 5 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Advance Information

Block Diagram



Description

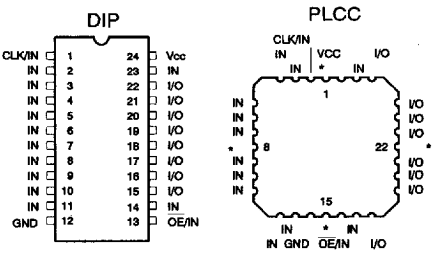
The ATF20LV8CZ is a low voltage compatible CMOS high performance Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns with virtually zero standby power dissipation are offered. All pins offer low ± 10 µA leakage.

The ATF20LV8CZ provides a low voltage and user-controlled zero power CMOS PLD solution with operating voltages down to 2.7 V. The ATF20LV8CZ has an edge-sensing power

(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
*	No Internal Connection
VCC	+5 V Supply



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Description (Continued)

down feature, offering "zero" (10 µA typical) standby power. This feature allows the user to manage total system power to meet specific application requirements, enhance reliability, all without sacrificing speed. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-up resistors. The ATF20LV8CZ provides edge-sensing "zero" standby power (10 µA typical).

The ATF20LV8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allowing highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3 V ± 5%	3 V ± 10%

Functional Description

The ATF20LV8CZ macrocell can be configured in one of three different modes. Each mode makes the ATF20LV8CZ look like a different device. The ATF20LV8CZ can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of registered versus combinatorial outputs and dedicated outputs versus output with output enable control.

The ATF20LV8CZ is capable of operating at supply voltages down to 2.7 V. It powers down automatically through IDT cicuiting down to "zero" stand-by power (10µA) when all inputs are idle.

The universal architecture of the ATF20LV8CZ can be programmed to emulate many 24-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF20LV8CZ can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents the ATF20LV8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection[1]

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R [2]	GAL20V8_C7 [2]	GAL20V8_C8 [2]	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8A
PLDesigner	P20V8R	P20V8C	P20V8C	P20V8A
Tango-PLD	G20V8R	G20V8C	G20V8AS	G20V8

Note: 1. Not applicable when using pin-controlled PD (Power-down) feature.
2. Only applicable for version 3.4 or lower.