AM26LS32CC, AM26LS33CC
Quad Line Receivers

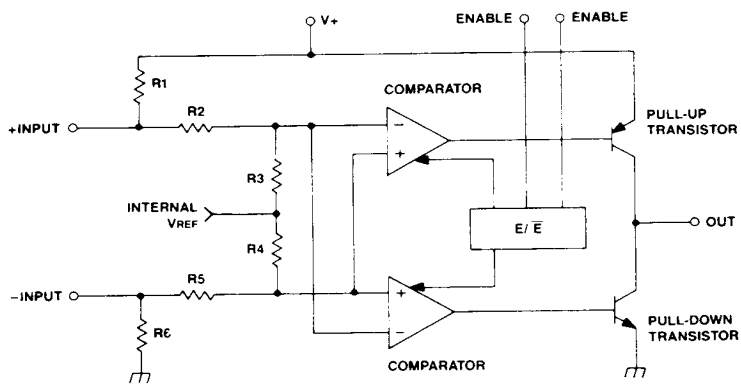
Description

The AM26LS32CC and AM26LS33CC Quad Line Receivers are general-purpose quad line receivers for balanced and unbalanced data transmission. A TTL-compatible ENABLE, $\overline{\text{ENABLE}}$ is common to all four receivers in the device package. The ENABLE, $\overline{\text{ENABLE}}$ allows the output to assume a high-impedance state for output busing.

Features

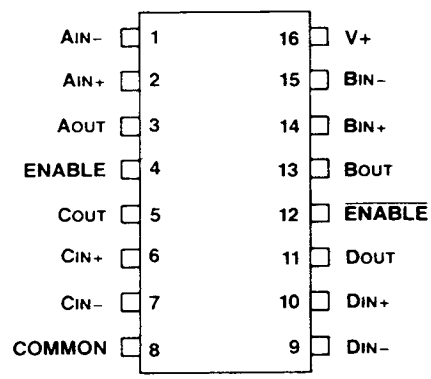
- Requires only a single 5 V (±10%) power supply
- Input sensitivity:
  AM26LS32CC ±200 mV
  AM26LS33CC ±500 mV
- Minimum input hysteresis:
  AM26LS32CC ±15 mV
  AM26LS33CC ± 30 mV
- Internal fail safe forces the output high for an open input condition
- Direct replacement for industry-standard differential line receivers
- Meets EIA RS-422A/423A specifications
- Four independent receivers with common strobe TTL-compatible input
- Electrostatic discharge protection on receiver inputs
- Typical propagation delay of 17 ns
- Available in a 16-pin plastic DIP

Functional Diagram



Notes: R1 and R6 are fail-safe resistors.
R2, R3, R4, R5 form an Input Divider.
With the internal reference (V_{REF}), these components set the input characteristics.
One of four identical circuits shown.

Pin Diagram



Maximum Ratings

Rating	Value	Unit
Supply Voltage (V +)	7.0	V
Control Input Voltage (ENABLE, $\overline{\text{ENABLE}}$)	7.0	V
Input Common Mode Range	±25	V
Input Differential Voltage	±25	V
Operating Temperature	0 to 85	°C
Storage Temperature Range	−40 to +125	°C
Power Dissipation (Package Limitation)	400	mW
Pin Temperature (Soldering, 15 sec)	300	°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1	AIN −	Negative Input, Receiver A
2	AIN +	Positive Input, Receiver A
3	AOUT	Output, Receiver A
4	ENABLE	Enable Input
5	COUT	Output, Receiver C
6	CIN +	Positive Input, Receiver C
7	CIN −	Negative Input, Receiver C
8	COMMON	Circuit Common, not necessarily physical or system ground
9	DIN −	Negative Input, Receiver D
10	DIN +	Positive Input, Receiver D
11	DOUT	Output, Receiver D
12	$\overline{\text{ENABLE}}$	$\overline{\text{Enable}}$ Input
13	BOUT	Output, Receiver B
14	BIN +	Positive Input, Receiver B
15	BIN −	Negative Input, Receiver B
16	V +	Supply Voltage, External

Electrical Characteristics

$0 \leq T_A \leq 85°C$, $4.5\ V \leq V+ \leq 5.5\ V$, unless otherwise specified

Characteristic	Conditions	Min	Max	Unit
Differential Input Threshold Voltage (Figure 2)	$I_O = -0.4$ mA, $V_{OH} \geq 2.7$ V AM26LS32CC, $-7.0\ V < V_{CM} < 7.0\ V$	—	0.2	V
	AM26LS33CC, $-15.0\ V < V_{CM} < 15.0\ V$	—	0.5	
	$I_O = 4.0$ mA, $V_{OL} \leq 0.5$ V AM26LS32CC, $-7.0\ V < V_{CM} < 7.0\ V$	—	−0.2	
	AM26LS33CC, $-15.0\ V < V_{CM} < 15.0\ V$	—	−0.5	
Dynamic Input Resistance (Figure 3)	$-15.0\ V < V_{CM} < 15.0\ V$ One input ac ground	6.0	—	kΩ
Input Current (Figure 4)	$V_{IN} = 15.0$ V	—	2.3	mA
	$V_{IN} = -15.0$ V	—	−2.8	
Input Hysteresis Voltage (Figure 2)	$V+ = 5.0\ V$, $T_A = 25°C$ AM26LS32CC, $V_{CM} = \pm 7.0$ V	±15	—	mV
	AM26LS33CC, $V_{CM} = \pm 15.0$ V	±30	—	
High-Level Output Voltage (Figure 5)	$V+ = 4.5\ V$, $V_{ID} = 1.0\ V$, $V_{\overline{EN}} = 0.8\ V$, $I_{OH} = -440\ \mu A$	3.6	—	V
Low-Level Output Voltage (Figure 5)	$V+ = 4.5\ V$, $V_{ID} = 0.8\ V$, $V_{\overline{EN}} = 0.8\ V$ $I_{OL} = 5.0$ mA	—	0.4	
	$I_{OL} = 10.0$ mA	—	0.45	
Output Short-Circuit Current (Figure 6)	$V+ = 5.5\ V$ $EN = \overline{EN} = 0.8\ V$	−15	−80	mA
Off-State Output Current (High Z) (Figure 7)	$V+ = 5.5\ V$, $V_O = 2.4\ V$	—	20	μA
	$V+ = 5.5\ V$, $V_O = 0.4\ V$	—	−20	
Power Supply Current (Figure 8)	$V+ = 5.5\ V$ All Inputs Grounded, Output Disabled	—	70	mA
Input Low-State Voltage*†		—	0.8	V
Input High-State Voltage*†		1.8	—	
Low-State Current*	V_{IN} 0 V, $V+ = 5.5\ V$	—	−0.36	mA
High-State Current*	$V_{IN} = 2.7\ V$, $V+ = 5.5\ V$	—	20	μA
High-Voltage Current*	$V_{IN} = 5.5\ V$, $V+ = 5.5\ V$	—	100	μA
Input Clamp Voltage*	$V+ = 4.5\ V$, $I_{IN} = -18$ mA	—	1.5	V

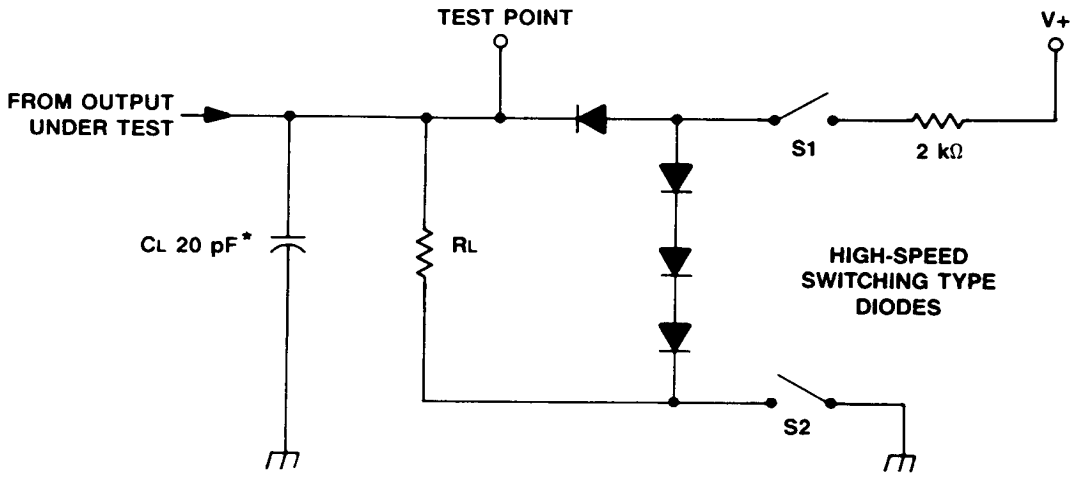
* These specifications refer only to the ENABLE and $\overline{\text{ENABLE}}$ inputs (pins 4 and 12 respectively).
† Indirectly guaranteed; not set up as an individual test.

Timing Characteristics

T_A = 25°C, V+ = 5.0 V, C_L = 20 pF

Characteristic	Conditions		Min	Max	Unit
Propagation Delay Time*	R_L = 5.0 kΩ (Figure 9)	t_{PLH}	—	25	ns
		t_{PHL}	—	25	
	R_L = 1.67 kΩ (Figure 10)	t_{PLZ}	—	30	
		t_{PHZ}	—	27	
	R_L = 5.0 kΩ (Figure 10)	t_{PZL}	—	22	
		t_{PZH}	—	24	

* See Figure 1 for Load Test Circuit, and Figures 11 and 12 for the Timing Diagrams.



* INCLUDING PROBE & JIG CAPACITANCE

Figure 1. Load Test Circuits for 3-State Outputs

Recommended Operating Conditions

Rating	Value	Unit
Supply Voltage (V+)	4.5 to 5.5	V
Operating Ambient Temperature Range	0 to 85	°C
Input Common Mode Range		
AM26LS32CC	±7.0	V
AM26LS33CC	±15.0	V

Test Circuits

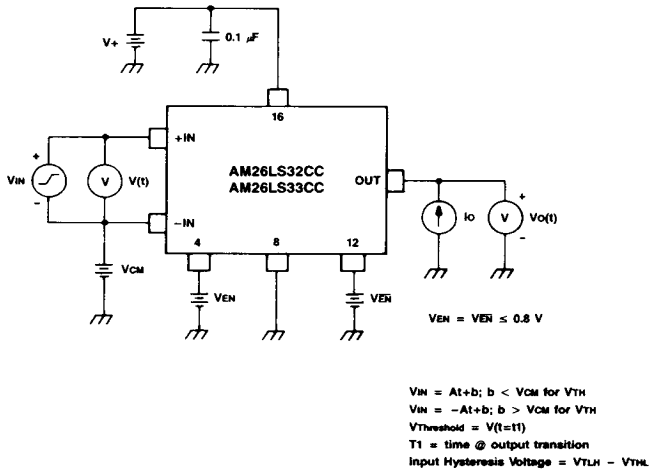


Figure 2. Differential Input Threshold Voltage

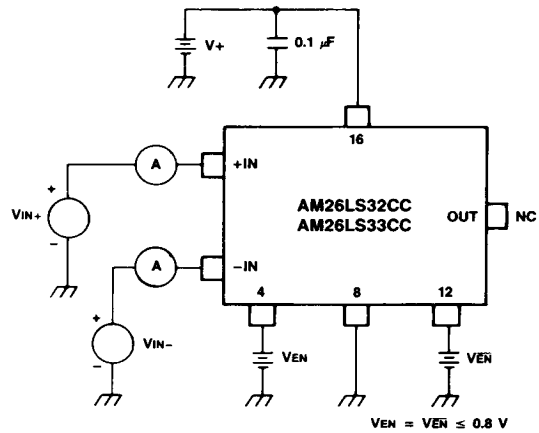


Figure 4. Input Current

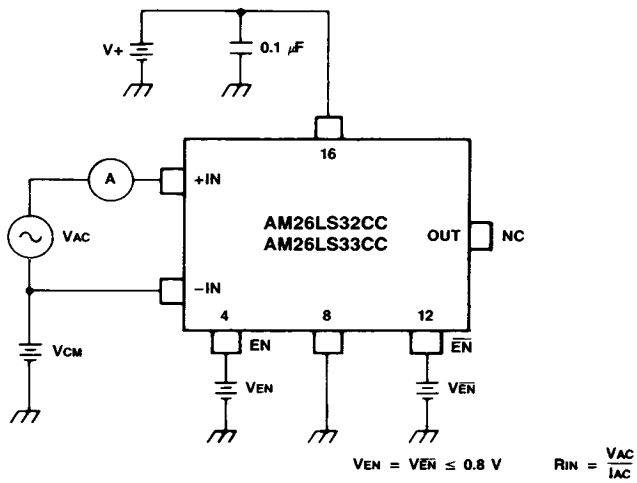


Figure 3. Dynamic Input Resistance

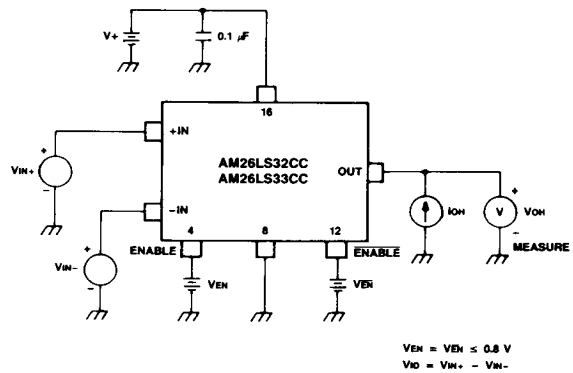


Figure 5. High-Level Output Voltage & Low-Level Output Voltage

Test Circuits (Continued)

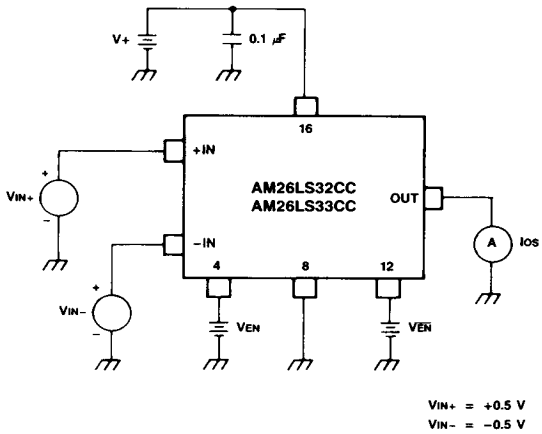


Figure 6. Output Current, Short Circuit

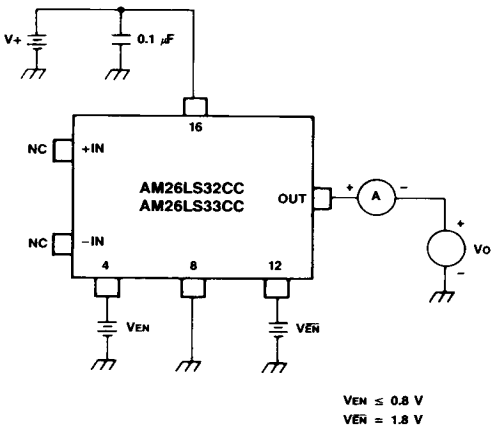


Figure 7. Off-State Output Current (High Z)

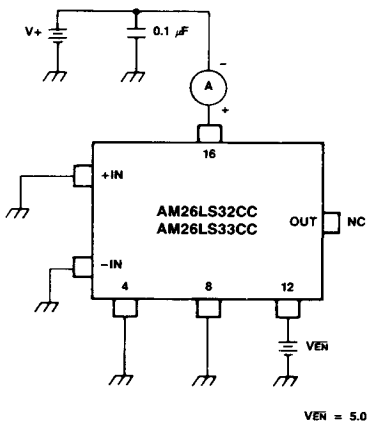


Figure 8. Power Supply Current

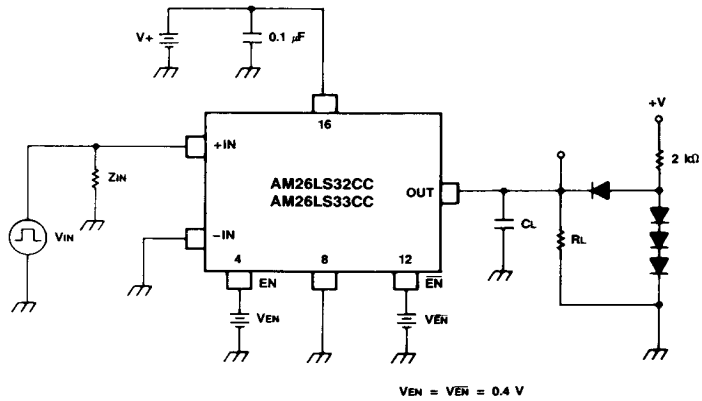


Figure 9. Propagation Delay Times (t_{PLH}, t_{PHL})

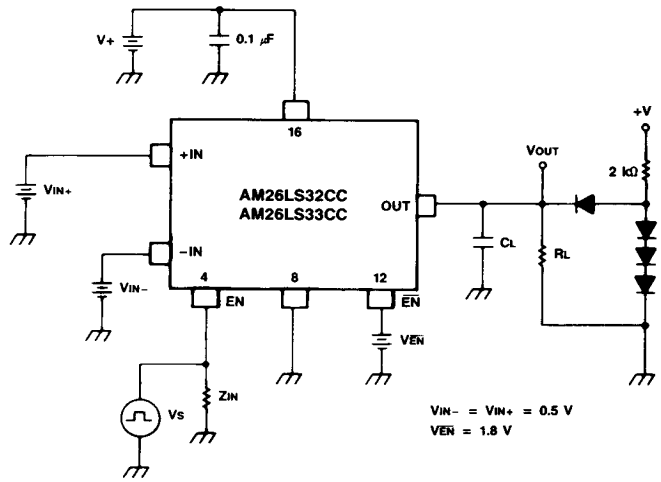


Figure 10. Propagation Delay Times (t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH})

Timing Diagrams

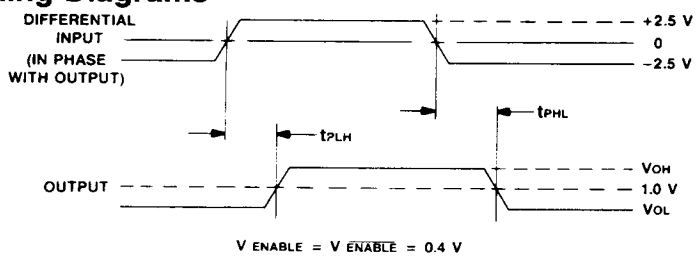
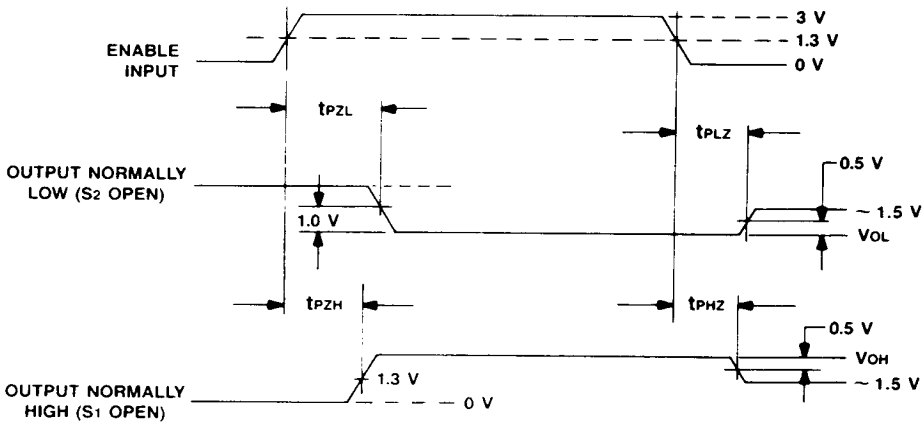


Figure 11. Signal Propagation Delay Time

Timing Diagrams (Continued)



Notes: S_1 and S_2 of Load Circuit are Closed Except as Noted Above, and V $\overline{\text{ENABLE}}$ = 1.8 V
Pulse Generator: Rate ≤ 1.0 MHz, Z_O = 50 Ω, tr ≤ 15 ns, tf ≤ 6 ns

Figure 12. ENABLE, $\overline{\text{ENABLE}}$ Delay Times

Applications

The following Truth Table shows the ENABLE and $\overline{\text{ENABLE}}$ conditions which must be met to provide specific receiver output states.

ENABLE	$\overline{\text{ENABLE}}$	Output
0	0	Enabled
1	0	Enabled
0	1	Disabled
1	1	Enabled

0 = Low State (V_{IN} ≤ 0.8 V)
1 = High State (V_{IN} ≥ 2.0 V)

The following diagram illustrates basic information for application of the AM26LS32CC and AM26LS33CC Quad Line Receiver devices in a two-wire balanced RS-422A system. This particular diagram shows the AM26LS32CC, AM26LS33CC Quad Line Receivers interfacing with the AM26LS31CC Quad Line Driver.

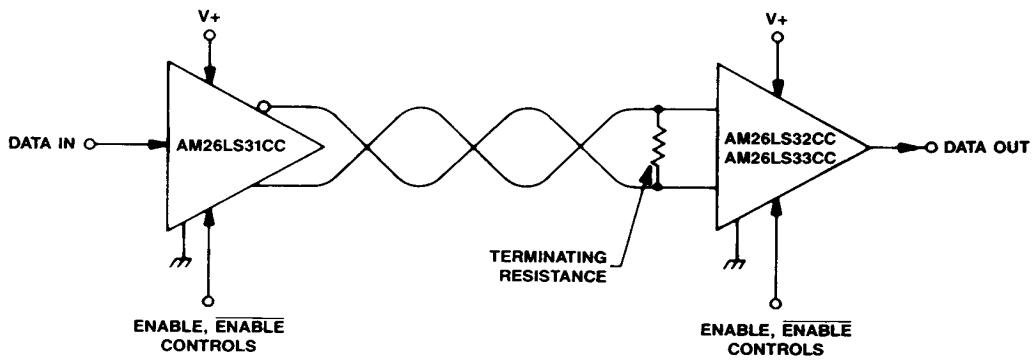
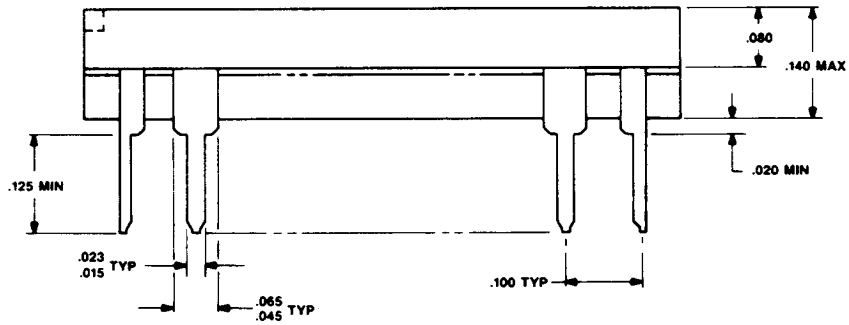
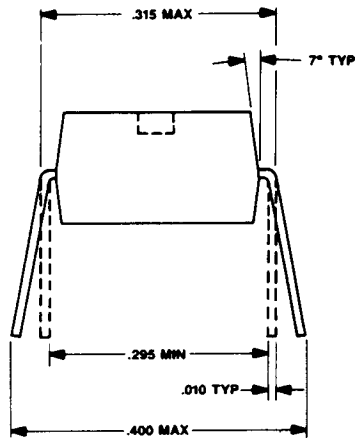
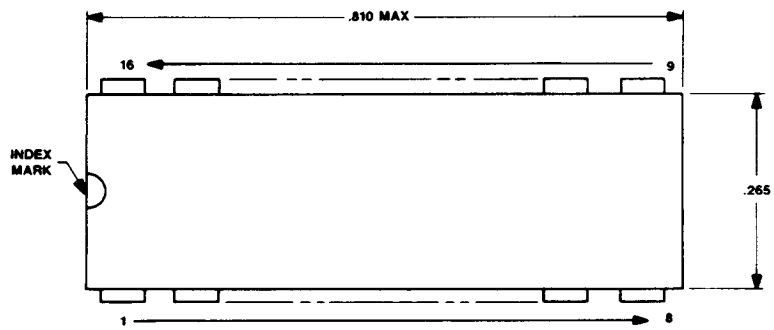


Figure 13. AM26LS32CC, AM26LS33CC Quad Line Receiver Application Diagram

Outline Drawing
(Dimensions in Inches)







Note: Pin numbers are shown for reference only

Ordering Information

DEVICE	COMCODE
AM26LS32CC	104438056
AM26LS33CC	104438064

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