Melody® 32 Audio Processor

ADSST-Melody-32

FEATURES

Single-Chip DSP-Based Implementation of Digital Audio Algorithms
Up to 160 MIPS and Extensive On-Chip Memory
Caters to a Wide Variety of Applications
32-Bit Fixed Point Implementation from End to End
Pseudo Floating Point Implementation and Selective 48-Bit Fixed Point Implementation Where Necessary to Improve Sonic Quality
Some of the Applicable Software Solutions Available Are:
- **Dolby® Digital**
- **Dolby Pro Logic® II**
- **DTS® ES™**
- **DTS Neo:6™**
- **MPEG AAC Multichannel**
- **THX® Surround EX™**
- **SRS Circle Surround II™**
- **96 kHz Processing**
- **ADI Surround Fields**
- **Speaker Enhancement**
- **Bass/Delay Management**
- **Automatic Stream Detection and Code Loading**
- **Customer Specific DSP Modes**
- **Host Communication Using SPI®**
- **Flexible Serial Ports**
- **I²S Support**
- **SRAM Support**
- **Support for IEC60958**

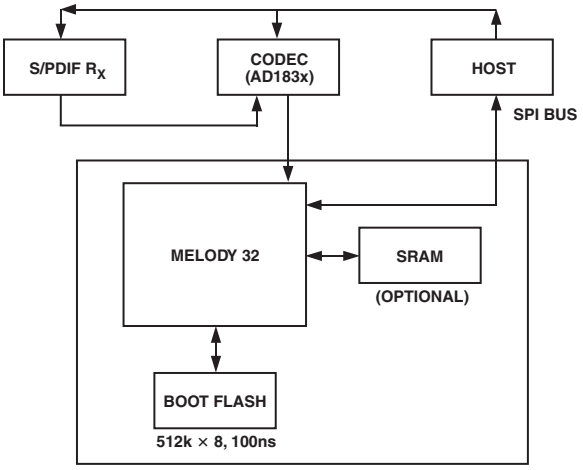
GENERAL DESCRIPTION

The Melody 32 family of digital audio decoders provides flexible solutions to the AV receiver and DVD market. The solutions offered can be tailored to the exact needs of the application. Combined with a range of high performance codecs from Analog Devices, the Melody family becomes a comprehensive answer to the needs of the high quality digital audio market.

The single-chip Melody 32 combines a high performance DSP architecture (three computational units, two data address generators, and a program sequencer) with two SPI compatible ports, three serial ports, one UART port, a DMA controller, three programmable timers, general-purpose programmable flag pins, interrupt capabilities, and on-chip program and data memory spaces.

The Melody 32 integrates 64 K words of on-chip memory configured as 32 K words (24-bit) of program RAM and 32 K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. Fabricated in a high speed, low power CMOS process, the Melody 32 operates with a 6.25 ns instruction cycle time (160 MIPS). All instructions, except two multiword instructions, can execute in a single cycle.

REFERENCE BLOCK DIAGRAM



REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

ADSST-Melody-32–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	2.37	2.63	V
V_{DDEXT}	External (I/O) Supply Voltage	2.97	3.63	V
V_{IH1}	High Level Input Voltage[1] @ V_{DDINT} = max V_{DDEXT} = max	2.0	V_{DDEXT}	V
V_{IH2}	High Level Input Voltage[2] @ V_{DDINT} = max V_{DDEXT} = max	2.2	V_{DDEXT}	V
V_{IL}	Low Level Input Voltage[1] @ V_{DDINT} = min V_{DDEXT} = min	–0.3	+0.8	V
T_{AMB}	Ambient Operating Temperature	0	70	°C

ELECTRICAL CHARACTERISTICS

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
V_{OH}	High Level Output Voltage[3]	2.4			V	@ V_{DDEXT} = min, I_{OH} = –0.5 mA
V_{OL}	Low Level Output Voltage[3]			0.4	V	@ V_{DDEXT} = min, I_{OL} = 2.0 mA
I_{IH}	High Level Input Current[4, 5]			10	µA	@ V_{DDEXT} = max, V_{IN} = V_{DD} max
I_{IL}	Low Level Input Current[4, 6]			10	µA	@ V_{DDEXT} = max, V_{IN} = 0 V
I_{IHP}[7]	High Level Input Current[6]	30		100	µA	@ V_{DDEXT} = max, V_{IN} = V_{DD} max
I_{LP}	Low Level Input Current[5]	20		70	µA	@ V_{DDEXT} = max, V_{IN} = 0 V
I_{OZH}[7]	Three-State Leakage Current[3]			10	µA	@ V_{DDEXT} = max, V_{IN} = V_{DD} max
I_{OZL}	Three-State Leakage Current[3]			10	µA	@ V_{DDEXT} = max, V_{IN} = 0 V
$I_{DD-IDLE1}$[8]	Supply Current (Core) Idle1[9]			2	mA	PLL Enabled, CCLK, HCLK Disabled
$I_{DD-IDLE2}$[8]	Supply Current (Core) Idle2[10]		1	2	mA	PLL Enabled, HCLK = 80 MHz, CLK Disabled
$I_{DDTYPICAL}$	Supply Current (Core) Typical[12]		184	210	mA	HCLK = 80 MHz, CCLK = 160 MHz
$I_{DD-PEAK}$	Supply Current (Core Peak)[10]		215	240	mA	HCLK = 80 MHz, CCLK = 160 MHz
$I_{DD-PERIPHERAL1}$	Supply Current (Peripheral)[10]		5	8	mA	PLL Enabled, CCLK, HCLK Disabled
$I_{DD-PERIPHERAL2}$	Supply Current (Peripheral)[10]		60	70	mA	HCLK = 80 MHz
$I_{DD-POWERDOWN}$	Supply Current[10]		100		µA	PLL, CORE, HCLK, CLKIN Disabled
C_{IN}	Input Capacitance[11, 12]			8	pF	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V

NOTES

[1] Applies to input and bidirectional pins: DATA15–0, HAD15–0, HAD16, HALE, HACK, HACK_P, BYPASS, $\overline{\text{HRD}}$, $\overline{\text{HWR}}$, ACK, PF7–0, $\overline{\text{HCMS}}$, $\overline{\text{HCIOMS}}$, $\overline{\text{BR}}$, TFS0, TFS1, TFS2/MOSI0, RFS0, RFS1, RFS2/MOSI1, OPMODE, BMODE1–0, TMS, TDI, TCK, DT2/MISO0, DR0, DR1, DR2/MISO1, TCLK0, TCLK1, TCLK2/SCK0, RCLK0, RCLK1, RCLK2/SCK1, $\overline{\text{RESET}}$, $\overline{\text{TRST}}$.

[2] Applies to input pin: CLKIN.

[3] Applies to output and bidirectional pins: DATA15–0, ADDR21–0, HAD15–0, $\overline{\text{MS3–0}}$, $\overline{\text{IOMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, CLKOUT, HACK, PF7–0, TMR2–0, $\overline{\text{BGH}}$, $\overline{\text{BG}}$, DT0, DT1, DT2/MISO0, TCLK0, TCLK1, TCLK2/SCK0, RCLK0, RCLK1, RCLK2/SCK1, TFS0, TFS1, TFS2/MOSI0, RFS0, RFS1, RFS2/MOSI1, $\overline{\text{BMS}}$, TDO, TXD, $\overline{\text{EMU}}$ DR2/MISO1.

[4] Applies to input pins: ACK, $\overline{\text{BR}}$, $\overline{\text{HCMS}}$, $\overline{\text{HCIOMS}}$, HAD16, HALE, $\overline{\text{HRD}}$, $\overline{\text{HWR}}$, CLKIN, DR0, DR1, BYPASS, RXD, HACK_P.

[5] Applies to input pins with internal pull-ups: BMODE0, BMODE1, OPMODE, BYPASS, TCK, TMS, TDI, RESET.

[6] Applies to input pin with internal pull-down: $\overline{\text{TRST}}$.

[7] Applies to three-state pins: DATA15–0, ADDR21–0, $\overline{\text{MS3–0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PF7–0, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, TFSx, RFSx, TDO, $\overline{\text{EMU}}$, TCLKx, RCLKx, DTx, HADI5–0, TMR2–0.

[8] Idle denotes Melody 32 state during execution of IDLE instruction. For more information, see Power Dissipation section.

[9] Test Condition: @ V_{DDINT} = 2.5 V, T_{AMB} = 25°C.

[10] Test Condition: @ V_{DDINT} = 2.65 V, T_{AMB} = 25°C.

[11] Applies to all signal pins.

[12] Guaranteed, but not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DDINT} Internal (Core) Supply Voltage . . . . . –0.3 V to +3.0 V
V_{DDEXT} External (I/O) Supply Voltage . . . . . –0.3 V to +4.6 V
V_{IL}–V_{IH} Input Voltage . . . . . –0.5 V to V_{DDEXT} + 0.5 V
V_{OL}–V_{OH} Output Voltage Swing . . . –0.5 V to V_{DDEXT} + 0.5 V
C_L Load Capacitance . . . . . 200 pF
t_{CCLK} Core Clock Period . . . . . 6.25 ns
f_{CCLK} Core Clock Frequency . . . . . 160 MHz
t_{HCLK} Peripheral Clock Period . . . . . 12.5 ns
f_{HCLK} Peripheral Clock Frequency . . . . . 80 MHz
T_{STORE} Storage Temperature Range . . . . . –65°C to +150°C
T_{LEAD} Lead Temperature (5 sec) . . . . . 185°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect devices reliability.

ORDERING INFORMATION

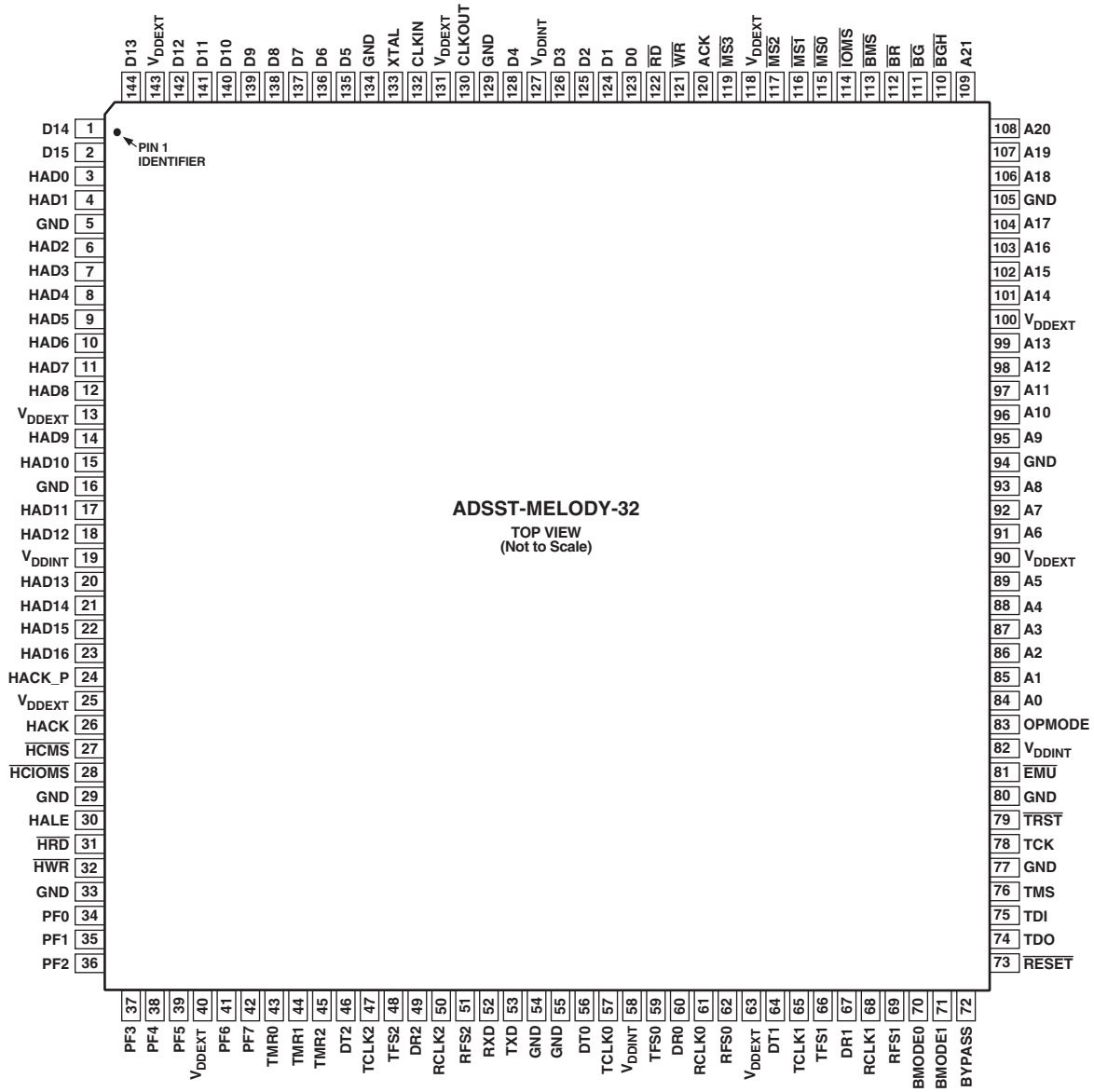
The Analog Devices Melody 32 AVR Reference Design must be ordered under the part number ADSST-Melody-SDK for the standalone reference design. This includes the evaluation board with an evaluation copy of the software and schematics.

Designers of products using this reference design also will be required to sign a license agreement with the respective license holder—i.e., Digital Theater Systems (DTS), Dolby Laboratories, THX Ltd., Microsoft, or SRS Labs—to use the appropriate code, and produce proof to Analog Devices of having successfully completed the appropriate licensing procedures before final product can be shipped to them. The final product will be shipped from Analog Devices and will include the decoder chipset and software; customers will be required to sign license agreements with Analog Devices and separately pay system royalties to the respective license holder.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSST-Melody-32 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN DESCRIPTIONS

The following list is the Melody 32 pin numbers descriptions. The Pin Functions table starts on the next page. All Melody 32 inputs are asynchronous and can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Inputs identified as synchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Unused inputs should be tied or pulled to V_{DDEXT} or GND, except for ADDR21–0, DATA15–0, PF7–0, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{TRST}}$, BMODE0, BMODE1, OPMODE, BYPASS, TCK, TMS, TDI, and $\overline{\text{RESET}}$), which can be left floating. These pins have a logic-level hold circuit that prevents input from floating internally.

Pin Number	Mnemonic	Pin Number	Mnemonic	Pin Number	Mnemonic	Pin Number	Mnemonic
1	D14	37	PF3	73	$\overline{\text{RESET}}$	109	A21
2	D15	38	PF4	74	TDO	110	$\overline{\text{BGH}}$
3	HAD0	39	PF5	75	TDI	111	$\overline{\text{BG}}$
4	HAD1	40	V_{DDEXT}	76	TMS	112	$\overline{\text{BR}}$
5	GND	41	PF6	77	GND	113	$\overline{\text{BMS}}$
6	HAD2	42	PF7	78	TCK	114	$\overline{\text{IOMS}}$
7	HAD3	43	TMR0	79	$\overline{\text{TRST}}$	115	$\overline{\text{MS0}}$
8	HAD4	44	TMR1	80	GND	116	$\overline{\text{MS1}}$
9	HAD5	45	TMR2	81	$\overline{\text{EMU}}$	117	$\overline{\text{MS2}}$
10	HAD6	46	DT2	82	V_{DDINT}	118	V_{DDEXT}
11	HAD7	47	TCLK2	83	OPMODE	119	$\overline{\text{MS3}}$
12	HAD8	48	TFS2	84	A0	120	ACK
13	V_{DDEXT}	49	DR2	85	A1	121	$\overline{\text{WR}}$
14	HAD9	50	RCLK2	86	A2	122	$\overline{\text{RD}}$
15	HAD10	51	RFS2	87	A3	123	D0
16	GND	52	RXD	88	A4	124	D1
17	HAD11	53	TXD	89	A5	125	D2
18	HAD12	54	GND	90	V_{DDEXT}	126	D3
19	V_{DDINT}	55	GND	91	A6	127	V_{DDINT}
20	HAD13	56	DT0	92	A7	128	D4
21	HAD14	57	TCLK0	93	A8	129	GND
22	HAD15	58	V_{DDINT}	94	GND	130	CLKOUT
23	HAD16	59	TFS0	95	A9	131	V_{DDEXT}
24	HACK_P	60	DR0	96	A10	132	CLKIN
25	V_{DDEXT}	61	RCLK0	97	A11	133	XTAL
26	HACK	62	RFS0	98	A12	134	GND
27	$\overline{\text{HCMS}}$	63	V_{DDEXT}	99	A13	135	D5
28	$\overline{\text{HCIOMS}}$	64	DT1	100	V_{DDEXT}	136	D6
29	GND	65	TCLK1	101	A14	137	D7
30	HALE	66	TFS1	102	A15	138	D8
31	$\overline{\text{HRD}}$	67	DR1	103	A16	139	D9
32	$\overline{\text{HWR}}$	68	RCLK1	104	A17	140	D10
33	GND	69	RFS1	105	GND	141	D11
34	PF0	70	BMODE0	106	A18	142	D12
35	PF1	71	BMODE1	107	A19	143	V_{DDEXT}
36	PF2	72	BYPASS	108	A20	144	D13

PIN FUNCTIONS

Pin	Type	Function
A21–0	O/T	External Port Address Bus
D7–0	I/O/T	External Port Databus, Least Significant 8 Bits
D15/PF15/ SPI1SEL7	I/O/T	Data 15 (if 16-Bit External Bus)/Programmable Flags 15 (if 8-Bit External Bus)/ SPI1 Slave Select Output 7 (if 8-Bit External Bus, when SPI1 Enabled)
D14/PF14/ SPI0SEL7	I/O/T	Data 14 (if 16-Bit External Bus)/Programmable Flags 14 (if 8-Bit External Bus)/ SPI0 Slave Select Output 7 (if 8-Bit External Bus, when SPI0 Enabled)
D13/PF12/ SPI1SEL6	I/O/T	Data 13 (if 16-Bit External Bus)/Programmable Flags 13 (if 8-Bit External Bus)/ SPI1 Slave Select Output 6 (if 8-Bit External Bus, when SPI1 Enabled)
D12/PF12/ SPI0SEL6	I/O/T	Data 12 (if 16-Bit External Bus)/Programmable Flags 12 (if 8-Bit External Bus)/ SPI0 Slave Select Output 6 (if 8-Bit External Bus, when SPI0 Enabled)
D11/PF11/ SPI1SEL5	I/O/T	Data 11 (if 16-Bit External Bus)/Programmable Flags 11 (if 8-Bit External Bus)/ SPI1 Slave Select Output 5 (if 8-Bit External Bus, when SPI1 Enabled)
D10/PF10/ SPI0SEL5	I/O/T	Data 10 (if 16-Bit External Bus)/Programmable Flags 10 (if 8-Bit External Bus)/SPI0 Slave Select Output 5 (if 8-Bit External Bus, when SPI0 Enabled)
D9/PF9/ SPI1SEL4	I/O/T	Data 9 (if 16-Bit External Bus)/Programmable Flags 9 (if 8-Bit External Bus)/SPI1 Slave Select Output 4 (if 8-Bit External Bus, when SPI1 Enabled)
D8/PF8/ SPI0SEL4	I/O/T	Data 8 (if 16-Bit External Bus)/Programmable Flags 8 (if 8-Bit External Bus)/SPI0 Slave Select Output 4 (if 8-Bit External Bus, when SPI0 Enabled)
PF7/ SPI1SEL3/DF	I/O/T	Programmable Flags 7/SPI1 Slave Select Output 3 (when SPI0 Enabled)/Divisor Frequency (Divisor Select for PLL Input during Boot)
PF6/SPI0SEL3/ MSEL6	I/O/T	Programmable Flags 6/SPI0 Slave Select Output 3 (when SPI0 Enabled)/Multiplier Select 6 (during Boot)
PF5/SPI1SEL2/ MSEL5	I/O/T	Programmable Flags 5/SPI1 Slave Select Output 2 (when SPI0 Enabled)/Multiplier Select 5 (during Boot)
PF4/SPI0SEL2/ MSEL4	I/O/T	Programmable Flags 4/SPI0 Slave Select Output 2 (when SPI0 Enabled)/Multiplier Select 4 (during Boot)
PF3/SPI1SEL1/ MSEL3	I/O/T	Programmable Flags 3/SPI1 Slave Select Output 1(when SPI0 Enabled)/Multiplier Select 3 (during Boot)
PF2/SPI0SEL1/ MSEL2	I/O/T	Programmable Flags 2/SPI0 Slave Select Output 1 (when SPI0 Enabled)/Multiplier Select 2 (during Boot)
PF1/SPISS1/ MSEL1	I/O/T	Programmable Flags 1/SPI1 Slave Select Input (when SPI1 Enabled)/Multiplier Select 1 (during Boot)
PF0/SPISS0/ MSEL0	I/O/T	Programmable Flags 0/SPI0 Slave Select Input (when SPI0 Enabled)/Multiplier Select 0 (during Boot)
$\overline{RD}$	O/T	External Port Read Strobe
$\overline{WR}$	O/T	External Port Write Strobe
ACK	I	External Port Access Ready Acknowledge
$\overline{BMS}$	O/T	External Port Boot Space Select
$\overline{IOMS}$	O/T	External Port IO Space Select
$\overline{MS3–0}$	O/T	External Port Memory Space Selects
$\overline{BR}$	I	External Port Bus Request
$\overline{BG}$	O	External Port Bus Grant
$\overline{BGH}$	O	External Port Bus Grant Hang
HAD15–0	I/O/T	Host Port Multiplexed Address and Databus
HAD16	I	Host Port MSB of Address Bus
HACK_P	I	Host Port ACK Polarity
$\overline{HRD}$	I	Host Port Read Strobe
$\overline{HWR}$	I	Host Port Write Strobe
HACK	O	Host Port Access Ready Acknowledge
HALE	I	Host Port Address Latch Strobe or Address Cycle Control
$\overline{HCMS}$	I	Host Port Internal Memory-Internal I/O Memory-Boot Memory Select
$\overline{HCIOMS}$	I	Host Port Internal I/O Memory Select
CLKIN	I	Clock Input/Oscillator Input 0
XTAL	I	Oscillator Input 1
BMODE1–0	I	Boot Mode 1–0
OPMODE	I	Operating Mode
CLKOUT	O	Clock Output
BYPASS	I	Phase-Lock-Loop (PLL) Bypass Mode
RCLK1–0	I/O/T	SPORT1–0 Receive Clock
RCLK2/SCK1	I/O/T	SPORT2 Receive Clock/SPI1 Serial Clock
RFS1–0	I/O/T	SPORT1–0 Receive Frame Sync
RFS2/MOSI1	I/O/T	SPORT2 Receive Frame Sync/SPI1 Master-Output, Slave-Input Data
TCLK1–0	I/O/T	SPORT1–0 Transmit Clock
TCLK2/SCK0	I/O/T	SPORT2 Transmit Clock/SPI0 Serial Clock

Pin	Type	Function
TFS1–0	I/O/T	SPORT1–0 Transmit Frame Sync
TFS2/MOSI0	I/O/T	SPORT2 Transmit Frame Sync/SPI0 Master-Output, Slave-Input Data
DR1–0	I	SPORT1–0 Serial Data Receive
DR2/MISO1	I/O/T	SPORT2 Serial Data Receive/SPI1 Master-Input, Slave-Output Data
DT1–0	O/T	SPORT1–0 Serial Data Transmit
DT2/MISO0	I/O/T	SPORT2 Serial Data Transmit/SPI0 Master-Input, Slave-Output Data
TMR2–0	I/O/T	Timer Output or Capture
RXD	I	UART Serial Receive Data
TXD	O	UART Serial Transmit Data
$\overline{\text{RESET}}$	I	Processor Reset. Resets the Melody 32 to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up
TCK	I	Test Clock (JTAG). Provides a clock for JTAG boundary scan.
TMS	I	Test Mode Select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I	Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the Melody 32. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-down resistor.
$\overline{\text{EMU}}$	O	Emulation Status (JTAG). Must be connected to the Melody 32 emulator target board connector only. $\overline{\text{EMU}}$ has a 50 Ω internal pull-up resistor.
V_{DDINT}	P	Core Power Supply. Nominally 2.5 V dc and supplies the Melody 32's core processor (four pins).
V_{DDEXT}	P	I/O Power Supply. Nominally 3.3 V dc (nine pins).
GND	G	Power Supply Return (12 pins).
NC		Do Not Connect. Reserved pins that must be left open and unconnected.

HARDWARE ARCHITECTURE (AV RECEIVER REFERENCE DESIGN)

In a typical AVR receiver application, the Melody 32 processor can be interfaced to external peripherals with relative ease. The communication between the Melody 32 processor and a host microcontroller uses the SPI bus. The host microcontroller is the master and the Melody 32 processor is the slave.

Figure 1 shows a typical implementation of an AV receiver using the Melody 32 processor.

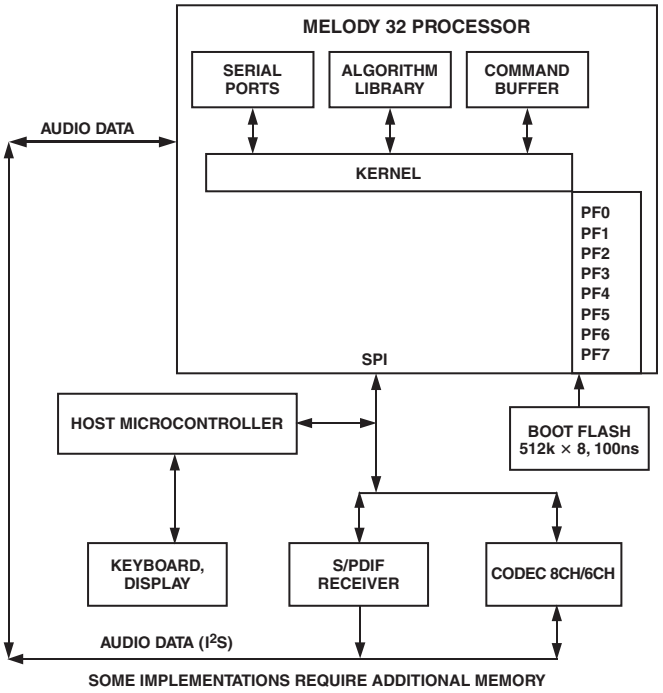


Figure 1. Hardware Architecture Reference Design

The peripherals can be controlled by the host controller using the SPI bus. The communication is based on commands and parameters. Status information regarding the Melody 32 decoding is periodically updated and made available to the host microcontroller.

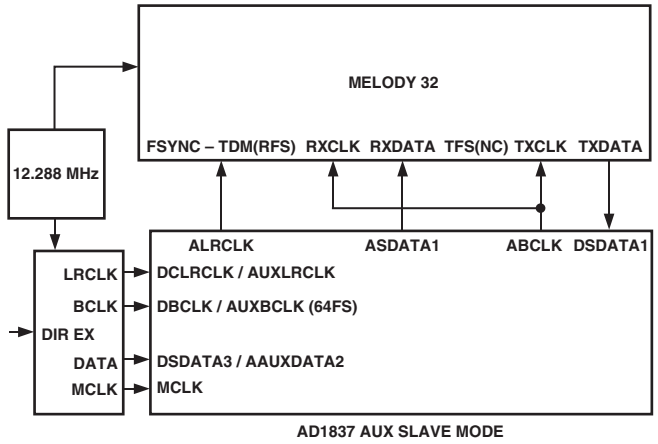


Figure 2. Melody 32 Codec Interface

SOFTWARE ARCHITECTURE

The Melody 32 software has the following parts:

- Executive kernel
- Algorithm as library module

The executive kernel performs the following functions:

- Power-up initialization
- Serial port management
- Automatic stream detect and code load
- Command processing
- Interrupt handling
- Data buffer management
- Calling library module
- Status reporting

All the algorithms are implemented in 32-bit precision. For example, with this implementation the performance of the Dolby Digital code exceeds "Class A" requirements mandated by Dolby Labs.

Figure 3 shows the software architecture.

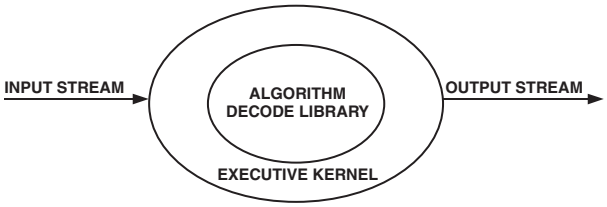


Figure 3. Software Architecture

Booting
The Melody 32 processor boots from an external EPROM or Flash memory. The code is automatically booted on power-up. Depending upon the stream detected, the appropriate code module is loaded from memory. The Flash required is 512 K × 8 with an access time of 100 ns.

Host Communication
The Melody 32 processor and host micro communication is defined using "Command Buffer." The command buffer is a memory area declared in the internal memory of Melody 32 processor. The host micro writes to the Melody 32 processor through the SPI port and issues an interrupt. The Melody 32 updates status information in the command buffer at periodic intervals, which can be read by the host micro. Thus, both the micro and the Melody 32 can exchange information. Commands and parameters are sent by micro through this SPI interface. Similarly, the Melody 32 can send back status information through the same port.

MIPS and Memory
The Melody 32 processor provides high performance with up to 160 MIPS of computing power. The internal memory of the Melody 32 is adequate in almost all applications. For DTS ES and AAC, 32 K × 16 SRAM is needed and for THX Surround EX, 64 K × 16 SRAM is needed. SRAM access time is 20 ns.

Host Microcontroller
The Melody 32 provides interrupt to the host microcontroller. When the level on this pin goes from high to low, it provides an interrupt to the microcontroller.

Power-on reset must be generated for the Melody 32, host microcontroller, and all other peripherals. In addition, the host microcontroller should be able to reset the Melody 32 processor.

MELODY 32 PERIPHERALS ARCHITECTURE

The functional block diagram shows Melody 32 on-chip peripherals, which include the external memory interface, host port, serial ports, SPI compatible ports, UART port, JTAG test and emulation port, timers, flags, and interrupt controller. These on-chip peripherals can connect to off-chip devices as shown in Figure 1.

The Melody 32 also has an external memory interface that is shared by the Melody 32's core, the DMA controller, and DMA capable peripherals, which include the UART, SPORT0, SPORT1, SPORT2, and host SPI port. The external port consists of a 16-bit databus, a 22-bit address bus, and control signals. The databus is configurable to provide an 8-bit or 16-bit interface to external memory. Support for word packing lets the Melody 32 access 16-bit or 24-bit words from external memory regardless of the external databus width. When configured for an 8-bit interface, the unused eight lines provide eight programmable, bidirectional general-purpose programmable flag lines, six of which can be mapped to software condition signals.

The memory DMA controller lets the Melody 32 move data and instructions from between memory spaces: internal-to-external, internal-to-internal, and external-to-external. On-chip peripherals can also use this controller for DMA transfers.

The Melody 32 can respond to up to 17 interrupts at any given time: three internal (stack, emulator kernel, and power-down), two external (emulator and reset), and 12 user-defined (peripherals) interrupts.

Programmers assign a peripheral to one of the 12 user-defined interrupts. These assignments determine the priority of each peripheral for interrupt service.

There are three serial ports on the Melody 32 that provide a complete synchronous, full-duplex serial interface. This interface includes optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each serial port can transmit or receive an internal or external programmable serial clock and frame syncs. Each serial port supports 128-channel time division multiplexing.

The Melody 32 provides up to 16 general-purpose I/O pins that are programmable as either inputs or outputs. Eight of these pins are dedicated general-purpose programmable flag pins. The other eight are multifunctional pins, acting as general-purpose I/O pins when Melody 32 connects to an 8-bit external databus and acting as the upper eight data pins when Melody 32 connects to a 16-bit external databus. These programmable flag pins can implement edge- or level-sensitive interrupts, some of which can be used to base the execution of conditional instructions. Three programmable interval timers generate periodic interrupts. Each timer can be independently set to operate in one of three modes:

- Pulse Waveform Generation Mode
- Pulsewidth Count/Capture Mode
- External Event Watchdog Mode

Each timer has one bidirectional pin and four registers that implement its mode of operation:

- A 7-Bit Configuration Register
- A 32-Bit Count Register
- A 32-Bit Period Register
- A 32-Bit Pulsewidth Register

A Single Status Register supports all three timers. A bit in the Mode Status Register globally enables or disables all three timers, and a bit in each timer's Configuration Register enables or disables the corresponding timer independently of the others.

Memory
The Melody 32 provides 64 K words of on-chip SRAM memory. This memory is divided into two 32 K blocks located on memory page 0 in the Melody 32's memory map. In addition to the internal and external memory space, the Melody 32 can address two additional and separate off-chip memory spaces: I/O space and boot space.

Internal (On-Chip) Memory
The Melody 32's unified program and data memory space consists of 16M locations that are accessible through two 24-bit address buses, the PMA and DMA buses.

The Melody 32 uses slightly different mechanisms to generate a 24-bit address for each bus. The Melody 32 has three functions that support access to the full memory map.

- The DAGs generate 24-bit addresses for data fetches from the entire Melody 32 memory address range. Because DAG Index (address) Registers are 16 bits wide and hold the lower 16 bits of the address, each of the DAGs has its own 8-bit page register (DMPGx) to hold the most significant eight address bits. Before a DAG generates an address, the program must set the DAG's DMPGx Register to the appropriate memory page.
- The program sequencer generates the addresses for instruction fetches. For relative addressing instructions, the program sequencer bases addresses for relative jumps, calls, and loops on the 24-bit program counter (PC). In direct addressing instructions (two-word instructions), the instruction provides an immediate 24-bit address value. The PC allows linear addressing of the full 24-bit address range.
- For indirect jumps and calls that use a 16-bit DAG Address Register for part of the branch address, the program sequencer relies on an 8-bit Indirect Jump Page (IJPG) Register to supply the most significant eight address bits. Before a cross page jump or call, the program must set the program sequencer's IJPG Register to the appropriate memory page.

The Melody 32 has 1 K word of on-chip ROM that holds boot routines. If peripheral booting is selected, the Melody 32 starts executing instructions from the on-chip boot ROM, which starts the boot process from the selected peripheral. For more information, see the Booting Modes section. The on-chip boot ROM is located on page 255 in the Melody 32's memory space map.

External (Off-Chip) Memory

Each of the Melody 32's off-chip memory spaces has a separate control register, so applications can configure unique access parameters for each space. The access parameters include:

- Read-and-write wait count
- Waitstate Completion Mode
- I/O clock divide ratio
- Write-hold time extension
- Strobe polarity
- Databus width

The core clock and peripheral clock ratios influence the external memory access strobe widths. For more information, see the Clock Signals section.

The off-chip memory spaces are:

- External memory space ($\overline{\text{MS3–0}}$ Pins)
- I/O memory space ($\overline{\text{IOMS}}$ Pin)
- Boot memory space ($\overline{\text{BMS}}$ Pin)

All of these off-chip memory spaces are accessible through the external port, which can be configured for 8-bit or 16-bit data widths.

External Memory Space

External memory space consists of four memory banks. These banks can contain a configurable number of 64 K word pages. At reset, the page boundaries for external memory have:

- Bank0 containing pages 1–63
- Bank1 containing pages 64–127
- Bank2 containing pages 128–191
- Bank3 containing pages 192–254

The MS3-0 memory bank pins select banks 3–0, respectively. The external memory interface decodes the 8 MSBs of the Melody 32 program address to select one of the four banks.

Both the Melody 32 core and DMA-capable peripherals can access the Melody 32's external memory space.

I/O Memory Space

The Melody 32 supports an additional external memory called I/O memory space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports a total of 256 K locations. The first 8 K addresses are reserved for on-chip peripherals. The upper 248 K addresses are available for external peripheral devices.

The Melody 32's instruction set provides instructions for accessing I/O space. These instructions use an 18-bit address that is assembled from an 8-bit I/O page (IOPG) register and a 10-bit immediate value supplied in the instruction. Both the Melody 32 core and a host (through the host port interface) can access I/O memory space.

Boot Memory Space

Boot memory space consists of one off-chip bank with 254 pages. The BMS memory bank pin selects boot memory space. Both the Melody 32 core and DMA-capable peripherals can access the Melody 32's off-chip boot memory space.

After reset, the Melody 32 always starts executing instructions from the on-chip boot ROM.

Depending on the boot configuration, the boot ROM code can start booting the Melody 32 from boot memory. For more information, see the Booting Modes section.

Interrupts

The interrupt controller lets the Melody 32 respond to 17 interrupts with minimum overhead. The controller implements an interrupt priority scheme as shown in Table I, Interrupt Priorities/Addresses.

Applications can use the unassigned slots for software and peripheral interrupts.

Table I. Interrupt Priorities/Addresses

Interrupt	IMASK/ IRPTL	Vector Address*
Emulator (NMI)— Highest Priority	NA	NA
Reset (NMI)	0	0x00 0000
Power-Down (NMI)	1	0x00 0020
Loop and PC Stack	2	0x00 0040
Emulation Kernel	3	0x00 0060
User Assigned Interrupt	4	0x00 0080
User Assigned Interrupt	5	0x00 00A0
User Assigned Interrupt	6	0x00 00C0
User Assigned Interrupt	7	0x00 00E0
User Assigned Interrupt	8	0x00 0100
User Assigned Interrupt	9	0x00 0120
User Assigned Interrupt	10	0x00 0140
User Assigned Interrupt	11	0x00 0160
User Assigned Interrupt	12	0x00 0180
User Assigned Interrupt	13	0x00 01A0
User Assigned Interrupt	14	0x00 01C0
User Assigned Interrupt— Lowest Priority	15	0x00 01E0

*These interrupt vectors start at address 0x10000 when the Melody 32 is in "no boot," run-form-external, memory mode.

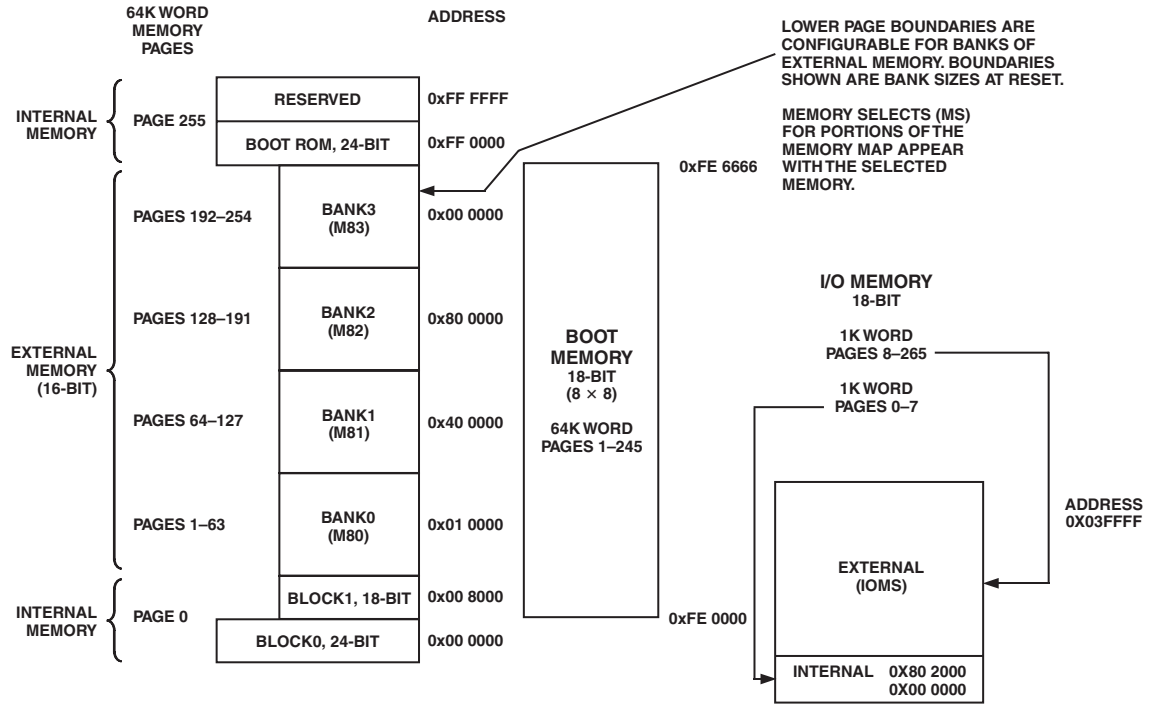


Figure 4. Internal/External Memory, Boot Memory, and I/O Memory Maps

Table II shows the ID and priority at reset of each of the peripheral interrupts. To assign the peripheral interrupts a different priority, applications write the new priority to their corresponding control bits (determined by their ID) in the Interrupt Priority Control Register. The peripheral interrupt's position in the IMASK and IRPTL Register and its vector address depend on its priority level, as shown in Table I. Because the IMASK and IRPTL Registers are limited to 16 bits, any peripheral interrupts assigned a priority level of 11 are aliased to the lowest priority bit position (15) in these registers and share vector address 0x00 01E0.

Table II. Peripheral Interrupts and Priority at Reset

Interrupt	ID	Reset Priority
Slave DMA/Host Port Interface	0	0
SPORT0 Receive	1	1
SPORT1 Transmit	2	2
SPORT1 Receive	3	3
SPORT1 Transmit	4	4
SPORT2 Receive/SPI0	5	5
SPORT2 Transmit/SPI1	6	6
UART Receive	7	7
UART Transmit	8	8
Timer A	9	9
Timer B	10	10
Timer C	11	11
Programmable Flag 0 (any PFx)	12	11
Programmable Flag 1 (any PFx)	13	11
Memory DMA Port	14	11

Interrupt routines can be nested, with higher priority interrupts taking precedence or processed sequentially.

Interrupts can be masked or unmasked with the IMASK Register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The emulation, power-down, and reset interrupts are nonmaskable with the IMASK Register, but software can use the DIS INT instruction to mask the power-down interrupt.

The Interrupt Control (ICNTL) Register controls interrupt nesting and enables or disables interrupts globally. The general-purpose programmable flag (PFx) pins can be configured as outputs, can implement software interrupts, and (as inputs) can implement hardware interrupts. Programmable flag pin interrupts can be configured for level-sensitive, single edge-sensitive, or dual edge-sensitive operation.

DMA Controller

The Melody 32 has a DMA controller that supports automated data transfers with minimal overhead for the Melody 32 core. Cycle stealing DMA transfers can occur between the Melody 32's internal memory and any of its DMA-capable peripherals.

Additionally, DMA transfers can be accomplished between any of the DMA capable peripherals and external devices connected to the external memory interface. DMA capable peripherals include the:

- Host port
- SPORTs
- SPI ports
- UART

Each individual DMA-capable peripheral has a dedicated DMA channel. To describe each DMA sequence, the DMA controller uses a set of parameters called a transfer control block (TCB).

When successive DMA sequences are needed, these TCBs can be linked or chained together, so the completion of one DMA sequence auto-initiates and starts the next sequence. DMA sequences do not contend for bus access with the Melody 32 core; instead DMAs "steal" cycles to access memory.

All DMA transfers use the DMA bus shown in the functional block diagram. Because all of the peripherals use the same bus,

arbitration for DMA Bus access is needed. The I/O Bus Arbitration Priority for DMA Bus access is outlined in Table III.

Table III. I/O Bus Arbitration Priority

DMA Bus Master	Arbitration Priority
SPORT0 Receive DMA	0—Highest
SPORT1 Receive DMA	1
SPORT2 Receive DMA	2
SPORT0 Transmit DMA	3
SPORT1 Transmit DMA	4
SPORT2 Transmit DMA	5
SPI0 Receive/Transmit DMA	6
SPI1 Receive/Transmit DMA	7
UART Receive DMA	8
UART Transmit DMA	9
Host Port DMA	10
Memory DMA	11—Lowest

Host Port

The Host Port is implemented using PF pins and is SPI compatible. Any host microcontroller can communicate with Melody 32 using this port. The host can send commands and parameters and Melody 32 can send status data using this port. This provides simplex bidirectional communication.

Melody 32 Serial Ports (SPORTs)

The Melody 32 incorporates three complete synchronous serial ports (SPORT0, SPORT1, and SPORT2) for serial and multiprocessor communications. The SPORTs support the following features:

- Bidirectional operation—Each SPORT has independent transmit and receive pins.
- Buffered (8 deep) transmit and receive ports—Each port has a data register for transferring data-words to and from other Melody 32 components and shift registers for shifting data in and out of the data registers.
- Clocking—Each transmit and receive port can either use an external serial clock (< 75 MHz) or generate its own, in frequencies ranging from 1144 Hz to 75 MHz.
- Wordlength—Each SPORT supports serial data-words from three bits to 16 bits in length transferred in Big Endian (MSB) or Little Endian (LSB) format.
- Framing—Each transmit and receive port can run with or without frame sync signals for each data-word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulsewidths, and early or late frame sync.
- DMA operations with single-cycle overhead—Each SPORT can automatically receive and transmit multiple buffers of memory data, one data-word each Melody 32 cycle. Either the Melody 32's core or a host processor can link or chain sequences of DMA transfers between a SPORT and memory. The chained DMA can be dynamically allocated and updated through the transfer control blocks (TCBs–DMA parameters) that set up the chain.
- Interrupts—Each transmit and receive port generates an interrupt upon completing the transfer of a data-word or after transferring an entire data buffer or buffers through DMA.

Serial Peripheral Interface (SPI) Ports

The Melody 32 has two SPI compatible ports that enable the Melody 32 to communicate with multiple SPI compatible devices.

These ports are multiplexed with SPORT2, so either SPORT2 or the SPI ports are active, depending on the state of the OPMODE Pin during hardware reset.

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSIx, and Master Input-Slave Output, MlSOx) and a clock pin (Serial Clock, SCKx).

Two SPI chip select input pins ($\overline{\text{SPISSx}}$) let other SPI devices select the Melody 32, and 14 SPI chip select output pins (SPIxSEL7–1) let the Melody 32 select other SPI devices.

The SPI select pins are reconfigured programmable flag pins. Using these pins, the SPI ports provide a full duplex, synchronous serial interface, which supports both master and slave modes and multimaster environments.

Each SPI port's baud rate and clock phase/polarities are programmable:

$$SPIClockrate = \frac{HCLK}{2 \times SPIBAUD}$$

Each has an integrated DMA controller, configurable to support both transmit and receive data streams. The SPI's DMA controller can only service unidirectional accesses at any given time.

The Melody 32 processor core runs at a maximum 160 MHz clock. Peripherals like serial ports, SPI port, UART, DMA controller, external memory interface, and boot memory interface are allowed to run at a lower speed. The clock at which the peripherals run is called HCLK. This peripheral clock is a fraction of the processor core clock (160 MHz). The divide ratio is programmable for each peripheral and external memory interfaces independently.

During transfers, the SPI ports simultaneously transmit and receive by serially shifting data in and out on their two serial data lines.

The serial clock line synchronizes the shifting and sampling of data on the two serial data lines. In Master Mode, the Melody 32's core performs the following sequence to set up and initiate SPI transfers:

1. Enables and configures the SPI port operation (data size and transfer format).
2. Selects the target SPI slave with an SPlxSELy output pin (reconfigured programmable flag pin).
3. Defines one or more TCBs in Page 0 of I/O memory space (optional in DMA Mode only).
4. Enables the SPI DMA engine and specifies transfer direction (optional in DMA Mode only).
5. In non-DMA Mode only, reads or writes the SPI port receive or transmit data buffer.

The SCKx line generates the programmed clock pulses for simultaneously shifting data out on MOSIx and shifting data in on MlSOx. In DMA mode only, transfers continue until the SPI DMA word count transitions from 1 to 0.

In Slave Mode, the Melody 32's core performs the following sequence to set up the SPI port to receive data from a master transmitter:

1. Enables and configures the SPI slave port to match the operation parameters set up on the master (data size and transfer format) SPI transmitter.
2. Defines and generates a receive TCB in Page 0 of memory space to interrupt at the end of the data transfer (optional in DMA Mode only).
3. Enables the SPI DMA engine for a receive access (optional in DMA Mode only).
4. Starts receiving the data on the appropriate SPI SCKx edges after receiving an SPI chip select on an SPISSx input pin (reconfigured programmable flag pin) from a master.

   In DMA Mode only, reception continues until the SPI DMA word count transitions from 1 to 0. The Melody 32's core could continue, by queuing up the next command TCB.

A slave mode transmit operation is similar, except the Melody 32's core specifies the data buffer in memory space from which to transmit data, generates and relinquishes control of the transmit TCB, and begins filling the SPI port's data buffer. If the SPI controller isn't ready on time to transmit, it can transmit a "zero" word.

UART Port

The UART Port provides a simplified UART interface to another peripheral or host. It performs full duplex, asynchronous transfers of serial data. Options for the UART include support for 5–8 data bits; 1 or 2 stop bits; and none, even, or odd parity. The UART Port supports two modes of operation:

- PIO (programmed I/O)
  The Melody 32's core sends or receives data by writing or reading I/O-mapped UATX or UARX Registers, respectively. The data is double-buffered on both transmit and receive.
- DMA (direct memory access)
  The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory.

The UART has two dedicated DMA channels. These DMA channels have lower priority than most DMA channels because of their relatively low service rates.

The UART's baud rate serial data format, error code generation and status, and interrupts are programmable:

- Supported bit rates range from 9.5 bits to 6.25 M bits per second (100 MHz peripheral clock)
- Supported data formats are 7-bit or 12-bit frames
- Transmit and receive status can be configured to generate maskable interrupts to the Melody 32's core

UART Clock Rate Calculation

The timers can be used to provide a hardware-assisted autobaud detection mechanism for the UART interface. (D = 1 to 65536)

$$UARTClockrate = \frac{HCLK}{16 \times D}$$

PROGRAMMABLE FLAG (PFX) PINS

The Melody 32 has 16 bidirectional, general-purpose I/O, Programmable Flag (PF15–0) pins. The PF7–0 pins are dedicated to general-purpose I/O.

The PF15-8 pins serve either as general-purpose I/O pins (if the Melody 32 is connected to an 8-bit external databus) or serve as DATA 15–8 lines (if the Melody 32 is connected to a 16-bit external databus).

The programmable flag pins have special functions for clock multiplier selection and for SPI port operation. For more information, see the Clock Signals section.

Ten memory-mapped registers control operation of the programmable flag pins:

- Flag Direction Register:
  Specifies the direction of each individual PFx pin as input or output.
- Flag Control and Status Registers:
  Specify the value to drive on each individual PFx output pin. As input, software can predicate instruction execution on the value of individual PFx input pins captured in this register. One register sets bits, and one register clears bits.
- Flag Interrupt Mask Registers:
  Enable and disable each individual PFx pin to function as an interrupt to the Melody 32's core. One register sets bits to enable interrupt function, and one register clears bits to disable interrupt function.

  Input PFx pins function as hardware interrupts, and output PFx pins function as software interrupts—latching in the IMASK and IRPTL Registers.
- Flag Interrupt Polarity Register:
  Specifies the polarity (active high or low) for interrupt sensitivity on each individual PFx pin.
- Flag Sensitivity Registers:
  Specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge sensitivity.

Low Power Operation

The Melody 32 has four power options that significantly reduce the power dissipation when the device operates under standby conditions. To enter any of these modes, the Melody 32 executes an IDLE instruction. The Melody 32 uses configuration of the PDWN, STOPCK, and STOPALL Bits in the PLLCTL Register to select between the low power modes as the Melody 32 executes the IDLE. Depending on the mode, an IDLE shuts off clocks to different parts of the Melody 32 in the different modes. The low power modes are:

- Idle
- Power-down core
- Power-down core/peripherals
- Power-down all

When the Melody 32 is in Idle Mode, the Melody 32 core stops executing instructions, retains the contents of the instruction pipeline, and waits for an interrupt. The core clock and peripheral clock continue running. To enter Idle Mode, the Melody 32 can execute the IDLE instruction anywhere in code. To exit Idle Mode, the Melody 32 responds to an interrupt and (after two cycles of latency) resumes executing instructions with the instruction after the IDLE.

When the Melody 32 is in Power-Down Core Mode, the Melody 32 core clock is off, but the Melody 32 retains the contents of the pipeline and keeps the PLL running. The peripheral bus keeps running, letting the peripherals receive data.

To enter Power-Down Core Mode, the Melody 32 executes an IDLE instruction after performing the following tasks:

Enter a power-down interrupt service routine:

1. Check for pending interrupts and I/O service routines
2. Clear (= 0) the PDWN Bit in the PLLCTL Register
3. Clear (= 0) the STOPALL Bit in the PLLCTL Register
4. Set (= 1) the STOPCK Bit in the PLLCTL Register

To exit Power-Down Core Mode, the Melody 32 responds to an interrupt and after two cycles of latency, resumes executing instructions with the instruction after the IDLE.

When the Melody 32 is in Power-Down Core/Peripherals Mode, the Melody 32 core clock and peripheral bus clock are off, but the Melody 32 keeps the PLL running. The Melody 32 does not retain the contents of the instruction pipeline.

The peripheral bus is stopped, so the peripherals cannot receive data. To enter Power-Down Core/Peripherals Mode, the Melody 32 executes an IDLE instruction after performing the following tasks:

Enter a power-down interrupt service routine:

1. Check for pending interrupts and I/O service routines
2. Clear (= 0) the PDWN Bit in the PLLCTL Register
3. Set (= 1) the STOPALL Bit in the PLLCTL Register

To Exit Power-Down Core/Peripherals Mode, the Melody 32 responds to a wake-up event and (after five to six cycles of latency) resumes executing instructions with the instruction after the IDLE.

When the Melody 32 is in Power-Down All Mode, the Melody 32 core clock, the peripheral clock, and the PLL are all stopped. The Melody 32 does not retain the contents of the instruction pipeline. The peripheral bus is stopped, so the peripherals cannot receive data.

To enter Power-Down All Mode, the Melody 32 executes an IDLE instruction after performing the following tasks.

Enter a power-down interrupt service routine:

1. Check for pending interrupts and I/O service routines
2. Set (= 1) the PDWN Bit in the PLLCTL Register

To exit Power-Down Core/Peripherals Mode, the Melody 32 responds to an interrupt and (after 500 cycles to restabilize the PLL) resumes executing instructions with the instruction after the IDLE.

CLOCK SIGNALS

The Melody 32 can be clocked by a crystal oscillator or a buffered, shaped clock derived from an external clock oscillator. If a crystal oscillator is used, the crystal should be connected across the CLKIN and XTAL Pins, with two capacitors connected as shown in Figure 5.

Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used for this configuration.

If a buffered, shaped clock is used, this external clock connects to the Melody 32's CLKIN Pin. CLKIN input cannot be halted, changed, or operated below the specified frequency during normal operation. This clock signal should be a TTL compatible signal. When an external clock is used, the XTAL input must be left unconnected. The peripheral clock is supplied to the CLKOUT Pin.

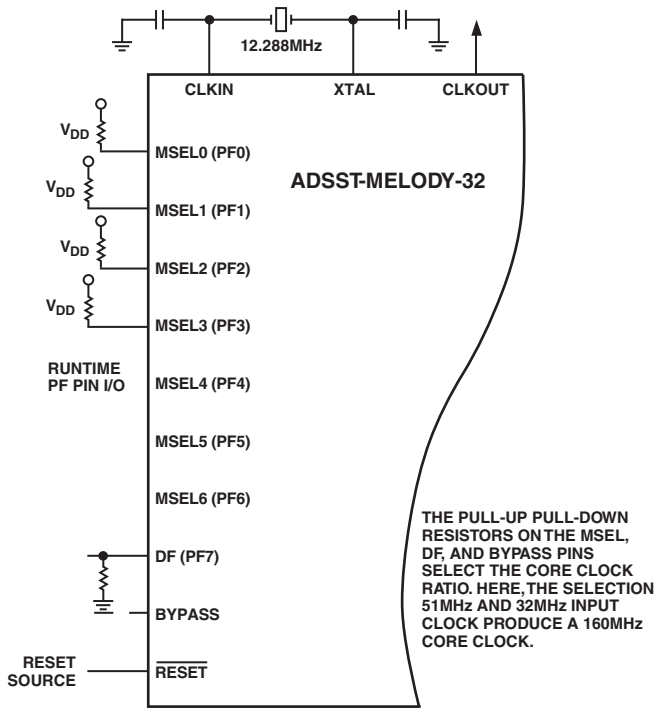


Figure 5. External Crystal Connections

All on-chip peripherals for the Melody 32 operate at the rate set by the peripheral clock. The peripheral clock is either equal to the core clock rate or one-half the Melody 32 core clock rate. This selection is controlled by the IOSEL Bit in the PLLCTL Register.

The maximum core clock is 160 MHz, and the maximum peripheral clock is 100 MHz; the combination of the input clock and core/peripheral clock ratios may not exceed these limits.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ signal initiates a master reset of the Melody 32. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization.

$\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power up, the clock does not continue to run and requires stabilization time when recovering from reset. The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid VDD is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency.

A minimum of 100 µs ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence, the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulsewidth specification, t_{RSP}. The $\overline{\text{RESET}}$ input contains some hysteresis. If using an RC circuit to generate your $\overline{\text{RESET}}$ signal, the circuit should use an external Schmitt trigger.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and resets all registers to their default values where applicable. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed.

Program control jumps to the location of the on-chip boot ROM (0xFF0000).

Power Supplies

The Melody 32 has separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 2.5 V requirement. The external supply must be connected to a 3.3 V supply. All external supply pins must be connected to the same supply.

As indicated in Table IV, the OPMODE Pin has a dual role, acting as a boot mode select during reset and determining SPORT or SPI operation at runtime.

If the OPMODE Pin at reset is the opposite of what is needed in an application during runtime, the application needs to set the OPMODE Bit appropriately during runtime prior to using the corresponding peripheral.

Booting Modes

The Melody 32 has the following mechanism for automatically loading internal program memory after reset.

Table IV. Select Boot Mode (OPMODE, BMODE1, and BMODE0)

OPMODE	BMODE1	BMODE0	Function
0	0	0	Run from Memory External 16 Bits (No Boot)
0	0	1	Boot from EPROM
0	1	0	Boot from Host
0	1	1	Reserved
1	0	0	Execute from Memory External Eight Bits (No Boot)
1	0	1	Boot from UART
1	1	0	Boot from SPI, up to 4 k Bits
1	1	1	Boot from SPI, > 4 k Bits up to 512 k Bits

The OPMODE, BMODE1, and BMODE0 pins, sampled during hardware reset, and three bits in the reset configuration register implement these modes:

- Boot from Memory External 16 Bits—The memory boot routine located in boot ROM memory space executes a boot stream formatted program located at Address 0x10000 of boot memory space, packing 16-bit external data into 24-bit internal data. The external port interface is configured for the default clock multiplier (128) and read waitstates (7).
- Boot from EPROM—The EPROM boot routine located in boot ROM memory space executes a boot stream formatted program located at Address 0x10000 of boot memory space, packing 8-bit or 16-bit external data into 24-bit internal data. The external port interface is configured for the default clock multiplier (32) and read waitstates (7).
- Execute from Memory External Eight Bits (No Boot)—Execution starts from Page 1 of external memory space, packing either 8-bit or 16-bit external data into 24-bit internal data. The external port interface is configured for the default clock multiplier (128) and read waitstates (7).
- Boot from UART—The host downloads a boot stream formatted program using an autobaud handshake sequence. The host agent selects a baud rate within the UART's clocking capabilities.

  After a hardware reset, the DSP's UART transmits 0xFF values (eight bits data, one start bit, one stop bit, no parity bit) until detecting the start of the first memory block.

  The UART boot routine is located in internal ROM memory space and uses the top 16 locations of Page 0 program memory and the top 272 locations of Page 0 data memory.
- Boot from SPI, up to 4 k bits—The SPI0 Port uses the SPIOSEL1 (reconfigured PF2) output pin to select a single serial EPROM device, submits a read command at Address 0x00, and begins clocking consecutive data into internal or external memory.

  Use only SPI compatible EPROMs of = 4 k bit (12-bit address range). The SPI0 boot routine located in internal ROM memory space executes a boot stream formatted program, using the top 16 locations of Page 0 program memory and the top 272 locations of Page 0 data memory. The SPI boot configuration is SPIBAUD0 = 60 (decimal), CPHA = 1, CPOL = 1, 8-bit data, and MSB first.
- Boot from SPI, from > 4 k bits to 512 k bits—The SP10 Port uses the SPIOSEL1 (reconfigured PF2) output pin to select a single serial EPROM device, submits a read command at Address 0x00, and begins clocking consecutive data into internal or external memory.
- Use only SPI compatible EPROMs of = 4 k bit (16-bit address range). The SP10 boot routine located in internal ROM memory space executes a boot stream formatted program, using the top 16 locations of Page 0 program memory and the top 272 locations of Page 0 data memory.

Output Drive Currents

Figure 6 shows typical I-V characteristics for the output drivers of the ADSST-Melody-32. The curves represent the current drive capability of the output drivers as a function of output voltage.

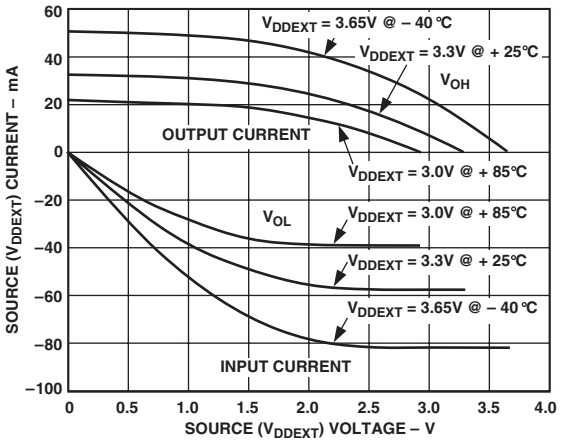


Figure 6. Typical Drive Currents

POWER DISSIPATION

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved.

Using the operation-versus-current information in Table V, designers can estimate the ADSST-Melody-32's internal power supply (V_{DDINT}) input current for a specific application, according to the formula for I_{DDINT} calculation following the table.

Table V. Operation Types Versus Input Current

	K-Grade I_{DDINT}(mA) CCLK = 160 MHz				B-Grade I_{DDINT}(mA)[1] CCLK = 140 MHz			
	Core		Peripheral		Core		Peripheral	
Activity	**Typ[1]**	**Max[2]**	**Typ[1]**	**Max[2]**	**Typ[1]**	**Max[2]**	**Typ[1]**	**Max[2]**
Power-Down[3]	100 µA	600 µA	0	50 µA	100 µA	500 µA	0	50 µA
Idle 1[4]	1	2	5	8	1	2	4	7
Idle 2[5]	1	2	60	70	1	2	55	62
Typical[6]	184	210	60	70	165	185	55	62
Peak[7]	215	240	60	70	195	210	55	62

[1]Test conditions: V_{DDINT} = 2.50 V; HCLK (peripheral clock) frequency = CCLK/2 (core clock/2) frequency; T_{AMB} = 25°C.
[2]Test conditions: V_{DDINT} = 2.65 V; HCLK (peripheral clock) frequency = CCLK/2 (core clock/2) frequency; T_{AMB} = 25°C.
[3]PLL, Core, peripheral clocks, and CLKIN are disabled.
[4]PLL is enabled and Core and peripheral clocks are disabled.
[5]Core CLK is disabled and peripheral clock is enabled.
[6]All instructions execute from internal memory. 50% of the instructions are repeat MACs with dual operand addressing, with changing data fetched using a linear address sequence. 50% of the instructions are type 3 instructions.
[7]All instructions execute from internal memory. 100% of the instructions are MACs with dual operand addressing, with changing data fetched using a linear address sequence.

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- Number of output pins that switch during each cycle (*O*)
- The maximum frequency at which they can switch (*f*)
- Their load capacitance (*C*)
- Their voltage swing (V_{DD})

and is calculated by the formula below:

$$P_{EXT} = O \times C \times V_{DD}^{2} \times f$$

The load capacitance includes the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle. For example, estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory—asynchronous RAM (16-bit)
- One 64 k × 16 RAM chip is used with a load of 10 pF
- Maximum peripheral speed CCLK = 80 MHz, HCLK = 80 MHz
- External data memory writes occur every other cycle, a rate of $1/(4t_{HCLK})$, with 50% of the pins switching
- The bus cycle time is 80 MHz (t_{HCLK} = 12.5 ns)

The P_{EXT} equation is calculated for each class of pins that can drive as shown in Table VI.

Table VI. P_{EXT} Calculation Example

Pin Type	# of Pins	% Switching	(×) C	(×)f (MHz)	(×)V_{DD}^2	P_{EXT}
Address	15	50	10 pF	20	10.9 V	0.01635 W
$\overline{MSx}$	1	0	10 pF	20	10.9 V	0.0000 W
$\overline{WR}$	1		10 pF	40	10.9 V	0.00436 W
Data	16	50	10 pF	20	10.9 V	0.01744 W
CLKOUT	1		10 pF	80	10.9 V	0.00872 W

P_{EXT} = 0.04687 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation with the following formula.

$$P_{TOTAL} = P_{EXT} + P_{INT}$$

Where:

- P_{EXT} is from Table VI
- P_{INT} is I_{DDINT} × 2.5 V, using the I_{DDINT} calculation shown below:

$$I_{DDINT} = (\%Typical \times I_{DDINT-TYPICAL}) + (\%Idle \times I_{DDINT-IDLE}) + (\%Power\,Down \times I_{DDINT-PWRDWN})$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all 1s to all 0s. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Test Conditions
The DSP is tested for output enable, disable, and hold time.

Output Disable Time
Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by –V is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the equation below.

$$t_{DECAY} = \frac{C_L \Delta V}{I_L}$$

The output disable time, t_{DIS}, is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 7. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays –V from the measured output high or output low voltage. The t_{DECAY} is calculated with test loads C_L and I_L, and with –V equal to 0.5 V.

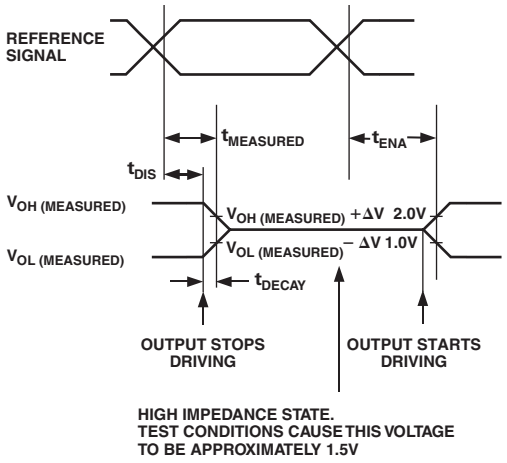


Figure 7. Output Enable/Disable

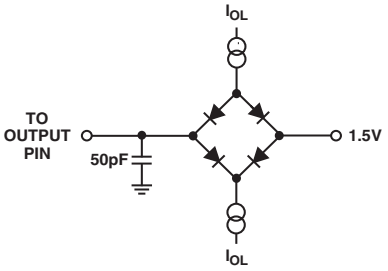


Figure 8. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 9. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time
Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time, t_{ENA}, is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 7. If multiple pins (such as the databus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation
To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation in the Output Disable Time section. Choose –V to be the difference between the ADSST-Melody-32's output voltage and the input threshold for the device requiring the hold time. A typical –V will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

Capacitive Loading
Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 11). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 10 and Figure 11 show how output rise time varies with capacitance. These figures also show graphically how output delays and holds vary with load capacitance. *Note that this graph or derating does not apply to output disable delays; see the Output Disable Time section.* The graphs in these figures may not be linear outside the ranges shown.

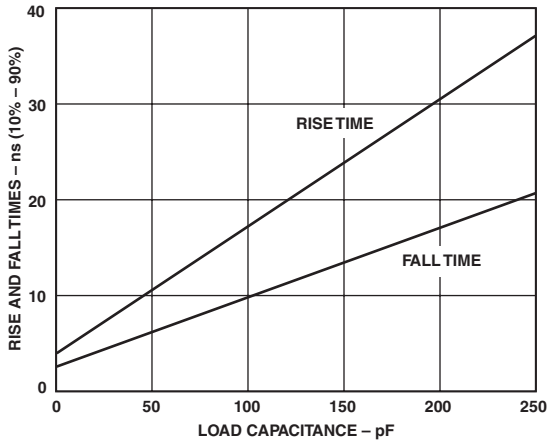


Figure 10. Typical Output Rise Time (10% – 90%, V_{DDEXT} = Minimum at Maximum Ambient Operating Temperature) vs. Load Capacitance

Environmental Conditions
The thermal characteristics in which the DSP is operating influence performance.

Thermal Characteristics
The ADSST-Melody-32 comes in a 144-lead LQFP package. It is specified for an ambient temperature (T_{AMB}) as calculated using the formula that follows.

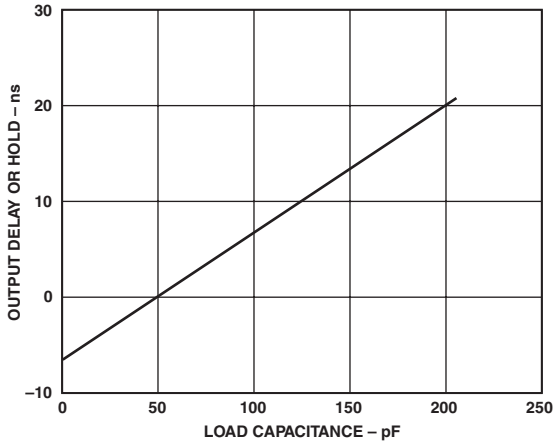


Figure 11. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature)

To ensure that the T_{AMB} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. A heatsink should be attached to the ground plane (as close as possible to the thermal pathways) with a thermal adhesive.

$$T_{AMB} = T_{CASE} - PD \times \theta_{CA}$$

Where:

- T_{AMB} = Ambient temperature (measured near top surface of package)
- *PD* = Power dissipation in W (this value depends upon the specific application; a method for calculating *PD* is shown under Power Dissipation)
- θ_{CA} = Value from Table VII
- For the LQFP package: θ_{JC} = 0.96°C/W

Table VII. θ_{CA} Values*

Airflow, Linear Ft./Min.	0	100	200	400	600
Airflow, Meters/Second	0	0.5	1	2	3
LQFP, θ_{CA} (°C/W)	44.3	41.4	38.5	35.3	32.1

*These are preliminary estimates.

SOUND FIELD SIMULATION, SPEAKER EQUALIZATION, AND EQUALIZATION EFFECTS

Reverberation (reverb for short) is one of the most heavily used effects in music. When you mention reverb to a musician, many will immediately think of a signal processor, or the reverb knob on their amplifier. But many people do not realize how important reverberation is, and that we actually hear reverb every day, without any special processors. The series of delayed and attenuated sound waves is what we call reverb, and this is what creates the "spaciousness" of a room. Figure 12 shows the basic simulator using the reverberation algorithm. Using the reverberation filters and combined processing, the following effects are simulated.

Figure 12 shows the proper setup for speaker equalization.

Hall Reverb
The hall reverb is an algorithm with a natural sound and smooth, colorless decay. Fixed room size and decay time parameters allow simulation of delayed spaces.
Parameters: Delay

Stadium Reverb
The stadium reverb is an algorithm with a dense reverberation and smooth decay.
Parameters: Delay

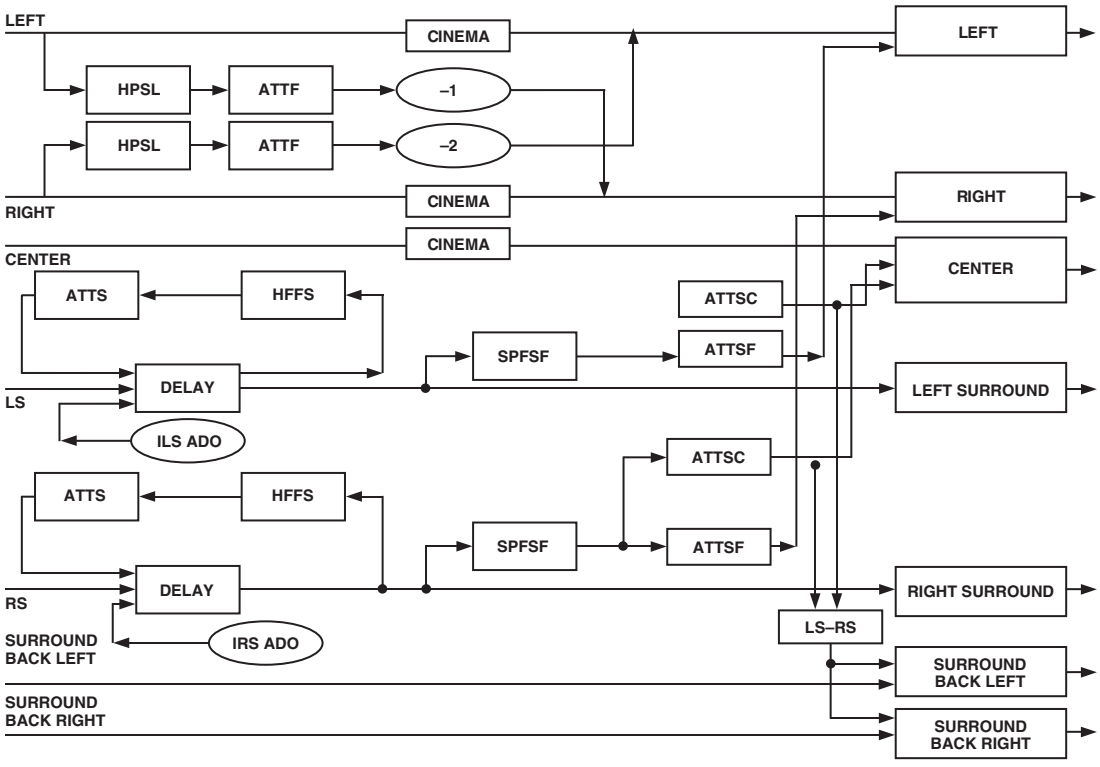


Figure 12. Speaker Equalization

Club Reverb
The club reverb is an algorithm with a reverberation and smooth decay.
Parameters: Delay

Music
A music algorithm simulating a music hall.

Cinema
A cinema-like surround sound is simulated using special filters.

Speaker Equalization
Digital signal processing has many advantages over analog processing. Digital processing allows the application of a wide range of mathematics. This provides more reliability, configurability, flexibility, and low noise susceptibility, resulting in very good performance in the digital system.

Loudspeakers are designed to have a uniform frequency response. But in case of the low cost, size, and the mechanical design constraints, the response of the speaker system is less uniform. In this case, in many audio systems, speaker equalization is performed to shape this response according to the listener. Figure 13 shows the dual loudness curves for the Melody 32 system.

Speaker equalization enables:

- Correct speaker response
- Enhancing some bands of frequencies for a better listening experience

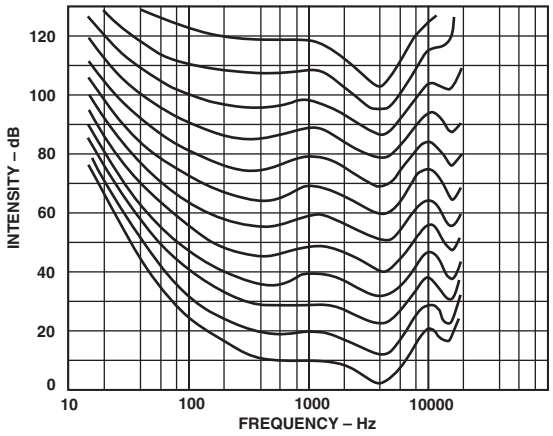


Figure 13. Dual Loudness Curves

The frequency band can be designed according to the speaker response. The variables A1, A2, and A3 are the parameters to adjust the sound pressure level. Figure 14 shows an example.

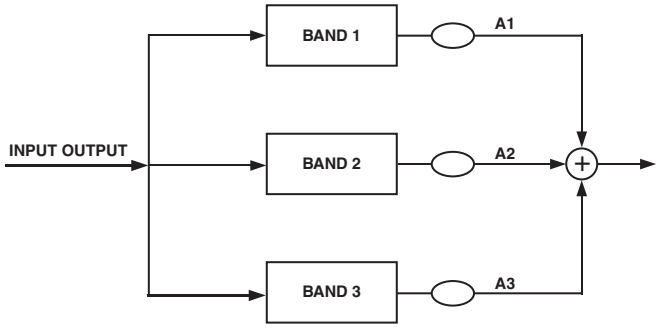


Figure 14. Frequency Bands

Equalization Effects (Pop, Rock, Classic, and Jazz)
A three-band digital graphic equalizer is used to provide the predefined equalizer functions of POP, ROCK, JAZZ, and CLASSIC. The three-band equalizer is applied to all the input channels. The preset values are fixed to provide the maximum effect in a small room.

Figures 15–22 plot the various, predefined equalization effects.

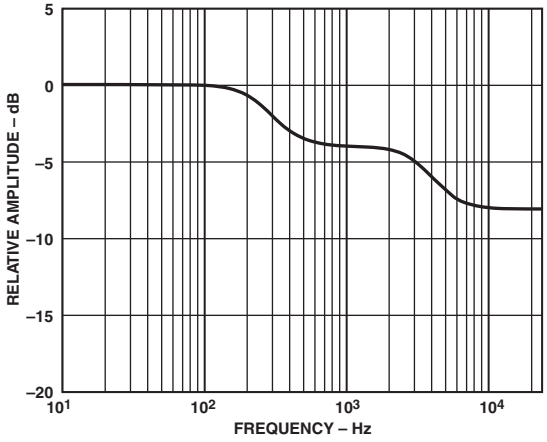


Figure 15. Equalization Effect – Classic Front

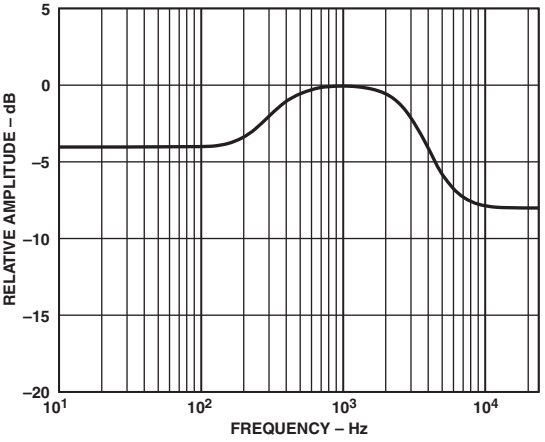


Figure 16. Equalization Effect – Classic Center

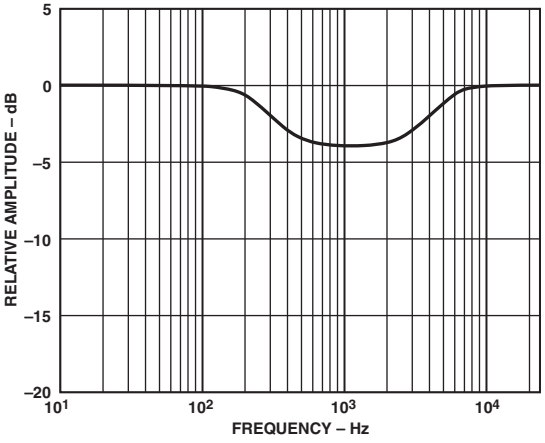


Figure 17. Equalization Effect – Jazz Front

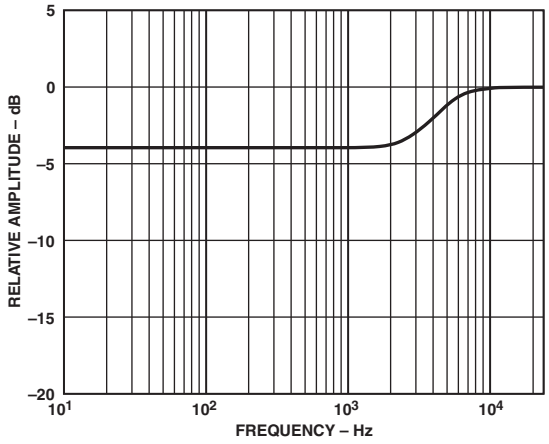


Figure 18. Equalization Effect – Jazz Surround

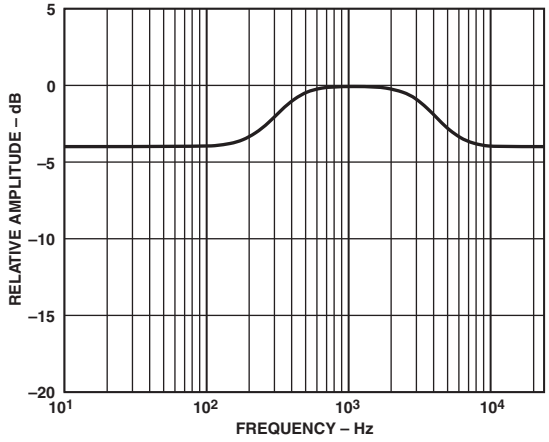


Figure 19. Equalization Effect – Pop Front and Center

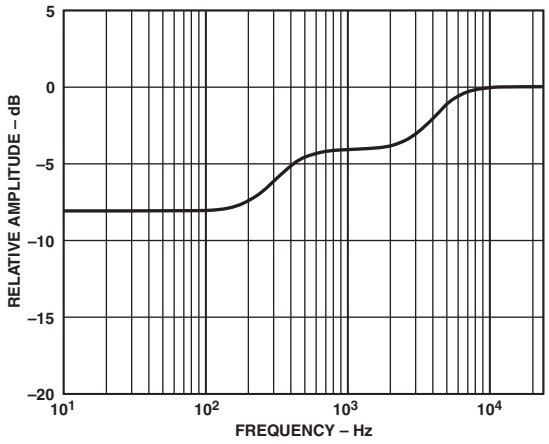


Figure 20. Equalization Effect – Rock Front

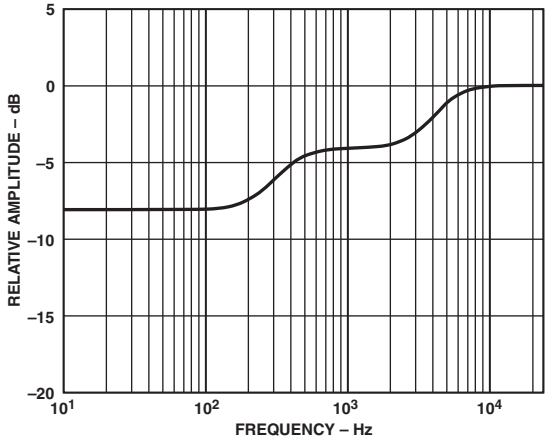


Figure 21. Equalization Effect – Rock Center

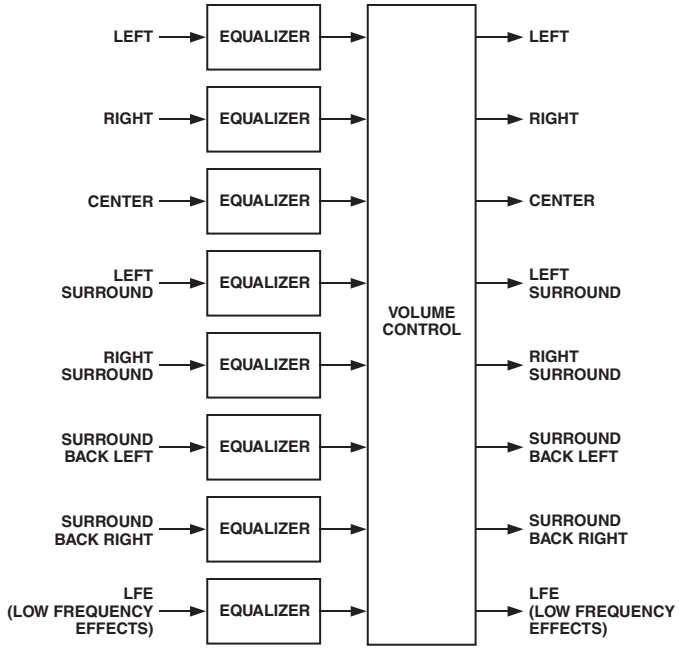
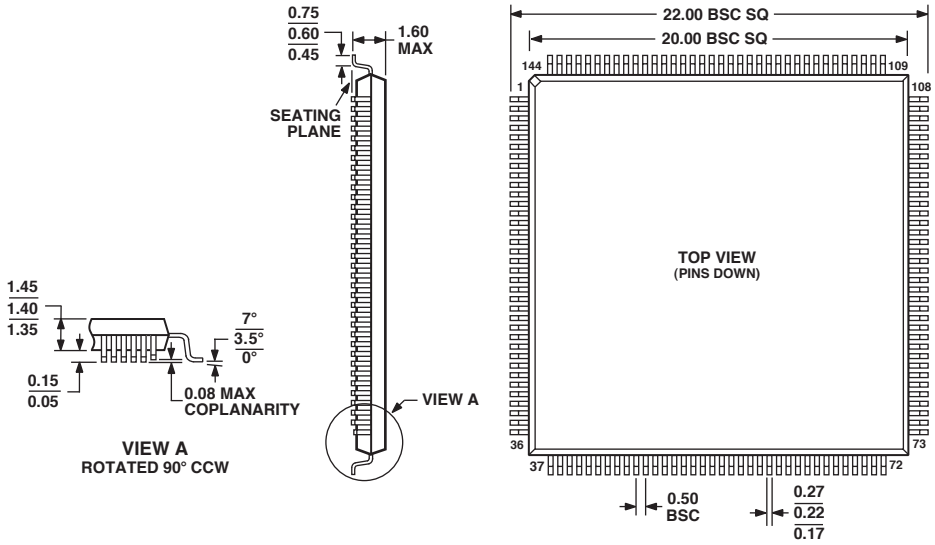


Figure 22. Equalization Effect

OUTLINE DIMENSIONS

144-Lead Low Profile Quad Flatpack [LQFP]
(ST-144)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BFB

NOTES
1. THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION, WHEN MEASURED IN THE LATERAL DIRECTION
2. CENTER DIMENSIONS ARE NOMINAL

Revision History

Location	Page
7/02—Data Sheet changed from REV. 0 to REV. A.	
Edits to GENERAL DESCRIPTION	1
Inserted new REFERENCE BLOCK DIAGRAM	1

C02776–0–7/02(A)

PRINTED IN U.S.A.