REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-07-20

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 8K X 8-BIT PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90803
A	67268	

SHEET 1

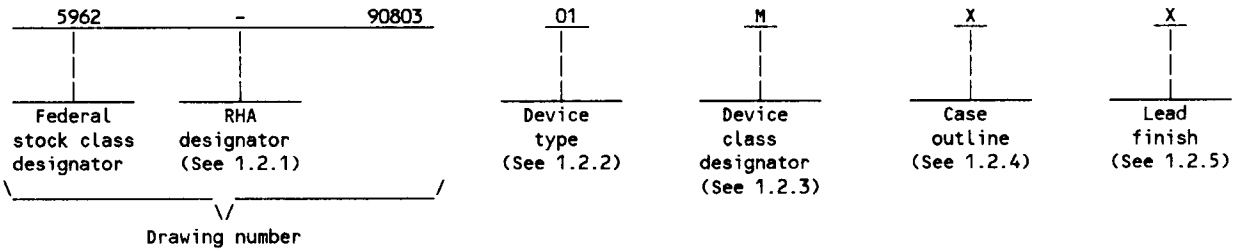
DESC FORM 193
JUL 91

5962-E577-92

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		8K X 8-bit PROM	55 ns
02		8K X 8-bit PROM	45 ns
03		8K X 8-bit PROM	35 ns
04		8K X 8-bit PROM	25 ns
05		8K X 8-bit PROM	55 ns
06		8K X 8-bit PROM	45 ns
07		8K X 8-bit PROM	35 ns
08		8K X 8-bit PROM	25 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range to ground potential (V_{CC}) . . . . . -0.5 V dc to +7.0 V dc
DC voltage applied to the outputs in the high-Z state . . -0.5 V dc to +7.0 V dc
DC input voltage . . . . . -3.0 V dc to +7.0 V dc
DC program voltage . . . . . 13.0 V dc
Maximum power dissipation . . . . . 1.0 W 2/
Lead temperature (soldering, 10 seconds) . . . . . +260°C
Thermal resistance, junction-to-case (θ_{JC}) . . . . . See MIL-STD-1835
Junction temperature (T_J) . . . . . +175°C
Storage temperature range (T_{STG}) . . . . . -65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) . . . . . +4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND) . . . . . 0 V dc
Input high voltage (V_{IH}) . . . . . 2.0 V dc minimum
Input low voltage (V_{IL}) . . . . . 0.8 V dc maximum 3/
Case operating temperature range (T_C) . . . . . -55°C to +125°C

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) . . . . . XX percent 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
3/ V_{IL} negative undershoots to a minimum of -3.0 V dc are allowed for pulse widths < 10 ns.
4/ When a Qualified Manufacturer's List (QML) source exists, a values will be provided.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Avenue, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard E1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

(Non-Government standards and other publications are normally available from the organizations that prepare of distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.4), the devices shall be programmed by the manufacturer prior to test with a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.4.1 Single event phenomena (SEP). SEP test limits are specified in table IB.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}, V_{IL}$, I_{OH} = -4 mA	1, 2, 3	01-03, 05-07	2.4		V
		I_{OH} = -2 mA		04, 08			
Output low voltage	V_{OL}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}, V_{IL}$, I_{OL} = 16 mA	1, 2, 3	01-03, 05-07		0.4	V
		I_{OL} = 6 mA		04, 08			
Input high voltage 1/	V_{IH}		1, 2, 3	All	2.0		V
Input low voltage 1/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	$V_{IN} = V_{CC}$ to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	$V_{OUT} = V_{CC}$ to GND	1, 2, 3	ALL	-10	10	µA
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND	1, 2, 3	All		-100	mA
Power supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 to 3.0 V, f = f_{MAX} 4/	1, 2, 3	01-03, 05-07		120	mA
				04, 08		140	
Standby supply current	I_{CC2}	V_{CC} = 5.5 V, $\overline{CS} \ge V_{IH}$, I_{OUT} = 0 mA	1, 2, 3	01-03, 05-07		30	mA
				04, 08		50	
Input capacitance 3/	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V, T_A = +25°C, f = 1 MHz (see 4.4.1c)	4	All		10	pF
Output capacitance 3/	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0 V, T_A = +25°C, f = 1 MHz (see 4.4.1c)	4	All		10	pF
Functional tests		See 4.4.1d	7, 8	All			
Address to output valid	t_{AA}	See figures 4 and 5 and note 5/	9, 10, 11	01, 05		55	ns
				02, 06		45	
				03, 07		35	
				04, 08		25	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Chip select active to output valid	t_{ACS}	See figures 4 and 5 and note 5/	9, 10, 11	01		55	ns
				02		45	
				03		40	
				04		25	
				05		35	
				06		30	
				07		20	
				08		15	
Chip select active to power-up 3/	t_{PU}		9, 10, 11	01-04	0		ns
Chip select inactive to power-down 3/	t_{PD}		9, 10, 11	01		55	ns
				02		45	
				03		35	
				04		25	
Chip select inactive to high-Z 3/	t_{HZCS}	See figures 4 and 5 and note 5/ and 6/	9, 10, 11	01		55	ns
				02		45	
				03, 05		35	
				04, 07		25	
				06		30	
				08		15	

1/ These are absolute values with respect to device ground and all overshoots and undershoots due to system or tester noise are included.
2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.
4/ At $f = f_{max}$, address inputs are cycling at the maximum frequency of $1/t_{AA}$.
5/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 5.
6/ Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 5.

Device types	All	
Case outlines	J, K, and L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	A_{12}	O_5
19	A_{11}	O_6
20	$\overline{CS}$	O_7
21	A_{10}	NC
22	A_9	A_{12}
23	A_8	A_{11}
24	V_{CC}	$\overline{CS}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Type	Mode	Outputs	A_{12}	A_{11}	$\overline{CS}$	A_{10}	A_9	A_8	V_{CC}	Power
All	Read	D_{OUT}	A_{12}	A_{11}	V_{IL}	A_{10}	A_9	A_8	V_{CC}	I_{CC}
01-04	Not selected	High-Z	A_{12}	A_{11}	V_{IH}	A_{10}	A_9	A_8	V_{CC}	I_{SB}
05-08	Not selected	High-Z	A_{12}	A_{11}	V_{IH}	A_{10}	A_9	A_8	V_{CC}	I_{CC}
All	Program 1/	D_{IN}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{ILP}	V_{IHP}	V_{CCP}	I_{CC}
All	Program inhibit 1/	High-Z	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{IHP}	V_{CC}	I_{CC}
All	Program verify 1/	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC}
All	Blank check 1/	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC}

1/ See 4.5.

FIGURE 2. Truth table.

NOTE: When a qualified source exists, a circuit shall be provided and placed on this page.

FIGURE 3. Radiation hardness bias circuit.

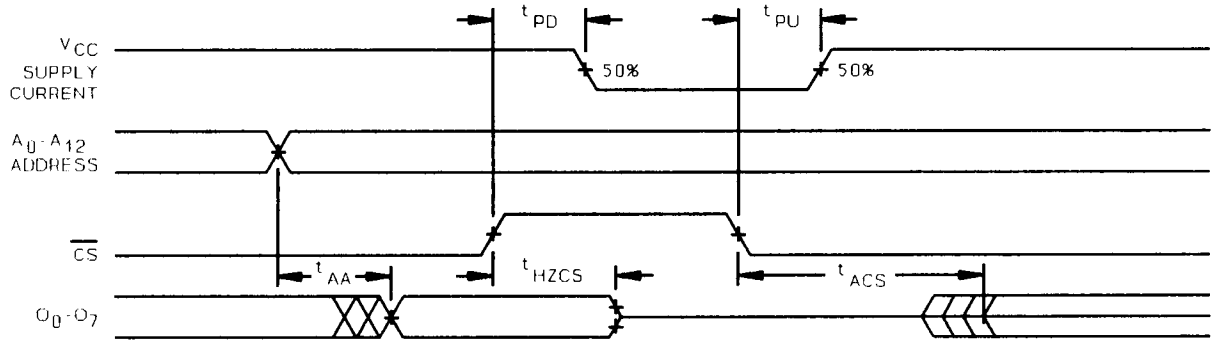
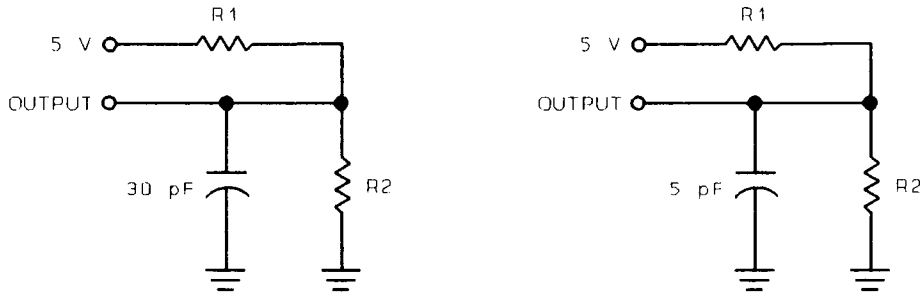


FIGURE 4. Switching waveforms.



Circuit A
Output load

Circuit B
Output load for t_{HZCS}

NOTE: Including scope and jig. (minimum values)

	Device types	
Load	01-03 05-07	04, 08
R1	250 Ω	658 Ω
R2	167 Ω	403 Ω

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 5. Output load circuit and test conditions.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.10.1 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.10.2 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIa. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.3 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE IB. SEP test limits. 1/ 2/

Device type	Temperature (±10°C)	Memory pattern	V_{CC} = 4.5 V Effective threshold LET no upsets ($Mev/(mg/cm^2)$)	V_{CC} = 4.5 V Maximum device cross section (cm^2)	Bias for latch-up test V_{CC} = 6.5 V no latch-up LET

1/ This table blank, table will be filled in when a qualified vendor exists.
2/ For SEP test conditions, see 4.4.5 herein.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as 3.1.9 through 3.1.13 (preburn-in electrical parameters through interim postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M the burn-in test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S the burn-in test circuit shall be submitted to the qualifying activity.

(1) Static burn-in for device classe S (method 1015 of MIL-STD-883, test condition A).

a. All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ±0.5 V. R1 = 220Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

b. V_{CC} = 4.5 V minimum.

c. Ambient temperature (T_A) shall be +125°C minimum.

d. Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

e. A data retention stress test shall be included as part of the screening procedure and shall consist of the following: (Steps 1 through 4 are performed at the wafer level.)

(1) Program 100 percent of the total number of cells, excluding the security bit.

(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C, or 2 hours at +300°C for unassembled devices only.

(3) Perform margin test using Vm = +5.7 V at +25°C using loose timing (i.e., $t_{AA} \geq 1\ \mu s$).

(4) Erase.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta Δ limits or electrical parameter limits specified in table IA, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.1.1 Qualification extension for device class B or S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die), to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHZ. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

e. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of Group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than four total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

f. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes B and S the procedures and circuits shall be maintained under document revision control by the manufacturer and shall be made available to the qualifying activity upon request. For device classes Q and V procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. JEDEC Standard No. 17 may be used as a guideline when performing O/V testing.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

a. For device class S steady-state life tests shall be conducted using test condition D and the circuit described in 4.2.1b herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of test specified in table IIC herein.

c. All devices selected for class S electrical testing shall be programmed with a checkerboard pattern or equivalent.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIC herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D. For device class M the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (per method 5005 table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 2,8A,10		1,7,9 or 2,8A,10
2	Static burn-in method 1015	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7*,Δ		1*,7*,Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7*,Δ		1*,7*,Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11,Δ		
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B,Δ		2,3,7, 8A,8B,Δ	1,2,3,7, 8A,8B,9, 10,11,Δ
10	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B
11	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ * indicates PDA applies to subgroup 1 and 7.
4/ ** see 4.4.1c.
5/ Δ indicates delta limit (see table IIC) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).
6/ The device manufacturer may at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in parameters	1015, total of 240 hrs. at +125° C	100%
Radiographic	2012	100%

TABLE IIC. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC2} standby	±10 percent of specified value in table I
I_{IX}	±10 percent of specified value in table I
I_{OZ}	±10 percent of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the purchase order. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

a. RHA tests for device classes B, S, Q, and V for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein RHA samples need not be tested at -55°C or +125°C prior to total dose irradiation.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. The samples shall pass the specified group A electrical parameters for subgroups specified in table IIA herein. Additionally classes Q and V, for quality conformance inspection may be at wafer level.

d. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510 (device classes M, B, and S) and MIL-I-38535 (device classes Q and V) for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure.

e. Prior to and during, total dose irradiation, the devices shall be biased to the worst case conditions established during characterization (see figure 3 herein).

(1) Inputs tested high, V_{CC} = volts dc, R_{CC} = Ω +5 percent, V_{IN} = volts dc, R_{IN} = Ω +20 percent, and alloutputs are open. (Values will be added when they become available.)

(2) Inputs tested low, V_{CC} = volts dc, R_{CC} = Ω +5 percent, V_{IN} = 0.0 V dc, and all outputs are open. (Values will be added when they become available.)

f. SEP testing, shall be performed on all classes S and V devices. SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics of the device. Test four devices with zero failures. ASTM Standard F1192-88 may be used as a guideline when performing SEP testing. For device class V, the device parametrics that influence single event upset immunity shall be monitored at the wafer level as part of a TRB approved wafer level hardness plan. The test conditions for SEP are as follows:

(1) The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

(2) The fluence shall be greater than 100 errors or ≥ 10^7 ions/cm^2.

(3) The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

(4) The particle range shall be ≥ 20 microns in silicon.

(5) The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

(6) Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latch-up measurements.

(7) For SEP test limits, see table IB herein.

g. For device classes M, B, and S, subgroups 1 and 2 of table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

h. Transient dose rate upset testing for classes Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

i. Transient dose rate survivability testing for classes Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence latch-up and device burn-out shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

j. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

(1) RHA delta limits.

(2) RHA upset levels.

(3) Test conditions (SEP).

(4) Number of upsets (SEP).

(5) Number of transients.

(6) Occurrence of latch-up.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Symbols, definitions and functional descriptions.

C_{IN}	Input terminal capacitance.
C_{OUT}	Output terminal capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IX}	Input current.
I_{OZ}	Output current.
T_C	Case temperature.
V_{CC}	Positive supply voltage.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), who was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.