



Integrated Device Technology, Inc.

## HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

**IDT54/74FCT841A/B/C**  
**IDT54/74FCT843A/B/C**  
**IDT54/74FCT844A/B/C**  
**IDT54/74FCT845A/B/C**

### FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT841A/843A/844A/845A equivalent to FAST™ speed
- **IDT54/74FCT841B/843B/844B/845B 25% faster than FAST**
- **IDT54/74FCT841C/843C/844C/845C 40% faster than FAST**
- Buffered common latch enable, clear and preset inputs
- I<sub>OL</sub> = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

### DESCRIPTION:

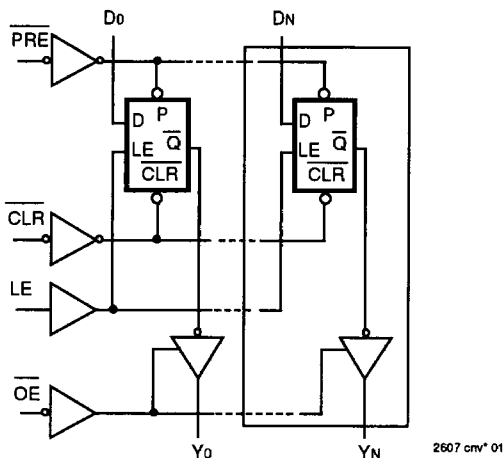
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 is a buffered, 10-bit wide version of the popular '373 function. The IDT54/74FCT843 and IDT54/74FCT844 are 9-bit wide buffered latches with Preset (PRE) and Clear (CLR)—ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845 is an 8-bit buffered latch with all the '843/4 controls, plus multiple enables ( $\overline{OE}_1$ ,  $\overline{OE}_2$ ,  $\overline{OE}_3$ ) to allow multiuser control of the interface, e.g., CS, DMA and RD/WR. It is ideal for use as an output port requiring high I<sub>OL</sub>/I<sub>OH</sub>.

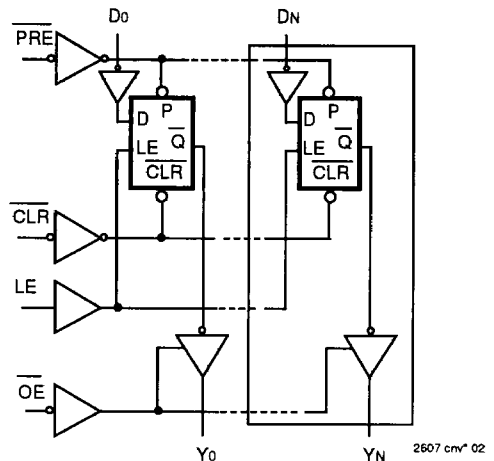
All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

### FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT841/843/845



### IDT54/74FCT844



### PRODUCT SELECTOR GUIDE

		Device		
		10-Bit	9-Bit	8-Bit
Non-Inverting		IDT54/74FCT841A/B/C	IDT54/74FCT843A/B/C	IDT54/74FCT845A/B/C
			IDT54/74FCT844A/B/C	
Inverting				

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FAST is a trademark of National Semiconductor Co.

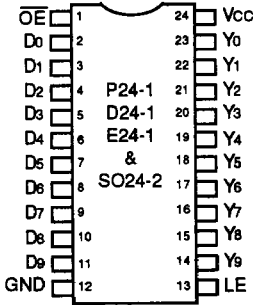
2607 tbi 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES

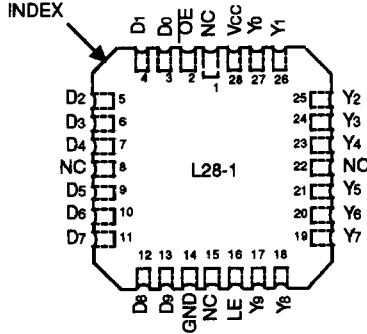
MAY 1992

**PIN CONFIGURATIONS**

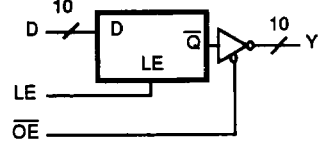
**IDT54/74FCT841 10-BIT LATCH**



**DIP/CERPACK/SOIC  
TOP VIEW**

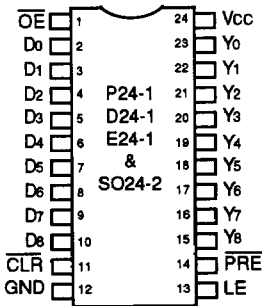


**LCC  
TOP VIEW**

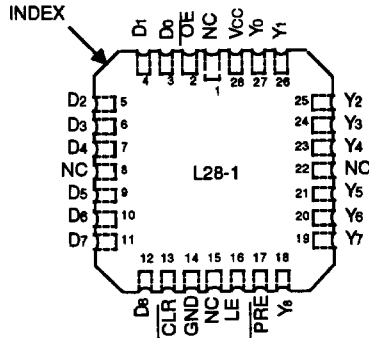


2607 cmv\* 03,04,05

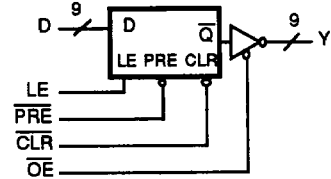
**IDT54/74FCT843/844 9-BIT LATCHES**



**DIP/CERPACK/SOIC  
TOP VIEW**



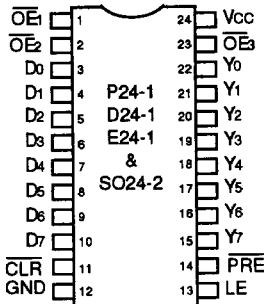
**LCC  
TOP VIEW**



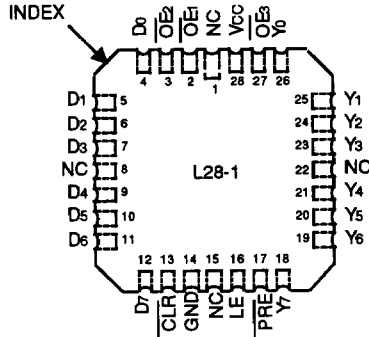
2607 cmv\* 06,07,08

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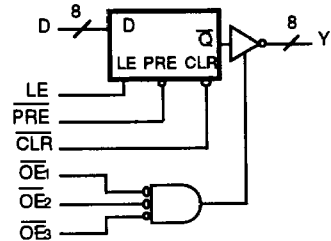
**IDT54/74FCT845 8-BIT LATCH**



**DIP/CERPACK/SOIC  
TOP VIEW**



**LCC  
TOP VIEW**



2607 cmv\* 09,10,11

**PIN DESCRIPTION**

Name	I/O	Description
<b>IDT54/74FCT841/843/845 (Non-Inverting)</b>		
CLR	I	When CLR is low, the outputs are LOW if OE is LOW. When CLR is HIGH, data can be entered into the latch.
Di	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Yi	O	The 3-state latch outputs.
OE	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs (Yi) are in the high-impedance (off) state.
PRE	I	Preset line. When PRE is LOW, the outputs are HIGH if OE is LOW. Preset overrides CLR.
<b>IDT54/74FCT844 (Inverting)</b>		
CLR	I	When CLR is low, the outputs are LOW if OE is LOW. When CLR is HIGH, data can be entered into the latch.
Di	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Yi	O	The 3-state latch outputs.
OE	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs (Yi) are in the high-impedance (off) state.
PRE	I	Preset line. When PRE is LOW, the outputs are HIGH if OE is LOW. Preset overrides CLR.

2607 tbl 02

**FUNCTION TABLE<sup>(1)</sup>**

**IDT54/74FCT841/843/845**

Inputs					Inter- nal	Out- puts	Function
CLR	PRE	OE	LE	Di	Qi	Yi	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

**NOTE:**  
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change,  
Z = High Impedance

2607 tbl 03

**FUNCTION TABLE<sup>(1)</sup>**

**IDT54/74FCT844**

Inputs					Inter- nal	Out- puts	Function
CLR	PRE	OE	LE	Di	Qi	Yi	
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

**NOTE:**  
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change,  
Z = High Impedance

2607 tbl 04

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

- NOTE:** 2607 tbl 05
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
  - Input and Vcc terminals only.
  - Outputs and I/O terminals only.

**CAPACITANCE** (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

- NOTE:** 2607 tbl 06
- This parameter is measured at characterization but not tested.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified: V<sub>Lc</sub> = 0.2V; V<sub>Hc</sub> = Vcc - 0.2V  
Commercial: TA = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: TA = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I <sub>IH</sub>	Input HIGH Current	Vcc = Max. V <sub>I</sub> = Vcc V <sub>I</sub> = 2.7V V <sub>I</sub> = 0.5V V <sub>I</sub> = GND	—	—	5	μA	
I <sub>IL</sub>	Input LOW Current		—	—	-5 <sup>(4)</sup>		
I <sub>OZH</sub>	Off State (High Impedance) Output Current		V <sub>O</sub> = Vcc	—	—		10
I <sub>OZL</sub>			V <sub>O</sub> = 2.7V	—	—		10 <sup>(4)</sup>
		V <sub>O</sub> = 0.5V	—	—	-10 <sup>(4)</sup>		
		V <sub>O</sub> = GND	—	—	-10		
V <sub>IK</sub>	Clamp Diode Voltage	Vcc = Min., I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V	
I <sub>OS</sub>	Short Circuit Current	Vcc = Max. <sup>(3)</sup> , V <sub>O</sub> = GND	-75	-120	—	mA	
V <sub>OH</sub>	Output HIGH Voltage	Vcc = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>Hc</sub> , I <sub>OH</sub> = -32μA	V <sub>Hc</sub>	Vcc	—	V	
		Vcc = Min., I <sub>OH</sub> = -300μA	V <sub>Hc</sub>	Vcc	—		
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -15mA MIL.	2.4	4.3	—		
		I <sub>OH</sub> = -24mA COM'L.	2.4	4.3	—		
V <sub>OL</sub>	Output LOW Voltage	Vcc = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>Hc</sub> , I <sub>OL</sub> = 300μA	—	GND	V <sub>LC</sub>	V	
		Vcc = Min., I <sub>OL</sub> = 300μA	—	GND	V <sub>LC</sub> <sup>(4)</sup>		
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 32mA MIL.	—	0.3	0.5		
		I <sub>OL</sub> = 48mA COM'L.	—	0.3	0.5		

- NOTES:** 2607 tbl 07
- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
  - Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
  - Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
  - This parameter is guaranteed but not tested.

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## POWER SUPPLY CHARACTERISTICS

V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>HC</sub> ; V <sub>IN</sub> ≤ V <sub>LC</sub>		—	0.2	1.5	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open OE = GND LE = V <sub>CC</sub> One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle OE = GND LE = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	1.7	4.0	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.0	5.0	
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 2.5MHz 50% Duty Cycle OE = GND LE = V <sub>CC</sub> Eight Bits Toggling	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	3.2	6.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	5.2	14.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>

$$I_C = I_{CC} + \Delta I_{CC} \cdot DH \cdot NT + I_{CCD} \cdot (f_{CP}/2 + f_i \cdot N_i)$$

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

DH = Duty Cycle for TTL Inputs High

NT = Number of TTL Inputs at DH

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>i</sub> = Input Frequency

N<sub>i</sub> = Number of Inputs at f<sub>i</sub>

All currents are in milliamps and all frequencies are in megahertz.

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**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Conditions <sup>(1)</sup>	FCT841A/843A-844A/845A				FCT841B/843B-844B/845B				FCT841C/843C-844C/845C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
(FCT841, 843, 845) tPLH tPHL	Propagation Delay DI to Y1 (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
(FCT844) tPLH tPHL	Propagation Delay DI to Y1 (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	8.0	1.5	9.0	1.5	7.0	1.5	8.0	ns
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay LE to Y1	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	1.5	6.4	1.5	6.8	ns
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	1.5	15.0	1.5	16.0	
tPLH	Propagation Delay, $\overline{\text{PRE}}$ to Y1	CL = 50pF	1.5	12.0	1.5	14.0	1.5	8.0	1.5	10.0	1.5	7.0	1.5	9.0	ns
tPHL		RL = 500Ω	1.5	14.0	1.5	17.0	1.5	10.0	1.5	13.0	1.5	9.0	1.5	12.0	
tPHL	Propagation Delay, $\overline{\text{CLR}}$ to Y1	CL = 50pF	1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	1.5	9.0	1.5	10.0	ns
tPLH		RL = 500Ω	1.5	14.0	1.5	17.0	1.5	10.0	1.5	10.0	1.5	9.0	1.5	9.0	
tPZH tPZL	Output Enable Time $\overline{\text{OE}}$ to Y1	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	6.5	1.5	7.3	ns
		CL = 300pF <sup>(4)</sup> RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	1.5	12.0	1.5	13.0	
tPHZ tPLZ	Output Disable Time $\overline{\text{OE}}$ to Y1	CL = 5pF <sup>(4)</sup> RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	5.7	1.5	6.0	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.3	
tsu	Data to LE Set-up Time	CL = 50pF	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time	RL = 500Ω	2.5	—	3.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tW	LE Pulse Width <sup>(3)</sup>	HIGH	4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{\text{PRE}}$ Pulse Width <sup>(3)</sup>	LOW	5.0	—	7.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{\text{CLR}}$ Pulse Width <sup>(3)</sup>	LOW	4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{\text{PRE}}$ to LE		4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{\text{CLR}}$ to LE		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

2607 tbl09

