Discontinuted (9/98 - last order; 3/99 last ship)

IBM11D4325B
IBM11D8325B

4M/8M x 32 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	EDO Mode Cycle Time	25ns	30ns

- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Extended Data Out (EDO) access cycle
- Refresh Modes: $\overline{RAS}$-Only, CBR and Hidden Refresh
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications
- Sn/Pb tab versions only
- 16MB versions in TSOP or SOJ packages.
- 32MB version only in SOJ package.

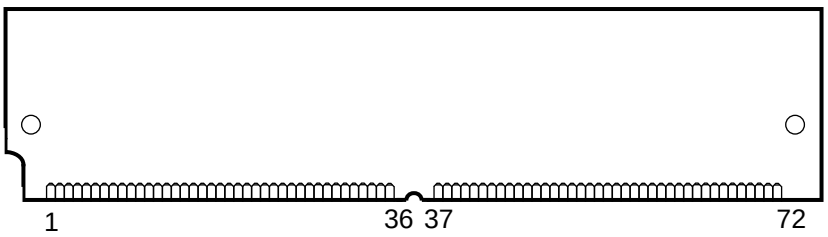
Description

The IBM11D8325B is a 32MB industry standard 72-pin 4-byte single in-line memory module (SIMM) manufactured using EDO DRAMs. The use of EDO DRAMs allows for a reduction in Page Mode Cycle Time from 40ns (Fast Page) to 25ns (EDO, 60ns sort). The module is organized as an 8Mx32 high speed memory array, and is configured as two 4Mx32 banks -each independently selectable via unique $\overline{RAS}$ inputs. The assembly is manufactured with sixteen 4Mx4 devices, each in a 300mil SOJ package, and is compatible with the JEDEC 72-Pin SIMM standard.

The IBM11D4325B is a 16MB half populated version, manufactured with eight 4Mx4 devices each in a 300mil TSOP or SOJ package.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25” long footprint.

Card Outline



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4M/8M x 32 DRAM Module

Pin Description

$\overline{RAS}0$, $\overline{RAS}2$	Row Address Strobe (16MB)
$\overline{RAS}0$ - $\overline{RAS}3$	Row Address Strobe (32MB)
$\overline{CAS}0$ - $\overline{CAS}3$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

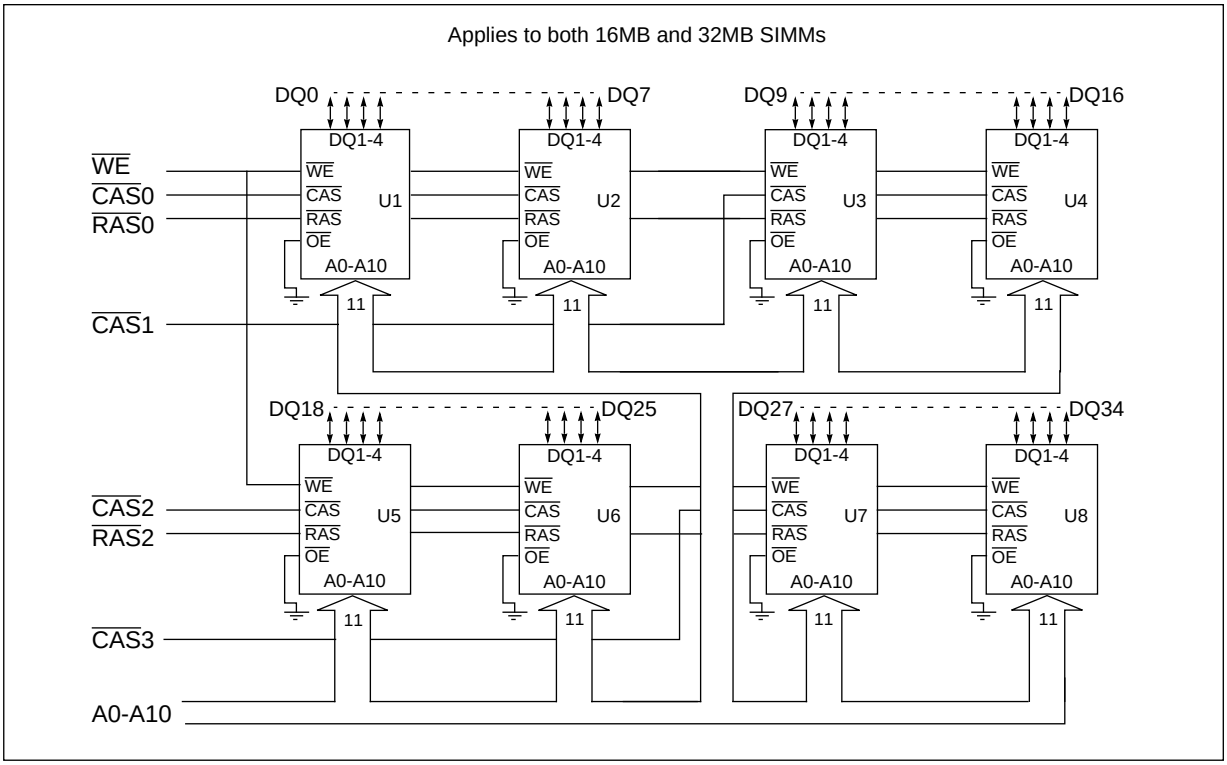
Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	25	DQ24	49	DQ9
2	DQ0	26	DQ7	50	DQ27
3	DQ18	27	DQ25	51	DQ10
4	DQ1	28	A7	52	DQ28
5	DQ19	29	NC	53	DQ11
6	DQ2	30	V_{CC}	54	DQ29
7	DQ20	31	A8	55	DQ12
8	DQ3	32	A9	56	DQ30
9	DQ21	33	$\overline{RAS}3$*	57	DQ13
10	V_{CC}	34	$\overline{RAS}2$	58	DQ31
11	NC	35	NC	59	V_{CC}
12	A0	36	NC	60	DQ32
13	A1	37	NC	61	DQ14
14	A2	38	NC	62	DQ33
15	A3	39	V_{SS}	63	DQ15
16	A4	40	$\overline{CAS}0$	64	DQ34
17	A5	41	$\overline{CAS}2$	65	DQ16
18	A6	42	$\overline{CAS}3$	66	NC
19	A10	43	$\overline{CAS}1$	67	PD1
20	DQ4	44	$\overline{RAS}0$	68	PD2
21	DQ22	45	$\overline{RAS}1$*	69	PD3
22	DQ5	46	NC	70	PD4
23	DQ23	47	$\overline{WE}$	71	NC
24	DQ6	48	NC	72	V_{SS}

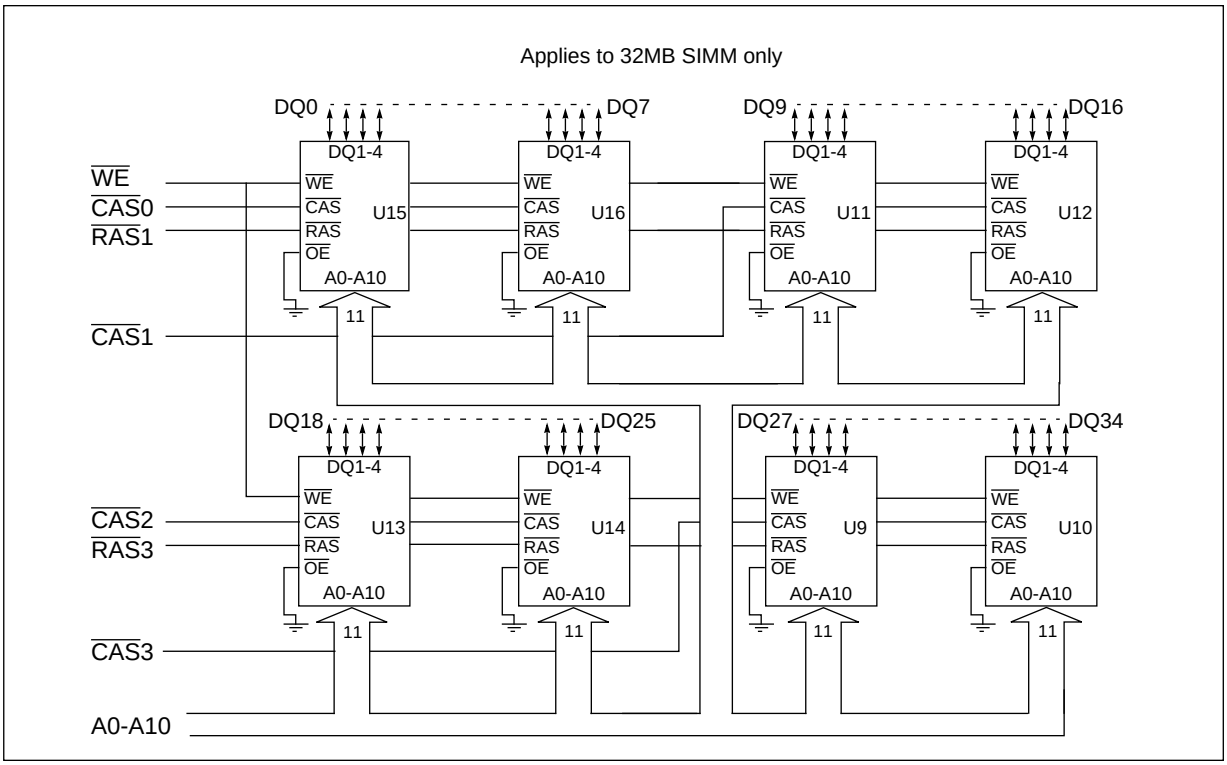
Ordering Information

Part Number	Organization	Speed	Addr.	Leads	Dimensions	Package	Notes
IBM11D4325B-60	4M x 32	60ns	11/11	Sn/Pb	4.25” x 1” x .205”	SOJ	
IBM11D4325B-70		70ns					
IBM11D4325B-60J		60ns					1
IBM11D4325B-70J		70ns					1
IBM11D4325B-60		60ns			4.25” x 1” x .104”	TSOP	
IBM11D4325B-70		70ns					
IBM11D4325B-60T		60ns					1
IBM11D4325B-70T		70ns					1
IBM11D8325B-60	8M x 32	60ns			4.25” x 1” x .360”	SOJ	
IBM11D8325B-70		70ns					
IBM11D8325B-60J		60ns					1
IBM11D8325B-70J		70ns					1

1. DRAM package designator appended to speed portion of part number on assemblies beginning with DRAM die rev E.

Block Diagram





Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby		H	H→X	X	X	X	High Impedance
Read		L	L	H	Row	Col	Valid Data Out
Early-Write		L	L	L	Row	Col	Valid Data In
EDO Mode - Read: 1st Cycle		L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles		L	H→L	H	N/A	Col	Valid Data Out
EDO Mode - Write: 1st Cycle		L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles		L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh		L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	Row	Col	Data Out
	Write	L→H→L	L	L	Row	Col	Data In

Presence Detect

Pin	4M x 32		8M x 32	
	-60	-70	-60	-70
PD1	V_{SS}	V_{SS}	NC	NC
PD2	NC	NC	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC	V_{SS}
PD4	NC	NC	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	3.74 (16MB) 7.5 (32MB)	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active (refresh cycle).

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0V for pulse widths of ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns). Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0V ± 0.5V)

Symbol	Parameter	4M x 32 Max	8M x 32 Max	Units
C_{I1}	Input Capacitance (A0-A10)	55	98	pF
C_{I2}	Input Capacitance (16MB: $\overline{RAS}$0, 32MB: $\overline{RAS}$0, 1)	40	40	pF
C_{I3}	Input Capacitance (16MB: $\overline{RAS}$2, 32MB: $\overline{RAS}$2, 3)	40	40	pF
C_{I4}	Input Capacitance ($\overline{CAS}$)	25	40	pF
C_{I5}	Input Capacitance ($\overline{WE}$)	66	127	pF
$C_{I/O}$	Output Capacitance (DQ0 - DQ34)	13	25	pF

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0V ± 0.5V)

Symbol	Parameter		4M x 32 Min	4M x 32 Max	8M x 32 Min	8M x 32 Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	680	—	696	mA	1, 2, 3
		-70	—	600	—	616		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	16	—	32	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	680	—	696	mA	1, 3, 4
		-70	—	600	—	616		
I_{CC4}	EDO Mode Current Average Power Supply Current, EDO Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{HPC} = t_{HPC} min)	-60	—	520	—	536	mA	1, 2, 3
		-70	—	440	—	450		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	8	—	16	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	680	—	696	mA	1, 3, 4
		-70	—	600	—	616		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-40	+40	-40	+40	µA	
		$\overline{CAS}$	-20	+20	-40	+40		
		All others	-80	+80	-160	+160		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank active and 1 bank standby.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 2ns.
4. Valid column addresses are A0 through A10.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	—	124	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10K	12	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	14	45	14	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	30	12	35	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	10	—	12	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	50	—	55	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	—	—	—	—	ns	3
t_T	Transition Time (Rise and Fall)	2	30	2	30	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units
		Min	Max	Min	Max	
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns
t_{WCH}	Write Command Hold Time	10	—	12	—	ns
t_{WP}	Write Command Pulse Width	10	—	12	—	ns
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns
t_{DH}	D_{IN} Hold Time	10	—	12	—	ns

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	—	15	—	15	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Hyper Page Mode (Extended Data Out) Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{HCAS}	$\overline{CAS}$ Pulse Width (EDO Mode)	10	10K	12	10K	ns	
t_{HPC}	EDO Mode Cycle Time (Read/Write)	25	—	30	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	15	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	10	—	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2
t_{RASP}	EDO Mode $\overline{RAS}$ Pulse Width	60	125K	70	125K	ns	

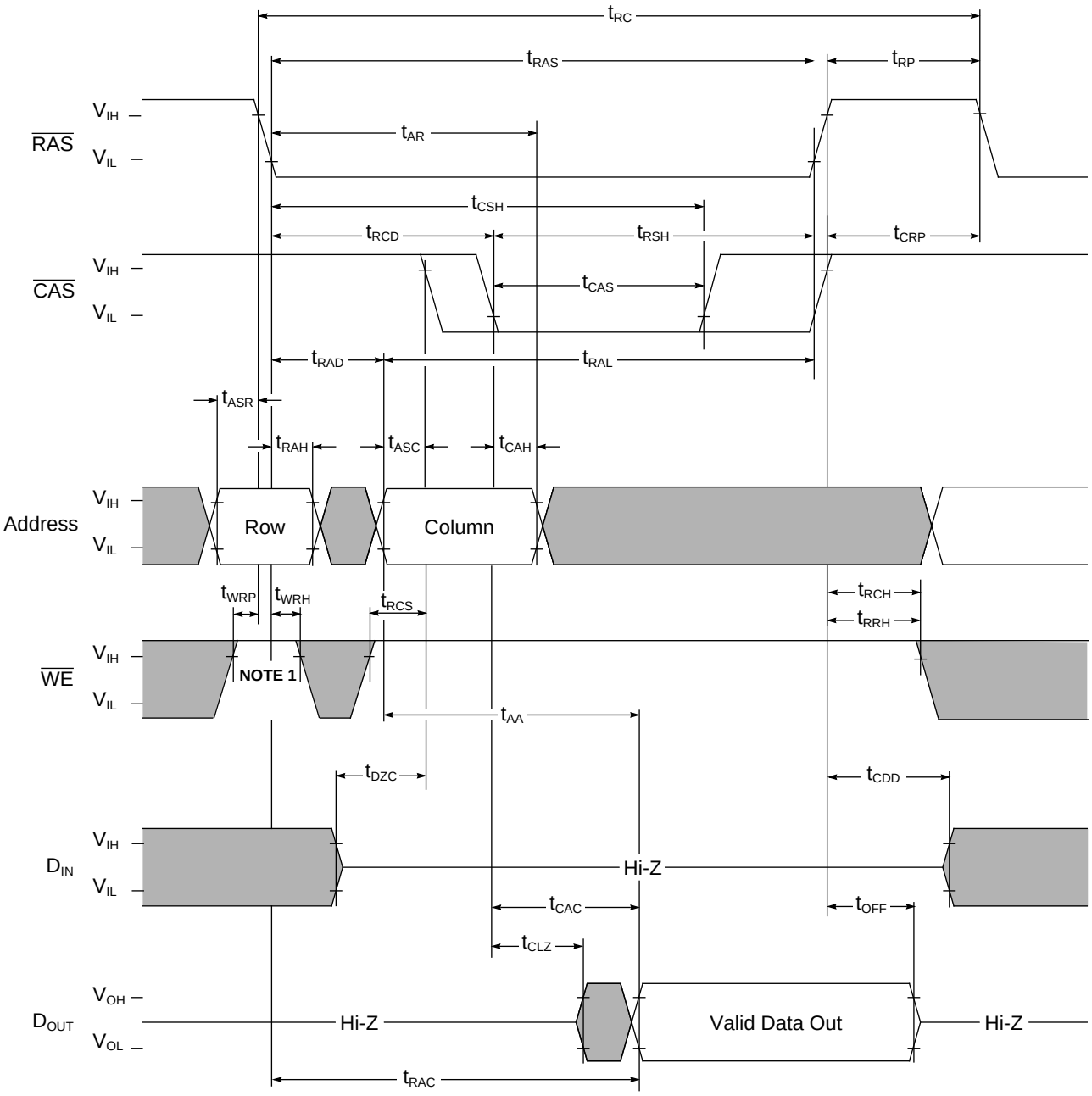
1. Access time assumes a load of 100pF at V_{OL} = 0.8V and V_{OH} = 2V.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.

Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

1. 2048 refreshes are required every 32ms.

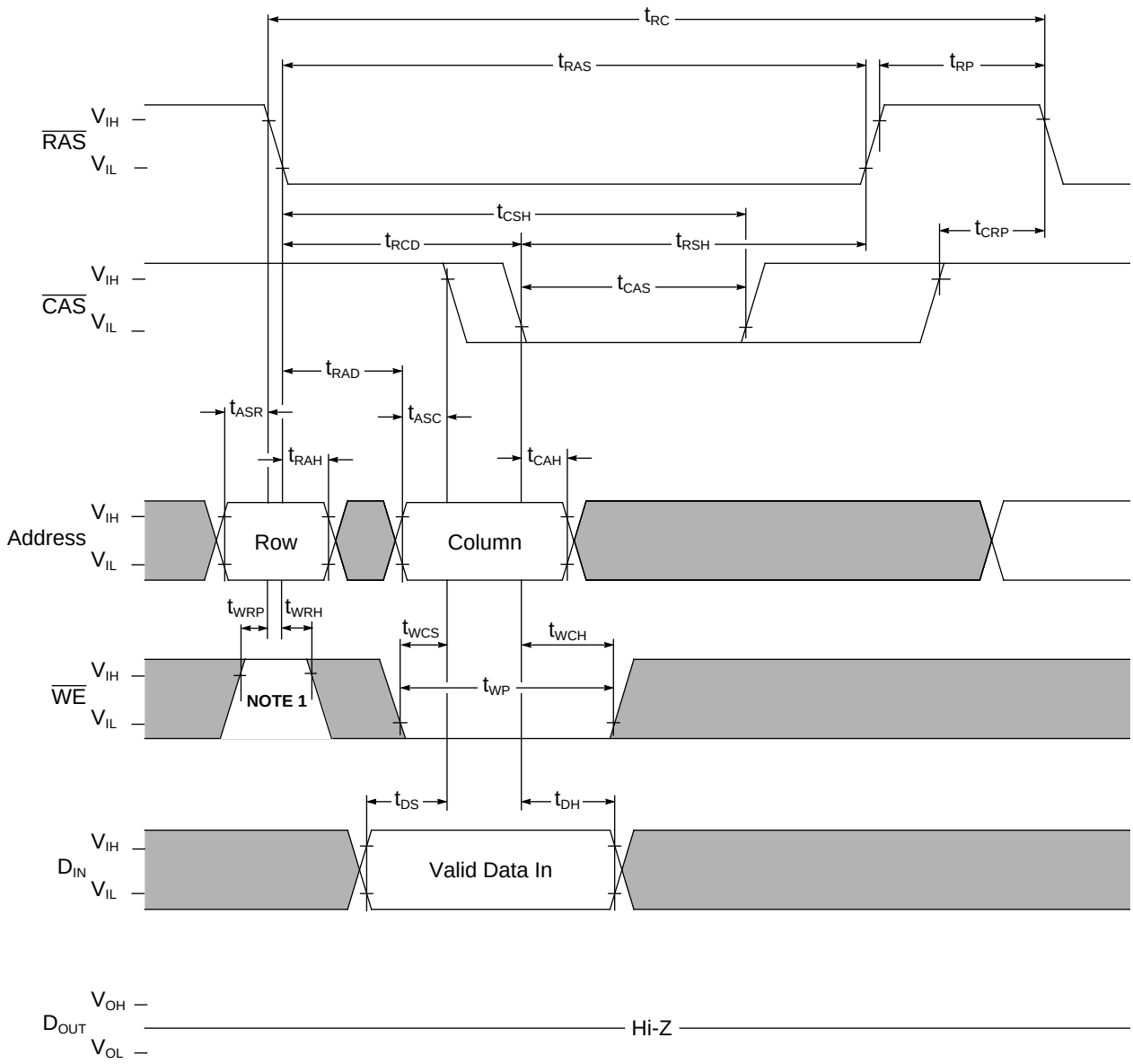
Read Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

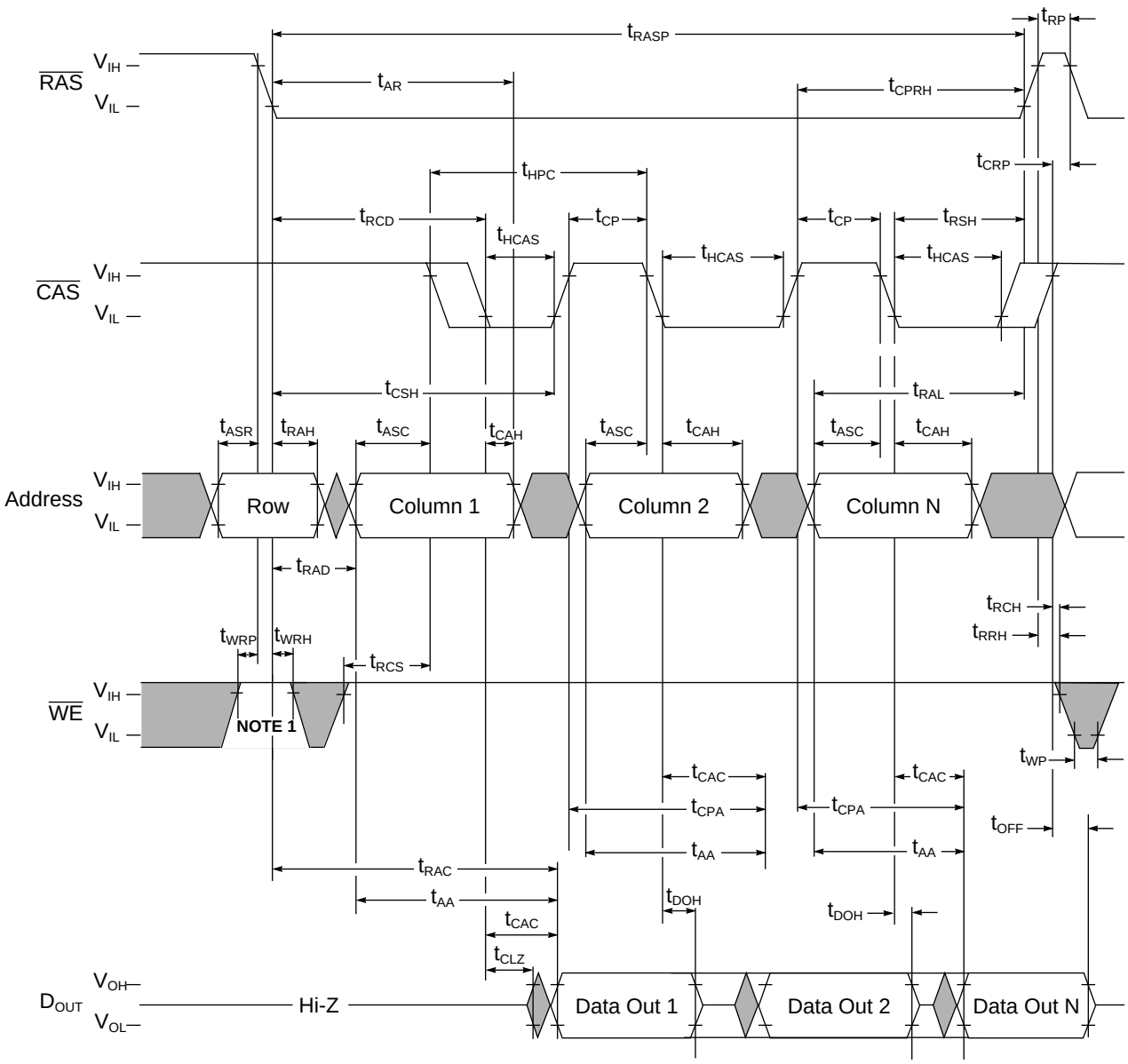
Write Cycle (Early Write)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional Doing so will facilitate compatibility with future EDO DRAMs.

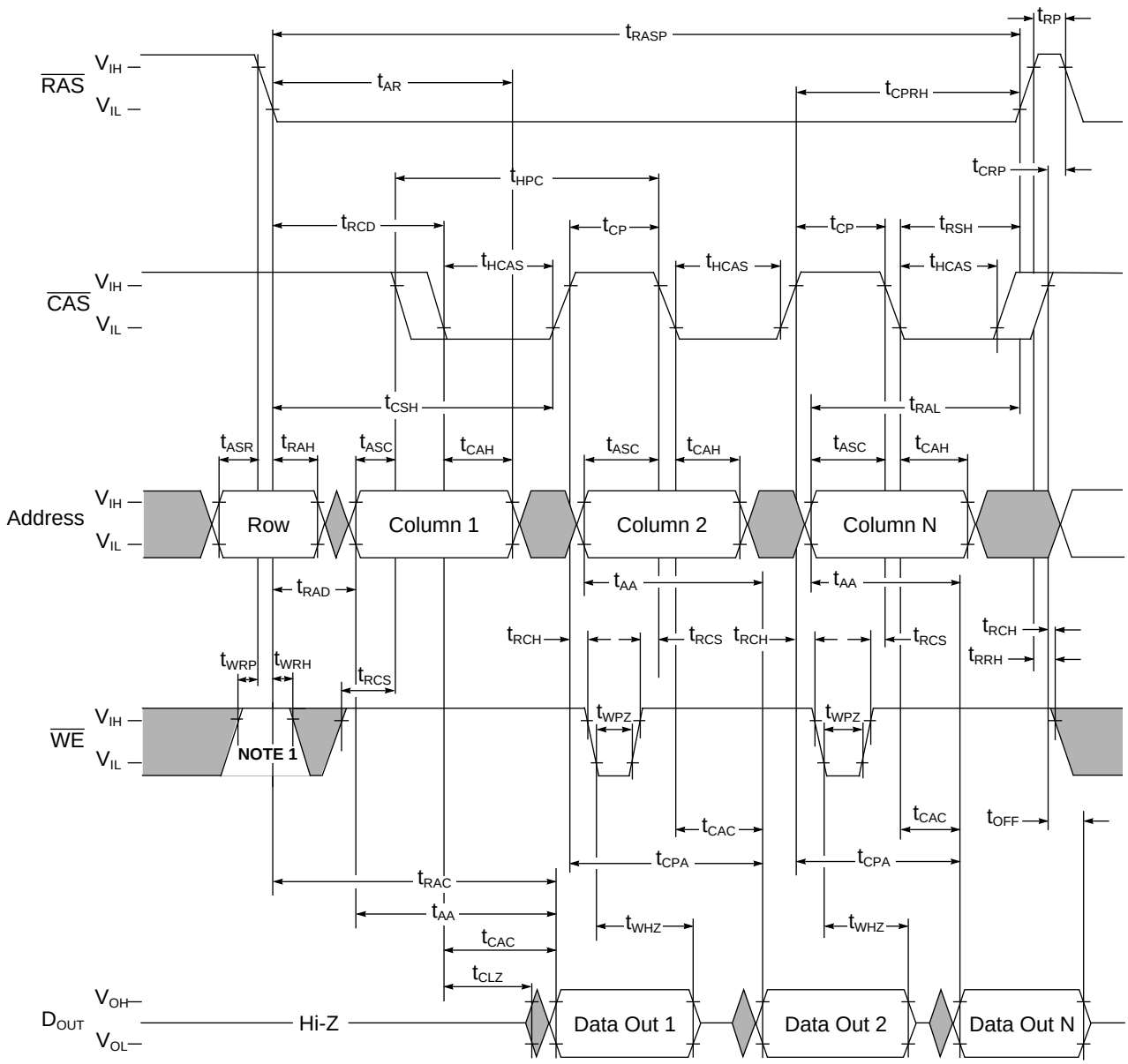
Extended Data Out Mode Read Cycle



: “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

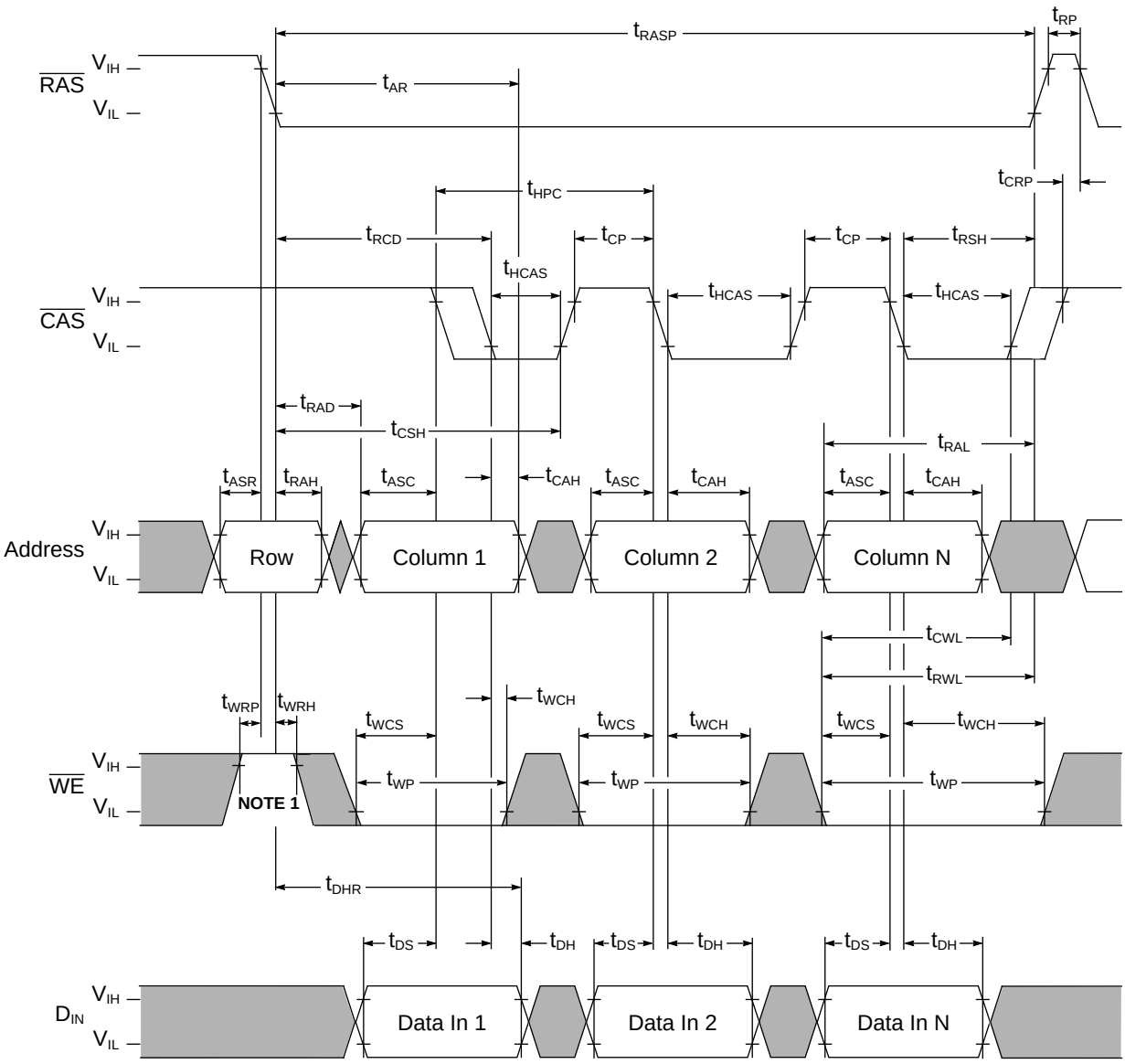
Extended Data Out Mode Read Cycle ($\overline{WE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

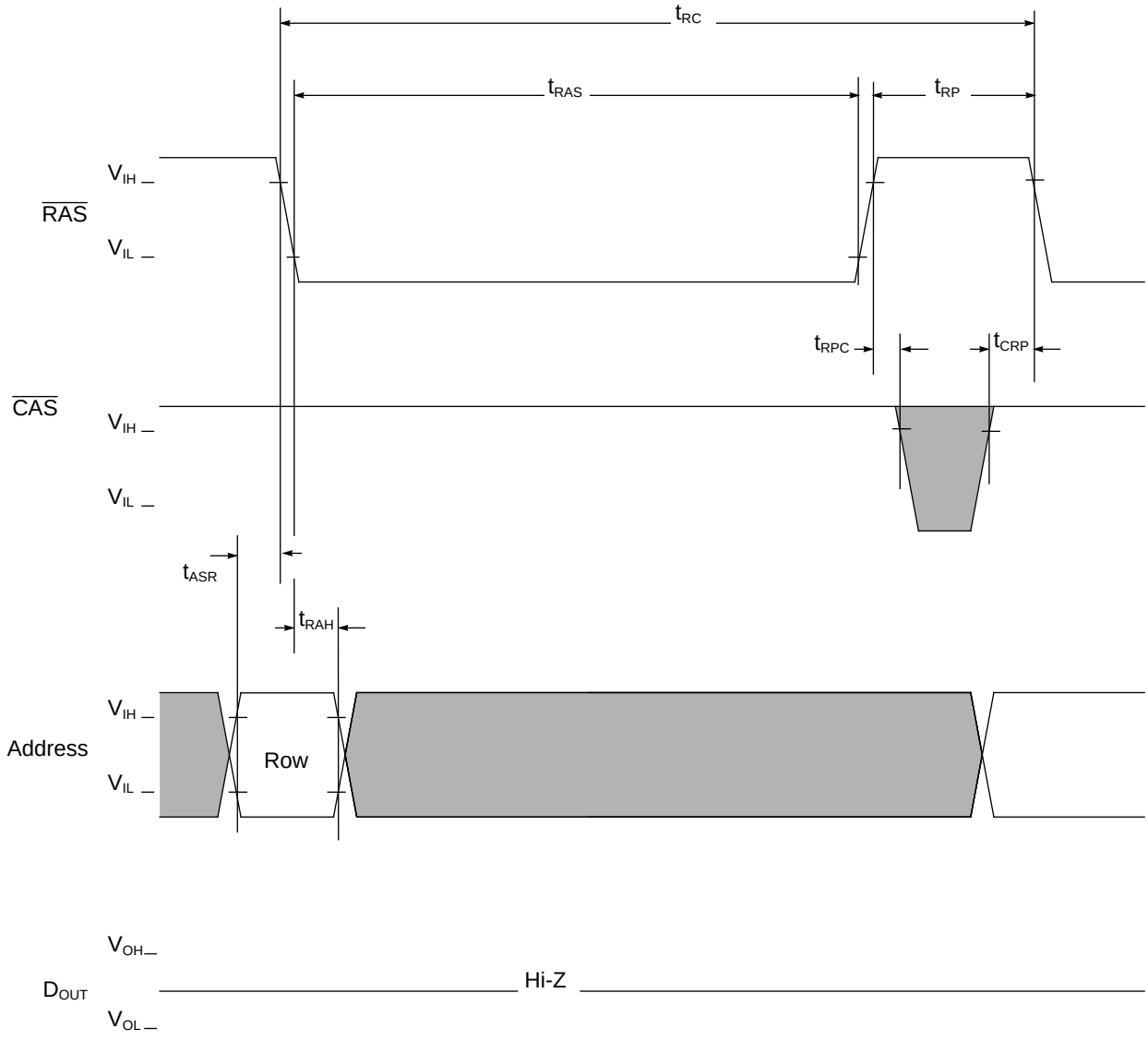
Extended Data Out Mode Early Write Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

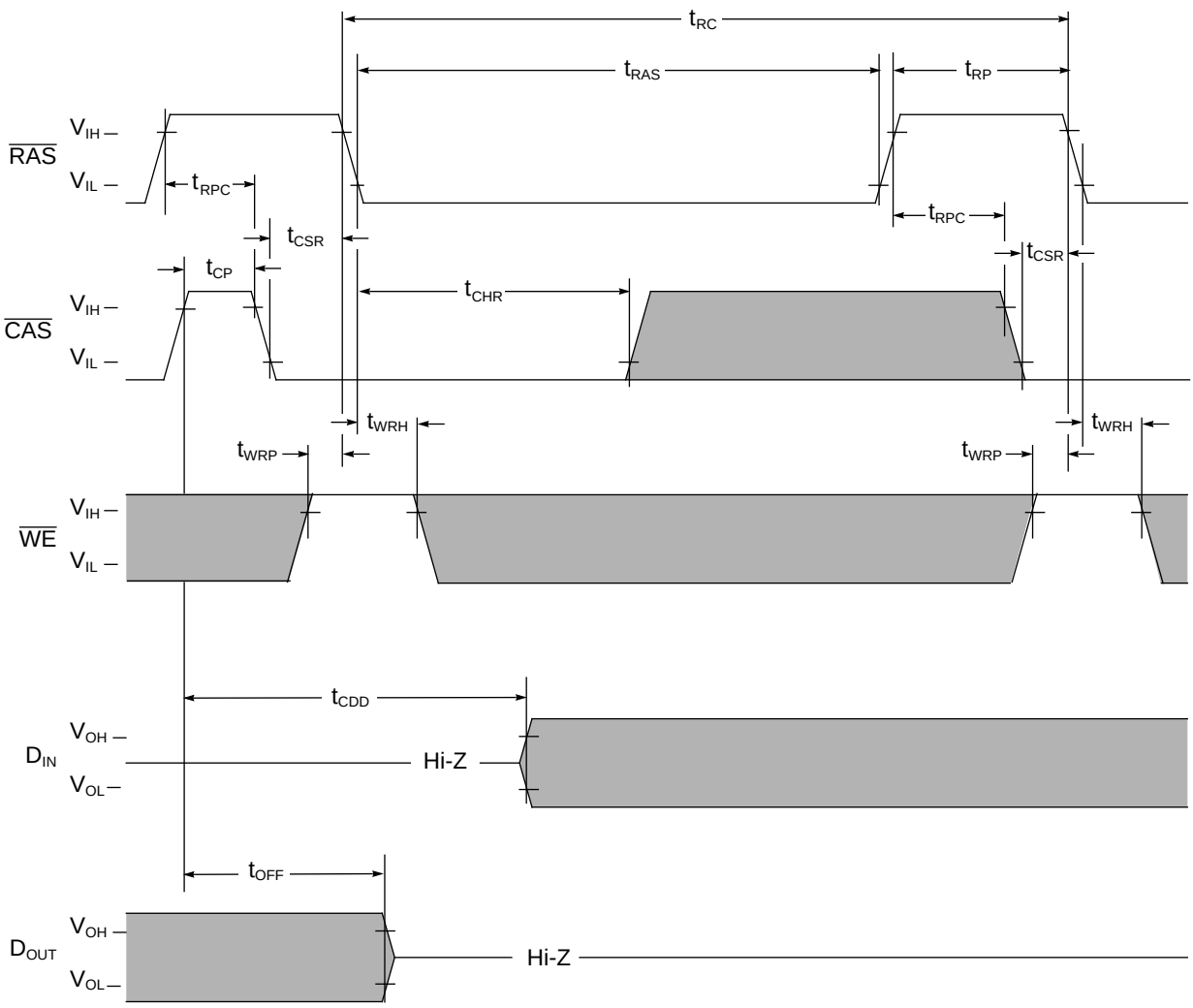
$\overline{RAS}$ Only Refresh Cycle



: “H” or “L”

Note: $\overline{WE}$, D_{IN} are “H” or “L”

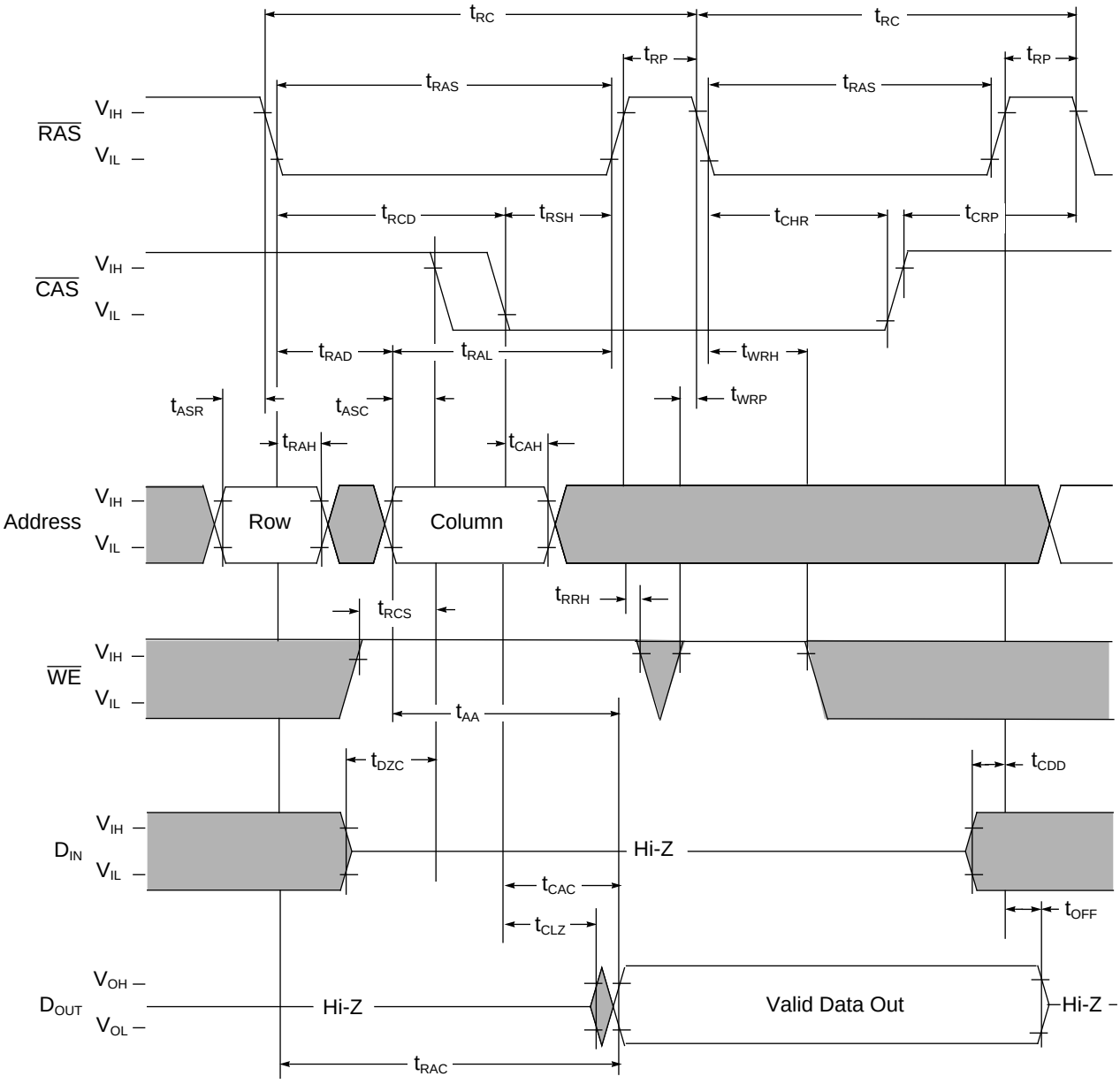
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



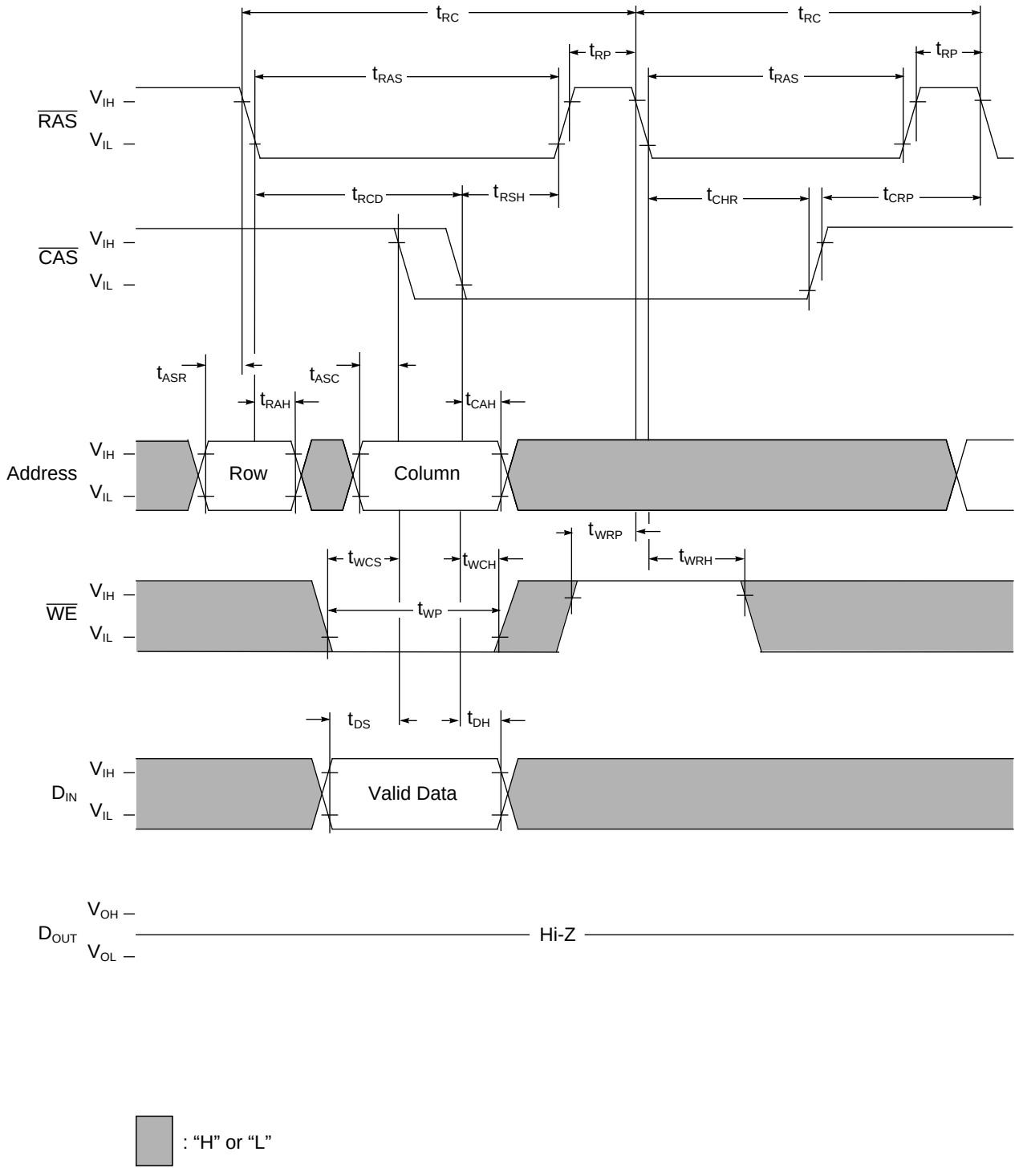
: “H” or “L”

NOTE: Address is “H” or “L”

Hidden Refresh Cycle (Read)

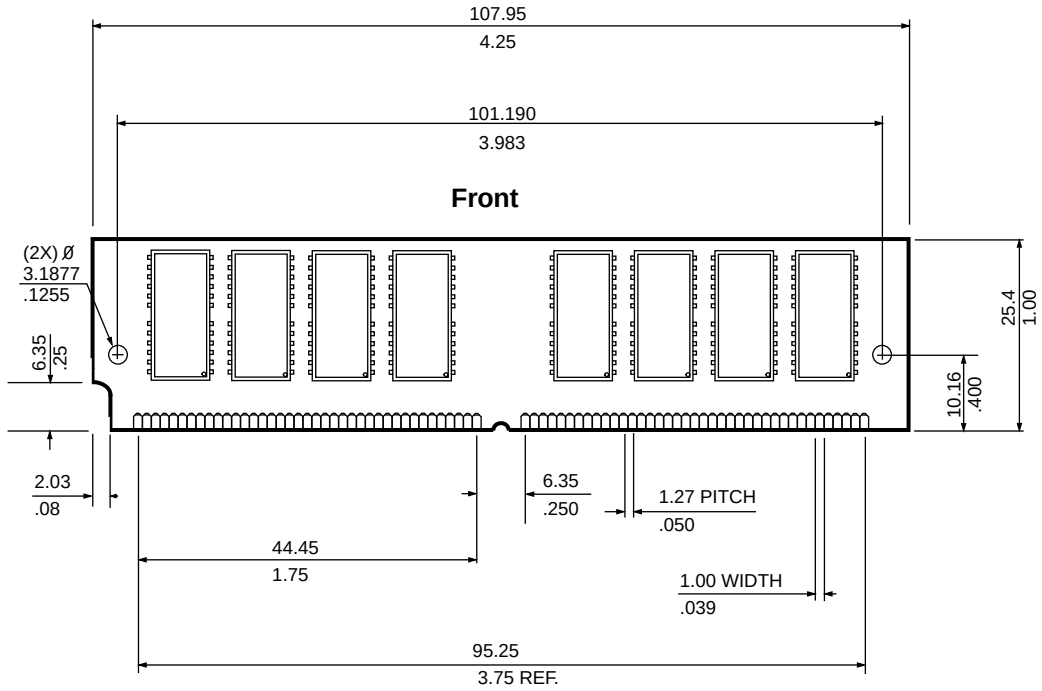


Hidden Refresh Cycle (Write)

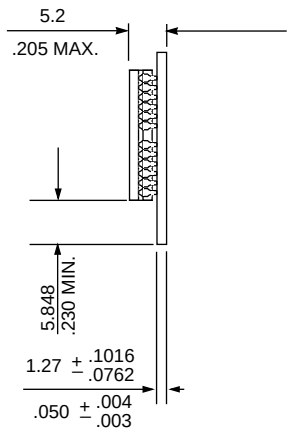


: “H” or “L”

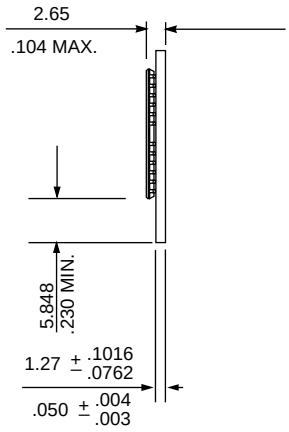
Layout Drawing



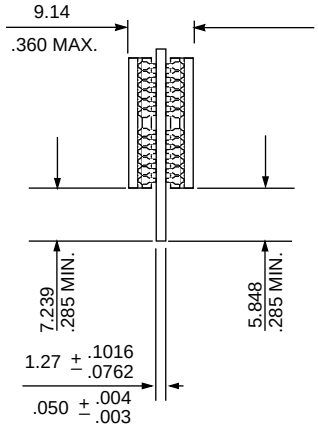
Side (16MB SOJ)



Side (16MB TSOP)



Side (32MB)



NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Revision Log

Rev	Contents of Modification
3/96	Initial release of combined spec for 4M x 32, 8M x 32 Removed Gold-Tab versions CBR timing diagram changed to allow $\overline{CAS}$ to remain low for back-to-back CBR cycles (originally released as spec #'s 26H3207 and 26H3208)
5/96	Added 16Mb TSOP version
8/96	Corrected typo's

Discontinuted (9/98 - last order; 3/99 last ship)

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