HS-7545

12-Bit Buffered Monolithic CMOS MDAC

Features

- 12 bit resolution
- Preadjusted Full Scale: ±1LSB max Gain Error
- Low Gain Tempco: 2ppm/°C
- Fast TTL Data Latches
- Single +5V to 15V Operation
- Small 20-pin 0.3" Wide DIP
- Low Cost

Description

The HS 7545 is a precision, monolithic 12-Bit, CMOS, 4-quadrant multiplying DAC with an on-board latch. The latch is loaded by a single 12-Bit wide word and directly interfaces to most 12-and 16-bit bus systems. Data is loaded into the input latch under the control of $\overline{CS}$ and $\overline{WR}$ inputs. These control inputs are active low. Tying these inputs low makes the input latch transparent allowing direct unbuffered operation of the DAC.

The HS 7545 is offered in a 20-pin plastic or hermetically-sealed CERDIP dual-in-line package. Processing to MIL-STD-883C is available.

Applications

- Digital Gain / Attenuation Control
- Digital Control Of Circuit Functions
- X-Y Graphics
- Robotics
- Digital / Synchro Conversion
- Battery Operated Equipment

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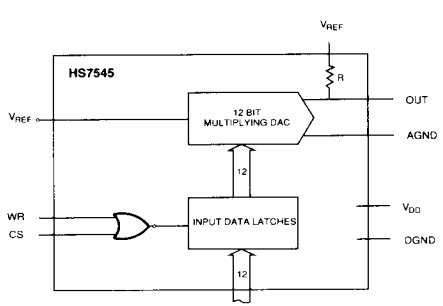
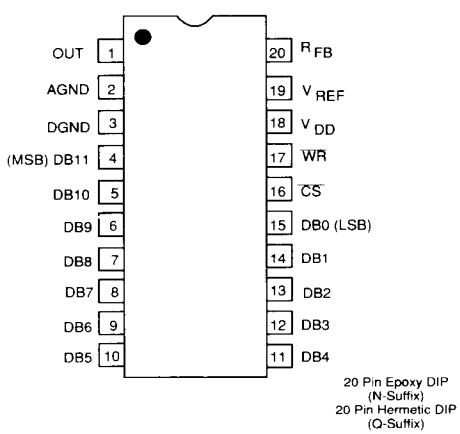
Functional Diagram



Pin Connections



20 Pin Epoxy DIP (N-Suffix)
20 Pin Hermetic DIP (Q-Suffix)

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12-Bit Buffered Monolithic CMOS MDAC

Absolute Maximum Ratings:

(T_A = 25°C unless otherwise noted.)

V_{DD} to DGND	-03V, +17V
Digital Input Voltage to DGND	-0.3V, V_{DD}
AGND to DGND	-0.3V, V_{DD}
V_{RFB}, V_{REF} to DGND	±25V
$V_{PIN}1$ to DGND	-0.3V, V_{DD}
Power Dissipation (Any Package) to +75°C	450mW
Derates Above +75°C by	6mW/°C
Operating Temperature (T_A= Full)	
HS-7545 TQ/GUQ	-55°C to 125°C
HS-7545 BQ/GCQ	-25°C to 85°C
HS-7545 KN/GLN	0°C to 70°
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60sec)	+300°C

Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.

Use proper ESD handling procedures.

Electrical Characteristics:

V_{DD} = +5V or ±15V unless otherwise noted. V_{REF} = +10V, Out = 0V, AGND = DGND = 0V, T_A= Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Static Accuracy						
Resolution	N		12			Bits
Relative Accuracy	INL				±1/2	LSB
Differential Nonlinearity	DNL				±1	LSB
Gain Error	G_{FSE}	Using internal R_{FB} DAC latches =1 1 1 1 1 1 1 1 1 1 1 1 HS-7545 KN/BQ/TQ T_A = 25°C T_A = Full HS-7545 GLN/GCQ/GUQ T_A = 25°C T_A = Full			 3 4 1 2	 LSB LSB LSB LSB
Gain Temperature Coefficient	TCG_{FS}			±2	±5	ppm/°C
Power Supply Rejection (ΔGain/ΔV_{DD})	PSS	T_A = 25°C, ΔV_{DD} = ±5% T_A = Full, ΔV_{DD} = ±5%			0.002 0.004	%/% %/%
Output Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V All digital inputs = 0V HS-7545 KN/BQ/GLN/GCQ T_A = 25°C T_A = Full HS-7545 TQ/GUQ T_A = 25°C T_A = Full			 10 50 10 200	 nA nA nA nA

Electrical Characteristics:

V_{DD} = +5V or ±15V unless otherwise noted. V_{REF} = +10V, Out = 0V, AGND = DGND = 0V, T_A = Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Dynamic Performance Propagation Delay	t_{PD}	From digital input change to 90% of final analog output, I_{OUT} Load = 100Ω, C_{EXT} = 13pF T_A = 25°C			300	nS
Current Settling Time	t_S	to 1/2 LSB I_{OUT} LOAD = 100Ω			1	µS
Digital Charge Injection	Q	V_{REF} = AGND ; T_A = 25°C V_{REF} = AGND ; T_A = Full			300 400	nVS nVS
A.C Feedthrough (V_{REF} to I_{OUT})	FT	V_{REF} = ±10V @ f = 10kHz All digital inputs = 0V		5		mV_{P-P}
Reference Input Input Resistance	R_{REF}		7	11	15	kΩ
Analog Outputs Output Capacitance	C_{OUT}	DB0-DB11= 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB11 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V			70 150	pF pF
Digital Inputs Input High Voltage	V_{INH}	V_{DD} = +5V V_{DD} = +15V	2.4 13.5			V V
Input Low Voltage	V_{INL}	V_{DD} = +5V V_{DD} = +15V			0.8 1.5	V V
Input Current	I_{IN}	T_A = 25°C T_A = Full			1 10	µA µA
Input Capacitance (DB0-DB11, $\overline{WR}$, $\overline{CS}$)	C_{IN}	V_{IN} = 0V			8	pF
Switching Characteristics		($t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$)				
Chip Select to Write Set-up Time	t_{CS}	V_{DD} = +5V, T_A = 25°C V_{DD} = +5V, T_A = Full V_{DD} = +15V, T_A = 25°C V_{DD} = +15V, T_A = Full	280 380 180 200	200 270 120 150		nS nS nS nS
Chip Select to Write Hold Time	t_{Ch}		0			nS
Write Pulse Width	t_{WR}	V_{DD} = +5V, T_A = 25°C V_{DD} = +5V, T_A = Full V_{DD} = +15V, T_A = 25°C V_{DD} = +15V, T_A = Full	250 380 160 240	175 270 100 170		nS nS nS nS
Data Set-up Time	t_{DS}	V_{DD} = +5V, T_A = 25°C V_{DD} = +5V, T_A = Full V_{DD} = +5V, T_A = 25°C V_{DD} = +15V, T_A = 25°C	140 210 90 120	100 150 60 80		nS nS nS nS
Data Hold Time	t_{DH}		10			nS

Electrical Characteristics:

V_{DD} = +5V or ±15V unless otherwise noted. V_{REF} = +10V, Out = 0V, AGND = DGND = 0V, T_A= Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Current	I_{DD}	All digital inputs = V_{INL} or V_{INH}			2	mA
		All digital inputs = 0V or V_{DD}				
		T_A = 25°C		2	100	µA
		T_A = Full		5	100	µA

Circuit Operation

General

Figure 1 shows a simplified circuit of the D/A Converter section and Figure 2 gives an approximate equivalent switch circuit. R is typically 11kΩ.

The binary-weighted currents are switched between OUT and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT terminal, C_{OUT}, is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT).

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

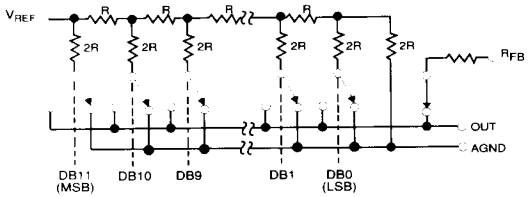

FIGURE 1: Simplified Schematic Of The HS7545

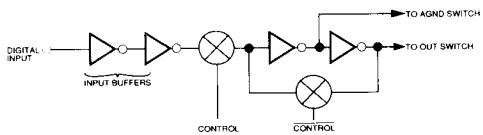

FIGURE 2: Digital Input Structure Of The HS7545

Digital Section

Figure 2 shows the digital structure for one bit. The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed such that when the PM-7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0 volts to 6.0 volts, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible. The PM-7545 may be operated with any supply voltage in the ranage 5 ≤ V_{DD} ≤ 15 volts. With V_{DD} = +15V, the input logic lievels are CMOS compatible only, i.e., 1.5V and 13.5V.

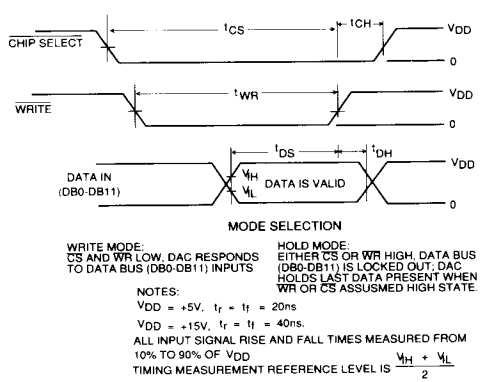

FIGURE 3: Write Cycle Timing Diagram

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Parameter Definitions

Relative Accuracy

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

Differential Nonlinearity

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ±1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will increase for an increase in digital code applied).

Gain Error

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

Output Capacitance

The capacitance from OUT to AGND.

Propagation Delay

This is measured from the digital input change to the analog output current reaching 90% of its final value. It is a measure of the DAC's internal circuitry

Digital Charge Injection

This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with V_{REF} = AGND.

Applications

Unipolar Operation

Figure 4 shows a simple unipolar circuit. Resistor R_1 is used to trim for full scale. The HS 7545 GLN, HS 7545 GCQ and HS 7545 GUD have a guaranteed maximum gain error of ±1 LSB at 25°C and V_{DD} = +5V, and in many applications the gain trim resistors are not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuit of Figure 4 has constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to-V_{IN} (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \le V_{IN} \le +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table1 shows the code relationship for the circuit of Figure 4.

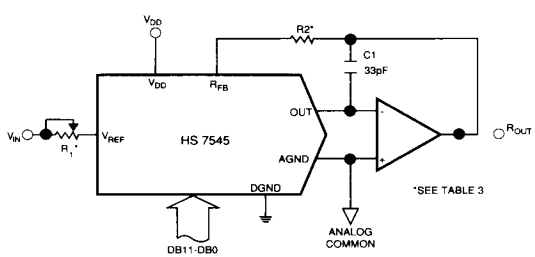

FIGURE 4: Unipolar Circuit Operation

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

TABLE 1: Unipolar Operation
Binary Code Table

Bipolar Operation (2's Complement Code)

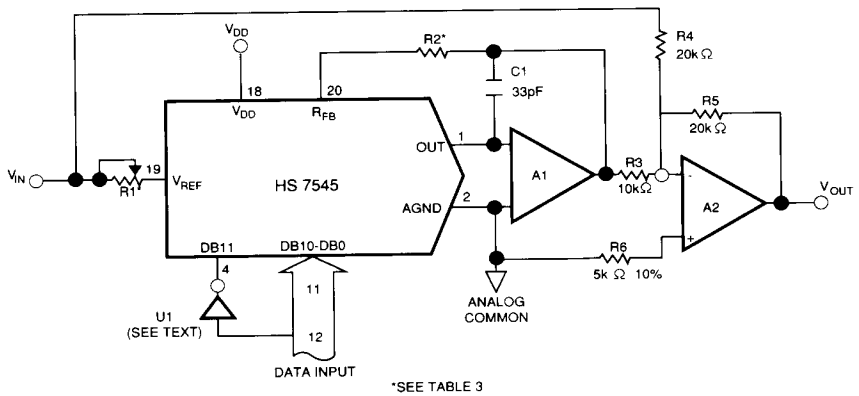

FIGURE 5: Bipolar Circuit Operation

Figure 5 shows a simple bipolar circuit configuration. Resistor R_1 is used to trim for full scale. The HS-7545 GLN, HS-7545 GCQ and HS-7545 GUD have a guaranteed maximum gain error of ±1 LSB at +25°C and V_{DD} = +5V, and in many applications, the gain trim resistors are not required. Capacitor C_1 provides phase compensation and helps prevent overshoot and ringing when using high speed op-amps. The circuit of Figure 5 has constant input impedance at the V_{REF} terminal.

Figure 5 and Table 2 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter U_1 on the MSB line, converts 2's-complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
0111	1111	1111	$+V_{IN}\left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN}\left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN}\left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{2048}\right\}$

TABLE 2: Bipolar Operation Code Table (2's Complement Code)

Trim Resistor Values

Table 3 shows the recommended trim resistor values for R_1 and R_2 in the circuits of Figure 4 & 5.

Trim Resitor	HS-7545 KN/BQ/TQ	HS-7545 GLN/GCQ/GUQ
R_1	100Ω	20Ω
R_2	33Ω	6.8Ω

Table 3: Recommended Trim Resistor Value

Ordering Information

PART #	PACKAGE	TEMP RANGE (°C)	RELATIVE ACCURACY	GAIN ERROR
HS 7545 KN	20 Pin Epoxy Dip	0 to 70	± 1/2 LSB	± 3 LSB
HS 7545 GLN	20 Pin Epoxy Dip	0 to 70	± 1/2 LSB	± 1 LSB
HS 7528 BQ	20 Pin Hermetic CERDIP	-25 to 85	± 1/2 LSB	± 3 LSB
HS 7545 GCQ	20 Pin Hermetic CERDIP	-25 to 85	± 1/2 LSB	± 1 LSB
HS 7528 TQ	20 Pin Hermetic CERDIP	-55 to 125	± 1/2 LSB	± 3 LSB
HS 7545 GUQ	20 Pin Hermetic CERDIP	-55 to 125	± 1/2 LSB	± 1 LSB

• For devices processed in total compliance with MIL-STD-883, add /883 after the part number. Consult factory for 883 data sheet.

• Package Designations: Suffix N Plastic DIP, Suffix Q Hermetic DIP. For package mechanical dimensions, call DataLinear at (408) 945-9080.

CROSS REFERENCE INFORMATION

ADI Part No.	DataLinear Part No.
AD 7545 JN	HS 7545 KN
AD 7545 KN	HS 7545 KN
AD 7545 LN	HS 7545 GLN
AD 7545 GLN	HS 7545 GLN
AD 7545 AQ	HS 7545 BQ
AD 7545 BQ	HS 7545 BQ
AD 7545 CQ	HS 7545 GCQ
AD 7545 GCQ	HS 7545 GCQ
AD 7545 SD	HS 7545 TQ
AD 7545 TD	HS 7545 TQ
AD 7545 UD	HS 7545 GUD
AD 7545 GUD	HS 7545 GUD