ANALOG DEVICES

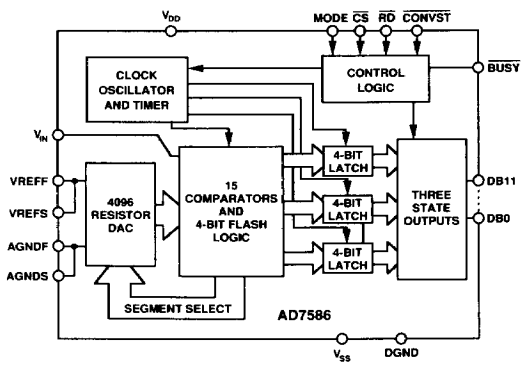
LC²MOS 12-Bit 1 μs ADC

AD7586

FEATURES
1 μs Conversion Time
AGND and VREF Force/Sense Connections
12-Bit Monotonic over Temperature
Low Power – 200 mW typ
Fast Bus Access Time – <57 ns

APPLICATIONS
Measurement and Control
Automatic Test Equipment
Precision Servo Control
All Data Acquisition Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7586 is a very fast 12-bit ADC that operates from ±5 V power supplies, offering high-speed performance combined with low power dissipation. The AD7586 is a triple-pass flash ADC, which uses 15 comparators in a 4-bit flash technique to achieve 12-bit accuracy in 1 μs conversion time. Each of the 4096 quantization voltage levels are realized internally with a precision resistor DAC. The use of thin-film resistor technology and on-chip force and sense amplifiers ensure 12-bit performance.

The AD7586 has a facility to force/sense the AGND and VREF inputs minimizing offset and gain errors. The precision resistor DAC with its excellent temperature drift characteristics combined with 12-bit accurate comparators provide 12-bit linearity over the entire temperature range.

The AD7586 has a high-speed digital interface with three-state data outputs. Data access and conversion start functions are controlled by $\overline{CS}$ and $\overline{RD}$ inputs, standard microprocessor signals. Conversion control can also be provided by a $\overline{CONVST}$ input for DSP applications. The data access time of less than 57 ns means that the AD7586 can interface directly to most modern microprocessors including DSP processors.

The AD7586 is fabricated in Analog Devices' Linear Compatible CMOS process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic.

PRODUCT HIGHLIGHTS

1. Fast 1 μs Conversion Time.
   Fast 1 μs conversion time makes the AD7586 suitable for a wide range of data acquisition applications.
2. Fast Microprocessor Interface.
   Standard control signals, $\overline{CS}$ and $\overline{RD}$, and fast bus access times make the AD7586 easy to interface to microprocessors
3. Low Power.
   LC²MOS fabrication process gives low power dissipation of 200 mW typically.

AD7586—SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGNDF & AGNDS are Kelvin connected to 0 V, VREFF & VREFS are Kelvin connected to −4 V, DGND = 0 V. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A, S Versions[1]	K, B Versions[1]	Units	Test Conditions/Comments
ACCURACY				
Resolution	12	12	Bits	
Integral Linearity @ +25°C	±2	±1.5	LSB max	
T_{min} to T_{max}	±2	±1.5	LSB max	
Differential Nonlinearity	±1	±1	LSB max	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	Bits	
Offset Error[2] @ +25°C	±2	±2	LSB max	Kelvin Connections Reduce Offset Error
T_{min} to T_{max}	±2	±2	LSB max	by 2 LSBs Typically
Gain Error[2] @ +25°C	±2	±2	LSB max	Kelvin Connections Reduce Gain Error
T_{min} to T_{max}	±2	±2	LSB max	by 2 LSBs Typically
ANALOG INPUT				
Input Voltage Range	0 to −4	0 to −4	Volts	
Input Current	−20	−20	μA max	V_{IN} = 0 to −4 V
REFERENCE INPUT				
VREFS (For Specified Performance)	−4	−4	Volts	±2%
Input Reference Current	−10	−10	mA max	
POWER SUPPLY REJECTION				
V_{DD} Only, (FS Change)	0.1	0.1	LSB typ	V_{SS} = −5 V, V_{DD} = +4.75 V to +5.25 V
V_{SS} Only, (FS Change)	0.1	0.1	LSB typ	V_{DD} = 5 V, V_{SS} = −4.75 V to −5.25 V
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$				
Output High Voltage, V_{OH}	4	4	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
Floating-State Leakage Current	±10	±10	μA max	
Floating-State Output Capacitance[3]	15	15	pF max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	30	30	mA max	Typically 20 mA, $\overline{CS}$ = $\overline{RD}$ = V_{DD}
I_{SS}	−30	−30	mA max	Typically 20 mA, $\overline{CS}$ = $\overline{RD}$ = V_{DD}
Power Dissipation	200	200	mW typ	$\overline{CS}$ = $\overline{RD}$ = 5 V
	300	300	mW max	

NOTES
[1]Temperature Ranges are as follows: J/K versions 0 to +70°C; A/B versions −40°C to +85°C; S version −55°C to +125°C.
[2]Without Kelvin connections on VREF and AGND the Offset and Gain Errors are typically 4 LSBs.
[3]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (J, K Versions)	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	35	35	40	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay (C_L = 10 pF)
t_3	20	20	14	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 20 pF)
	10	10	0	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 100 pF)
t_4[2]	**10**	**10**	**10**	ns min	Bus Relinquish Time after $\overline{RD}$
	55	**55**	**65**	ns max	
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6	35	35	40	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Propagation Delay
t_7	75	75	90	ns min	$\overline{CONVST}$ Pulse Width
t_8[3]	**57**	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_9	**60**	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{BUSY}$ High to $\overline{RD}$ Low, (Mode 1)
t_{11}	25	25	25	ns min	$\overline{CS}$ High Time, (Mode 0)
t_{12}	0	0	0	ns min	$\overline{CS}$ High to $\overline{CONVST}$ Low, (Mode 1)
t_{13}	0	0	0	ns min	$\overline{BUSY}$ High to $\overline{CONVST}$ Low, (Mode 1)
t_{CONV}	950	950	950	ns typ	Conversion Time (Mode 0)
	1000	**1000**	**1000**	ns max	

NOTES

[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_4 is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_4, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

[3]t_8 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND[2] . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
VREFF, VREFS to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND
$\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$, Mode . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
DB0 to DB11, $\overline{BUSY}$ . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]If V_{SS} is open circuited with V_{DD} and AGND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to DGND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

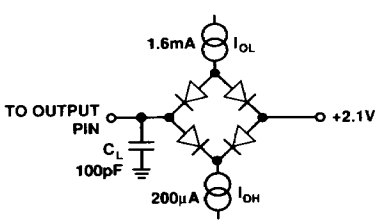


Figure 1. Load Circuit for Access and Relinquish Time

CAUTION

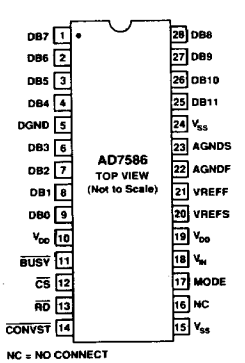
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN FUNCTION DESCRIPTION

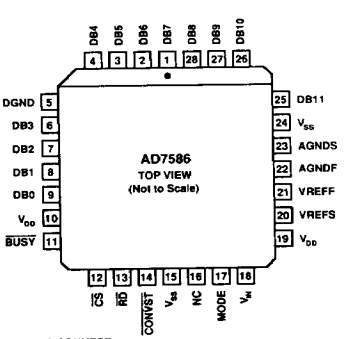
Pin Number	Mnemonic	Description
POWER SUPPLY		
10 & 19	V_{DD}	Positive Power Supply, +5 V ±5%. Both V_{DD} pins must be tied together.
15 & 24	V_{SS}	Negative Power Supply, −5 V ±5%. Both V_{SS} pins must be tied together.
22	AGNDF	Analog Ground Force. The input can be used in conjunction with AGNDS to force/sense the external AGND (See Figure 3). Force/sensing the AGND minimizes offset error. In applications where offset error is not important these inputs can be tied together and connected directly to the external AGND reference.
23	AGNDS	Analog Ground Sense. This is the complementary input for AGNDF (above) to force/sense the analog ground reference. AGNDF and AGNDS are tied together internally.
5	DGND	Digital Ground.
ANALOG AND REFERENCE INPUTS		
18	V_{IN}	Analog Input. The analog input range is 0 to −4 V.
20	VREFS	Voltage Reference Sense Input. The input can be used in conjunction with VREFF to force/sense an external voltage reference (See Figure 3). Force/sensing the VREF input minimizes gain error. In applications where gain error is not important these inputs can be tied together and connected directly to an external reference.
21	VREFF	Voltage Reference Force Input. This is the complementary input for VREFS (above) to force/sense an external voltage reference. VREFF and VREFS are tied together internally.
INTERFACE		
1–4, 6–9	DB7–DB4, DB3–B0	Three-state data outputs. These outputs are controlled by $\overline{CS}$ and $\overline{RD}$. DB11 is the most significant bit, (MSB).
25–28	DB11–DB8	
11	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is low during conversion.
12	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
13	$\overline{RD}$	Read Input. This active low signal, in conjunction with $\overline{CS}$ is used to enable the output data three-state drivers and initiate a conversion when the MODE input pin is tied low.
CONTROL		
14	$\overline{CONVST}$	Conversion Start Input. This input may be used to start conversion when the MODE input pin is tied high.
17	MODE	Mode Input. When this pin is low, conversion is initiated on the falling edge of $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ must remain low for the duration of the conversion. When this pin is high conversion is initiated by a rising edge on the $\overline{CONVST}$ input.
16	NC	No Connect pin. This pin has no internal connections.

PIN CONFIGURATIONS

DIP



PLCC



ORDERING GUIDE

Model[1]	Temperature Range	Integral Nonlinearity	Package Option[2]
AD7586JN	0°C to +70°C	±2.0 LSB	N-28
AD7586KN	0°C to +70°C	±1.5 LSB	N-28
AD7586JP	0°C to+70°C	±2.0 LSB	P-28A
AD7586KP	0°C to+70°C	±1.5 LSB	P-28A
AD7586AQ[3]	−40°C to +85°C	±2.0 LSB	Q-28
AD7586BQ[3]	−40°C to +85°C	±1.5 LSB	Q-28
AD7586SQ[3]	−55°C to +125°C	±2.0 LSB	Q-28

NOTES
[1]Analog Devices reserves the right to ship J-Leaded Ceramic Chip Carrier packages in lieu of PLCC packages.
[2]J = J-Leaded Ceramic; N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.
[3]Contact your local sales office for availability.

OPERATIONAL DIAGRAM

An operational diagram for the AD7586 is shown in Figure 2. The only external component required for basic operation of the part is a −4 V reference.

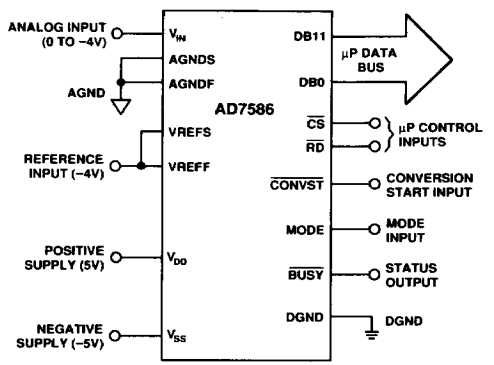


Figure 2. Operational Diagram

CONVERTER DETAILS

The AD7586 is a triple-pass flash ADC which uses 15 comparators in a 4-bit flash technique to perform the 12-bit conversion procedure. Each of the 4096 quantization levels is realized internally with a precision resistor DAC.

The fifteen comparators first compare the analog input voltage to the VREF/16 voltages of the resistor array. This determines the four most significant bits and selects 1 out of 16 voltage segments. The comparators are then switched to 15 subvoltages on that segment to determine the next four bits and select 1 out of 256 voltage segments. A further switching of the comparators to another 15 subvoltages produces the complete 12-bit conversion result. The 12 bits of data are then stored internally in a three-state output latch.

FORCE/SENSE CONNECTIONS

The AD7586 has a facility for Kelvin (force/sense) connections on the AGND and VREF pins to minimize offset and gain errors. Force/sensing these inputs eliminates error contributions from voltage or IR drops due to resistances from nonideal, internal conductors. IR drops in the AGND path cause an offset error while IR drops in the reference path cause a gain error. Typically, the use of Kelvin connections reduces the offset and gain errors by 2 LSBs.

A low op amp offset voltage is important as any offset voltage will add directly to the voltage that is being forced/sensed. Suitable op amps for this application are precision op amps such as the AD705, AD707 or the AD708 (dual op amp), all of which feature offset voltages of less than 100 μV.

REFERENCE INPUT

The AD7586 operates from a −4 V external reference. Figure 3 shows a typical reference connection circuit based on the AD586. The AD586 is a high performance voltage reference which exhibits excellent stability performance, 5 ppm/°C max. The AD586's +5 V output is scaled and inverted before being applied to the AD7586 VREF inputs. Proper decoupling on the force/sense op amp outputs is important to suppress high speed transients during the conversion procedure. Note, connecting capacitors directly to op amp outputs can cause stability problems. However, the use of large capacitors, 10 μF in Figure 3, limits the open-loop bandwidth preventing any closed-loop oscillations.

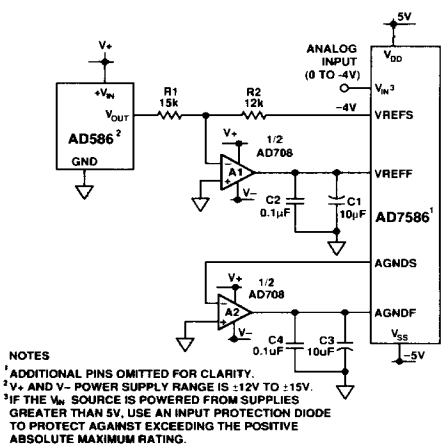


Figure 3. Typical Application Circuit Using the AD586, AGND and VREF Are Force/Sensed

Where offset and gain errors are not important, the force/sense op amps can be omitted and the force/sense pins can be tied together as shown for the AGND connection in Figure 4. However the reference circuitry will invariably use an external op amp to scale the reference input voltage to −4 V, this op amp can provide the second function of force/sensing at no extra cost. In all applications, both the AGND and the VREF pins must be driven from low impedance sources.

The AD586 is a precision voltage reference used for applications throughout this data sheet. However, other references exist which may be preferable in some applications. One example is the ZNREF040, 4 V reference, available from Plessey Semiconductor. This part is not as suitable for precision applications, its temperature drift specification is 50 ppm/°C. It does have the advantage of a smaller package size, 3-pin metal can.

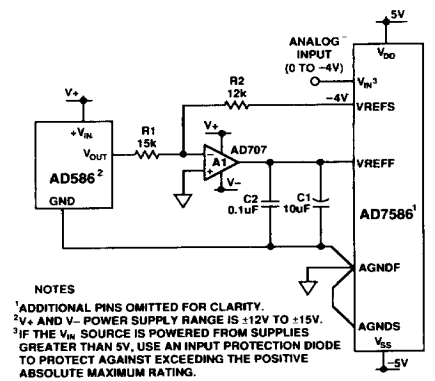


Figure 4. Typical Application Circuit Using the AD586, VREF is Force/Sensed

UNIPOLAR OPERATION

The analog input range of the AD7586 is 0 to −4 V. The designed code transitions occur on integer multiples of 1 LSB. The output code is natural binary with 1 LSB = FS/4096 = (4 V/4096) = 0.977 mV, see Figure 5.

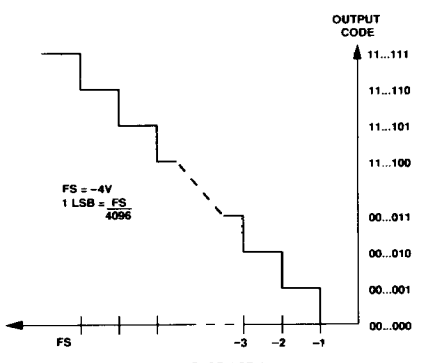


Figure 5. AD7586 Transfer Function

UNIPOLAR OFFSET AND GAIN ERROR ADJUST

Both offset and gain errors are less than 2 LSBs, when force/sense amplifiers are used for the reference and AGND pins, eliminating the need for calibrating the AD7586 in the majority of cases. However, applications requiring absolute accuracy may use the force/sense amplifiers to null any system offset or gain errors caused by signal conditioning or other external circuitry.

The overall transfer function can be calibrated as a "mid riser" type or a "mid tread" type. A mid riser type is where the code transitions occur on successive integer LSB values, the mid tread type is where the code transitions occur mid way between successive integer LSB values. The only difference between the two types is a 1/2 LSB offset, the first and last code transition voltages are shown below in Table I.

	Mid Tread	Mid Riser
First Code Transition Voltage (0000 0000 0000 to 0000 0000 0001)	−0.488 mV	−0.977 mV
Last Code Transition Voltage (1111 1111 1110 to 1111 1111 1111)	−3.9985 V	−3.9990 V

Table I. Ideal First and Last Transition Voltages for Unipolar Operation

Figure 6 shows a circuit which is suitable for offset and gain error adjustment. The AD708 dual op amp is used to force/sense the AGND and VREF pins, the voltages at the force/sense op amp outputs can be varied with trim potentiometers R3 and R6. The order of adjustment does not matter; in other words, adjusting offset does not affect gain error or vice versa.

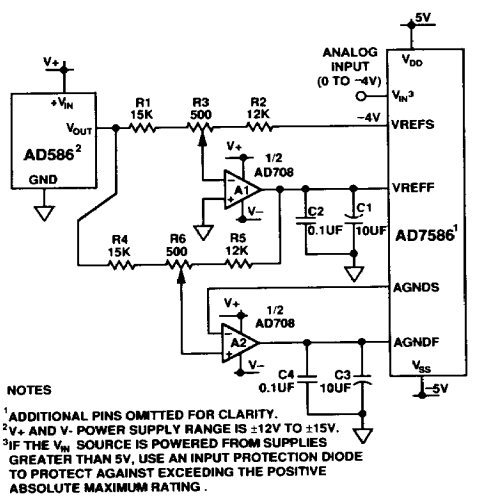


Figure 6. Unipolar Operation with Full-Scale Adjustment

Offset adjustment is achieved by adjusting the AGND force/sense voltage. To adjust the offset apply the first code transition voltage to V_{IN} (see Table I) and adjust R6 until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

Gain error can be nulled by adjusting the reference input which in turn adjusts the full-scale digital output. To adjust the full-scale output apply the last code transition voltage at V_{IN} and vary R3 until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

BIPOLAR OPERATION

Figure 7 shows how bipolar operation can be achieved with the AD7586. The circuit uses an op amp to offset the analog signal by −2 V before being applied to the AD7586 analog input. The circuit has an analog input range of ±2 V with an LSB size of 0.997 mV. The output code is offset binary, see Figure 8 for the transfer function.

Signal ranges other than ±2 V are easily accommodated by using a different value of R3. For example, setting R3 equal to 30 k increases the analog input range to ±5 V. R3 should always be chosen such that the voltage range at V_{IN} covers the full dynamic range (0 to −4 V) of the ADC. All resistors should be the same type and from the same manufacturer so that their temperature coefficients match.

For ac sampling applications it is possible to substitute the op amp, A1, for a sample-and-hold amplifier SHA. Not all SHAs have both the inverting and noninverting terminals available to the user in which case the op amp is still necessary to level shift the analog input.

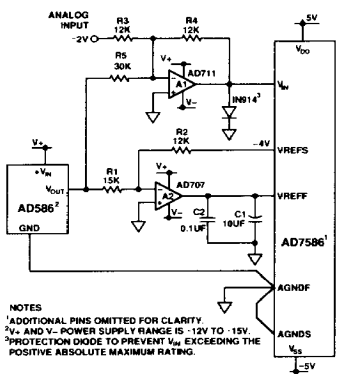


Figure 7. AD7586 Bipolar Operation

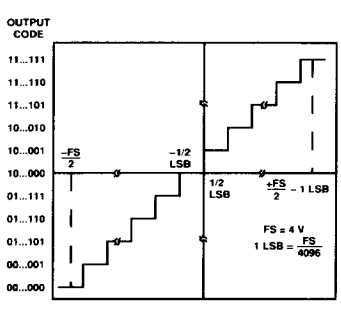


Figure 8. Ideal Input/Output Transfer Function for the Circuit of Figure 7

BIPOLAR OFFSET AND GAIN ERROR ADJUST

For applications where absolute accuracy is important then system offset and gain errors can be adjusted to zero using the force/sense amplifiers as in the unipolar case. In the case of Figure 7, one source of gain error is the resistor mismatch between R3 and R4. This error in conjunction with other gain error sources can be nulled by making either R2 or R3 variable and using the same adjustment procedure as discussed for the unipolar circuit. For offset adjustment, an AGND force/sense amplifier is needed with the same resistor biasing and trim arrangement as that shown in Figure 6 (R4, R5 and R6). Again, the adjustment procedure is the same as that discussed for Figure 6. Note, the analog input signal is level shifted by −2 V, therefore, −2 V must be subtracted from the first and last code transition voltages listed in Table I before being applied to this circuit.

TIMING AND CONTROL

Conversion start and data access are controlled by four digital inputs: $\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$ and MODE. There are two basic modes of operation, Mode 0 and Mode 1 which are shown in Figures 9 to 11. Mode 0 is designed for applications where a microprocessor has complete control over conversion start and data access. Mode 1 is designed for DSP applications where a timer controls conversion start, ensuring equal sampling intervals, while data access is again controlled by a microprocessor. The AD7586 MODE input pin selects the timing mode: MODE = 0 V for Mode 0 and MODE = 5 V for Mode 1.

Mode 0 (MODE = 0 V)

For direct bus interfacing using Mode 0, the microprocessor must have a WAIT state facility. A read operation to the ADC brings $\overline{CS}$ and $\overline{RD}$ low which triggers a conversion. The AD7586 acknowledges by bringing $\overline{BUSY}$ low indicating that conversion is in progress. $\overline{BUSY}$ returns high at the end of conversion when the ADC's output latches have been updated and the conversion result is placed on the data outputs. Note the data bus is in the three-state condition for the duration of the conversion and becomes active before $\overline{BUSY}$ goes high (see t_3, Figure 9) at the end of conversion.

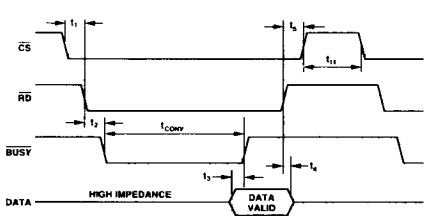


Figure 9. Mode 0 Timing Diagram (Mode = 0 V)

Mode 1 (MODE = 5 V)

In this mode conversion is started by asserting the $\overline{CONVST}$ input (see Figure 10). $\overline{BUSY}$ goes low after the falling of the $\overline{CONVST}$ input. However, the ADC conversion procedure does not start until after the rising of the $\overline{CONVST}$ pulse. $\overline{BUSY}$ returns high when conversion is complete. The total width of the $\overline{BUSY}$ pulse is equal to the $\overline{CONVST}$ pulse width plus the ADC conversion time. Note, the time t_{CONV} is typically 30 ns larger in Mode 1 than in Mode 0. Data can be read by a microprocessor any time after the rising edge of $\overline{BUSY}$. Note that pulsing $\overline{CONVST}$ low while a conversion is in progress will initiate a new conversion.

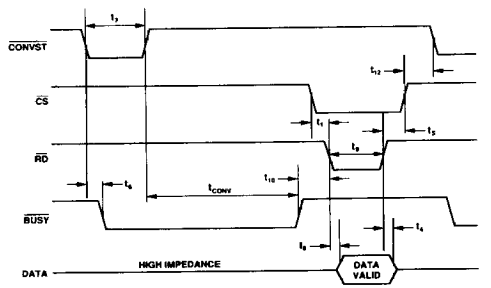


Figure 10. Mode 1 Timing Diagram (Mode = 5 V)

Figure 11 shows a variation of Mode 1 timing that is useful when external latches are used to store the conversion results. In this case, $\overline{CS}$ and $\overline{RD}$ are tied permanently low and the data bus is always active, except when $\overline{BUSY}$ is low. The data bus is in the three-state condition during the $\overline{BUSY}$ low state. The data bus then becomes active just before $\overline{BUSY}$ returns high at the end of conversion, so that $\overline{BUSY}$ can be used as a clocking signal for external latches.

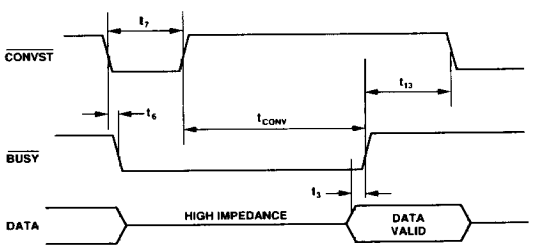


Figure 11. Mode 1 Timing Diagram, $\overline{CS}$ = $\overline{RD}$ = 0 V (Mode = 5 V)

SAMPLE-AND-HOLD INTERFACING

A sample-and-hold amplifier is necessary for ac applications. The interface connections are straight forward as shown for the AD684 in Figure 12. The AD7586 $\overline{BUSY}$ signal is ideal for triggering a SHA's HOLD input. An important SHA specification for ADC interfacing is settling time. This is the time required by the SHA output to settle after receiving a HOLD command. To allow for this, there must be a delay which is at least as long as the SHA settling time between the HOLD command and the AD7586's first flash decision. Large hold-mode settling time can be compensated for in Mode 1. The delay between the start of a conversion and the first flash decision is approximately 200 ns. In Mode 1 timing, $\overline{BUSY}$ goes low when $\overline{CONVST}$ goes low but the conversion procedure does not start until $\overline{CONVST}$ goes high. So, the $\overline{CONVST}$ pulse width can be used to compensate for any additional SHA settling time greater than 200 ns. For example, if a SHA has a settling time of 500 ns, then the $\overline{CONVST}$ pulse width should be 300 ns.

AD684 SAMPLE-AND-HOLD

The AD684 is a quad sample-and-hold (SHA) with an acquisition time of 1 μs. Figure 12 shows the SHA coupled with the AD7586 to form a single channel data acquisition system. To calculate the overall throughput rate, the acquisition time and the settling time of the SHA along with the ADC conversion time have to be taken into account. For the single channel system shown in Figure 12, the minimum throughput time is approximately 2.5 μs. This figure allows for 1 μs each for acquisition and conversion time and 500 ns for settling time and other overheads.

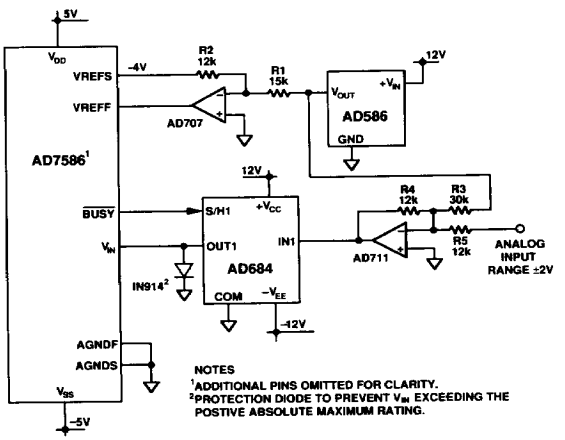


Figure 12. AD684–AD7586 Interface