



## **Dolby Virtual Speaker / Dolby Headphone Decoder**

### General Description

The NJU26220 simulates a highly realistic 5.1-speaker surround sound listening environment from as few as two speakers or headphone by Dolby Virtual Speaker/Dolby Headphone technology.

The NJU26220 processes the Dolby Virtual Speaker and Dolby Headphone technology that combined with Pro Logic II processing. It includes Pro Logic II decoder. Moreover, multi-channel signal inputs from an external decoder are possible.

It is suitable for digital TVs, stereo mini-components, PCs, and any audio/visual products.





NJU26220FN2

#### **FEATURES**

- Dolby Virtual Speaker
- Dolby Headphone
- Dolby Pro Logic II (Max 5.1ch Output)
- Multi-channel signals input (Max 5.1ch Input)
- Monitor output
- Lip-Sync Delay function (Digital Audio Delay)

#### Digital Signal Processor Specification

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 12.288MHz(Standard), built-in PLL Circuit
- Digital Audio Interface
  : 4 Input ports / 4 Output ports
- Microcomputer Interface
- r Interface : I<sup>2</sup>C Bus (Standard-mode/100kbps, Fast-mode/400kbps)

: QFP48-N2 (Pb-Free)

- : 4-Wire Serial Bus (4-Wire: Clock, Enable, Input data, Output data)
- Power Supply
- : DSP Core : 1.8V : I/O interface: 3.3V(+5.0V Input tolerant)

Package

New Japan Radio Co., Ltd.

# NJU26220

www.DataSheet4U.com

## DSP Block Diagram



Fig.1 NJU26220 Block Diagram





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## Pin Configuration



Fig.3 Pin Configuration

# NJU26220

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## Pin Description

### **Table1 Pin Description**

1      VDDO      P      I/O Power Supply 4:33/        2      BCKI      1      Bit Clock Input        3      VSSIO      G      I/O Power Supply GND        4      VSS      G      DSP Core Power Supply (SND        5      VDD      P      DSP Core Power Supply (SND        6      TEST0      I*      for test (connect with VSSIO through 3:3-ohm resistance.)        7      MUTEb      I      Master Volume Status after reset '1': OdB, O: Mute        8      WDC      OD*      Watchdog Clock output pin (Open-Drain Output)        9      PROC      I      Signal Processing after reset '1': Normal Processing, '0': Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply (GND        11      VDDIO      P      I/L Power Supply (SND        13      VDDPLL      P      PLL Power Supply +1.8V        14      VSSIO      G      DSP Core Power Supply +1.8V        14      VSSIO      G      DSP Core Power Supply +1.8V        17      CLKOUT      O SC Clock Unput        18      CLK      1      OSC Clock Unput<	Pin No.	Symbol	I/O	Function
2      BCKI      I      Bit Clock Input        3      VSSIO      G      I/O Power Supply GND        4      VSS      G      DSP Core Power Supply 41.8V        6      TESTO      I*      for test (connect with VSSIO through 3.3-ohm resistance.)        7      MUTEb      I*      Master Volume Status after reset '1: Odb, 0: Mute        8      WDC      OD*      Watchdog Clock output pin (Open-Drain Output)        9      PROC      I*      Signal Processing after reset '1: Normal Processing, 0: Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply GND        11      VDDIO      P      I/O Power Supply GND        13      VDSPLL      PLL Power Supply GND        14      VSSIO      G      DSP Core Power Supply GND        15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply H.3V        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Cock Output        19      VSSIO      G      I/O Power Supply H.3W	1	VDDIO	Р	I/O Power Supply +3.3V
3      VSSIO      G      I/O Power Supply GND        4      VSS      G      DSP Core Power Supply H.8/V        5      VDD      P      DSP Core Power Supply H.8/V        6      TEST0      I*      for test (connect with VSSIO through 3.3-ohm resistance.)        7      MUTEb      I*      Master Volume Status after reset "1: Normal Processing. '0: Waiting for a Command without Processing        9      PROC      I*      Signal Processing after reset "1:Normal Processing. '0: Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply GND        11      VDDIO      P      I/O Power Supply 43.3V        12      SEL      I      Host Interface Selection '1: Serial Interface, '0: I*C bus        13      VDDPLL      P      PLL Power Supply 43.8V        14      VSSIO      G      DSP Core Power Supply H.8V        15      VSS      G      DSP Core Power Supply H.8V        16      VDD      P      DSP Core Power Supply H.8V        17      CLKOUT      O SC Clock Unput (12.288MHz)        18      CLK      I      OSC Clock Unput (12.284MHz)	2	BCKI	I	Bit Clock Input
4      VSS      G      DSP Core Power Supply GND        5      VDD      P      DSP Core Power Supply +1.8V        6      TEST0      I*      for test (connect with VSSIO through 3.3-ohm resistance.)        7      MUTEb      I*      Master Volume Status after reset '1: Odb, 0: Mute        8      WDC      OD*      Watchdog Clock output pin (Open-Drain Output)        9      PROC      I*      Signal Processing after reset '1: Normal Processing, 0': Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply GND        11      VDDIO      P      I/O Power Supply GND        12      SEL      I      Host Interface Selection '1: Serial Interface, '0: I'C bus        13      VDDPLL      P LL Power Supply GND      I        14      VSSIG      G      DSP Core Power Supply GND        15      VSS      G      DSP Core Power Supply H3.8V        16      VDD      P      IOS Cock Output        17      CLKOUT      O      OSC Clock Nuput (12.288MHz)        19      VSSIO      G      I/O Power Supply GND        20      <	3	VSSIO	G	I/O Power Supply GND
5      VDD      P      DSP Core Power Supply +1.8V        6      TEST0      I*      for test (connect with VSSIO through 3.3-ohm resistance.)        7      MUTEb      I*      Master Volume Status after reset '1: 0dB, 0': Mute        8      WDC      OD*      Watchdog Clock output ipi (Open-Drain Output)        9      PROC      I*      Gringel Processing after reset '1:Normal Processing. '0: Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply 43.3V        12      SEL      I      Host Interface Selection '1: Serial Interface, '0: I'C bus        13      VDDPLL      P      PLL Power Supply (AND        14      VSSIO      G      DSP Core Power Supply (GND        15      VSS      G      DSP Core Power Supply (AND        16      VDD      P      DSP Core Power Supply (AND        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Niput (12.288MHz)        20      VDDIO      P      I/O Power Supply (SND        21      RESETb      I      Reset (RESETb='0: DSP Reset)        2	4	VSS	G	DSP Core Power Supply GND
6      TEST0      I*      for test (connect with VSSIO through 3.3-ohm resistance).        7      MUTEb      I*      Master Volume Status after reset '1': 00B, '0': Mute        8      WDC      OD*      Watchdog Clock output pin (Open-Drain Output)        9      PROC      I*      Signal Processing after reset '1': Normal Processing, '0': Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply GND        11      VDDIO      P      I/O Power Supply GND        12      SEL      I Hoost Interface Selection '1': Serial Interface, '0': I'C bus        13      VDDPLL      P      PLL Power Supply GND        14      VSSIO      G      DSP Core Power Supply GND        15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply GND        17      CLKOUT      O      OSC Clock Output (12.28MHz)        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply H1.8V        21      RESETb      I      for test (connect to VDSIO)        22	5	VDD	Р	DSP Core Power Supply +1.8V
7      MUTEb      I*      Master Volume Status after reset '1': VdB, '0: Mute        8      WDC      OD*      Watchdog Clock output pin (Open-Drain Output)        9      PROC      I*      Signal Processing after reset '1':Normal Processing, '0: Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply (GND        11      VDDIO      P      I/O Power Supply +1.8V        12      SEL      I      Host Interface Selection '1': Serial Interface, '0': I'C bus        13      VDDPLL      P      PLL Power Supply H.8V        14      VSSPLL      G      PLL Power Supply GND        15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply GND        18      CLK      I      OSC Clock Output        18      CLK      I      OSC Clock Output        20      VDDIO      P      I/O Power Supply GND        21      RESETb      I      Reset (RESETb=0'): DSP Reset)        22      TEST1      I      for test (connect to VSSIO)        24      TEST3      I	6	TEST0	*	for test (connect with VSSIO through 3.3-ohm resistance.)
8      WDC      OD*      Watchdog Clock output pin (Open-Drain Output)        9      PROC      I*      Signal Processing after reset '1'.Normal Processing, '0': Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply GND        11      VDDIO      P      I/O Power Supply +3.3V        12      SEL      1      Host Interface Selection '1': Serial Interface, '0': I'C bus        13      VDDPLL      P      PLL Power Supply H.8V        14      VSSPLL      G      PLL Power Supply GND        15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply GND        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Output        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply GND        21      RESETb      I      Reset(RESETb-0': DSP Reset)        22      TEST1      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to	7	MUTEb	*	Master Volume Status after reset '1': 0dB, '0': Mute
9      PROC      I'      Signal Processing after reset '1':Normal Processing. '0': Waiting for a Command without Processing        10      VSSIO      G      I/O Power Supply GND        11      VDDIO      P      I/O Power Supply 3.3V        12      SEL      I      Host Interface Selection '1': Serial Interface, '0': I'C bus        13      VDDPLL      P      PLL Power Supply 41.8V        14      VSSPLL      G      PLL Power Supply GND        16      VDD      P      DSP Core Power Supply GND        16      VDD      P      DSC Clock Output        18      CLK      I      OSC Clock Nutput (12.288MHz)        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply -1.8V        21      RESETb      I      for test (connect to VSSIO)        23      TEST2      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to VSSIO)        25      AD1/SDIN      I      I'C Address (I'C mode) / Serial In (4-wire serial mode)        26      AD2/SSb      I	8	WDC	OD*	Watchdog Clock output pin (Open-Drain Output)
10      VSSIO      G      I/O Power Supply GND        11      VDDIO      P      I/O Power Supply 4:33V        12      SEL      I      Host Interface Selection '1': Serial Interface, '0': I'C bus        13      VDDPLL      P      PLL Power Supply 4:18V        14      VSS      G      DSP Core Power Supply GND        15      VSS      G      DSP Core Power Supply 4:1.8V        16      VDD      P      DSP Core Power Supply 4:1.8V        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Nuput (12:288MHz)        19      VSSIO      G      I/O Power Supply -0ND        20      VDDIO      P      I/O Power Supply -0.33V        21      RESETb      I      for test (connect to VSSIO)        23      TEST2      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect oVSSIO)        25      AD1/SDIN      I 'C Address ('C mode) / Serial enable (4-wire serial mode)        26      AD2/SSb      I 'C SDA('C mode) / Serial clock (4-wire serial mode)	9	PROC	*	Signal Processing after reset '1':Normal Processing, '0': Waiting for a Command without Processing
11      VDDIO      P      I/O Power Supply +3.3V        12      SEL      I      Host Interface Selection '1': Serial Interface, '0': I'C bus        13      VDDPLL      P      PLL Power Supply 1NV        14      VSSPLL      G      PLL Power Supply GND        15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply 1NV        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Nuput (12.288MHz)        19      VSSIO      G      I/O Power Supply +3.3V        20      VDDIO      P      I/O Power Supply +3.3V        21      RESETb      I      Reset (connect to VSSIO)        23      TEST1      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to VSSIO)        25      ADI/SDIN      I      I'C Address (I'C mode) / Serial ln(4-wire serial mode)        26      AD2/SSb      I      I'C Address (I'C mode) / Serial cout (4-wire serial mode)        28      SDA/SDOUT      I/O      Poes Dove Power Suppl	10	VSSIO	G	I/O Power Supply GND
12      SEL      I      Host Interface Selection '1': Serial Interface, '0': I <sup>C</sup> Dus        13      VDDPLL      P      PLL Power Supply Y1.8V        14      VSSPLL      G      PLL Power Supply GND        15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply GND        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Nupt (1.2288MHz)        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply GND        21      RESETb      I      Reset (RESETb='0': DSP Reset)        22      TEST1      I      for test (connect to VSSIO)        23      TEST2      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to VSSIO)        25      AD1/SDIN      I      fC Address (fC mode) / Serial enable (4-wire serial mode)        27      SCL/SCK      I      fC SCL (fC mode) / Serial Cut (4-wire serial mode)        28      SDA/SDOUT      I/O      POWE Power Supply	11	VDDIO	Р	I/O Power Supply +3.3V
13      VDDPLL      P      PLL Power Supply +1.8V        14      VSSPLL      G      PLL Power Supply GND        15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply H.8V        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Nuput (12.288MHz)        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply +3.3V        21      RESETD      I      Reset (connect to VDDIO)        23      TEST2      I      for test (connect to VDDIO)        24      TEST3      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to VSSIO)        25      AD1/SDIN      I      I*C Address (I*C mode) / Serial lout (4-wire serial mode)        27      SCL/SCK      I      I*C Address (I*C mode) / Serial Cut (4-wire serial mode)        28      SDA/SDOUT      I/O      P      DSP Core Power Supply 41.	12	SEL	I	Host Interface Selection '1': Serial Interface, '0': I <sup>2</sup> C bus
14      VSSPLL      G      PLL Power Supply GND        15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply +1.8V        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Output        19      VSSIO      G      I/O Power Supply +3.3V        20      VDDIO      P      I/O Power Supply +3.3V        21      RESETb      1      Reset (RESETb='0: DSP Reset)        22      TEST1      1      for test (connect to VSSIO)        24      TEST3      1      for test (connect to VSSIO)        25      ADI/SDIN      1      I'C Address (I'C mode) / Serial loak (4-wire serial mode)        26      AD2/SSb      1      I'C Address (I'C mode) / Serial onot (4-wire serial mode)        28      SDA/SDOUT      I/O      I'C SDA (I'C mode) / Serial Ock (4-wire serial mode)        29      VDD      P      DSP Core Power Supply +1.8V        30      VSS      G      DSP Core Power Supply 43.3V        33      MCK      O      AL(ock Output  <	13	VDDPLL	Р	PLL Power Supply +1.8V
15      VSS      G      DSP Core Power Supply GND        16      VDD      P      DSP Core Power Supply 1.8V        17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Output        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply 4.3.3V        21      RESETb      I      Reset (RESETb='0: DSP Reset)        22      TEST1      I      for test (connect to VSSIO)        24      TEST2      I      for test (connect to VSSIO)        25      AD1/SDIN      I      I'C Address (I'C mode) / Serial In (4-wire serial mode)        26      AD2/SSb      I      I'C SCL (I'C mode) / Serial clock (4-wire serial mode)        27      SCL/SCK      I      I'C SDA (I'C mode) / Serial clock (4-wire serial mode)        28      SDA/SDOUT      I/O      FC SDA (I'C mode) / Serial Cot (4-wire serial mode)        30      VSS      G      DSP Core Power Supply H.1.8V        30      VSS      G      DSP Core Power Supply GND        31      VSSIO      G	14	VSSPLL	G	PLL Power Supply GND
16      VDD      P      DSP Core Power Supply +1.8V        17      CLKOUT      O      OSC Clock Unput (12.288MHz)        18      CLK      I      OSC Clock Input (12.288MHz)        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply +3.3V        21      RESETb      I      Reset (RESETb='0': DSP Reset)        22      TEST1      I      for test (connect to VDDIO)        23      TEST2      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to VSSIO)        25      AD1/SDIN      I      f'C Address (f'C mode) / Serial ln (4-wire serial mode)        27      SCL/SCK      I      f'C SCL (f'C mode) / Serial anable (4-wire serial mode)        28      SDA/SDOUT      I/O      f'C SDA (f'C mode) / Serial anable (4-wire serial mode)        29      VDD      P      DSP Core Power Supply +1.8V        30      VSS      G      DSP Core Power Supply GND        31      VSSIO      G      I/O Power Supply A3.3V        33      MCK      O      A	15	VSS	G	DSP Core Power Supply GND
17      CLKOUT      O      OSC Clock Output        18      CLK      I      OSC Clock Input (12.288MHz)        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply +3.3V        21      RESETb      I      Reset (RESETb='0': DSP Reset)        22      TEST1      I      for test (connect to VDSIO)        23      TEST2      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to VSSIO)        25      AD1/SDIN      I      I <sup>2</sup> C Address (I <sup>4</sup> C mode) / Serial enable (4-wire serial mode)        26      AD2/SSb      I      I <sup>2</sup> C Address (I <sup>4</sup> C mode) / Serial clock (4-wire serial mode)        27      SCL/SCK      I      I <sup>2</sup> C SDA (I <sup>4</sup> C mode) / Serial clock (4-wire serial mode)        28      SDA/SDOUT      I/O      I/O      Source Supply Senial clock (4-wire serial mode)        30      VSS      G      DSP Core Power Supply GND      III        31      VSSIO      G      I/O Power Supply RND      IIII        32      VDDIO      P      I/O Power Supply H 3.3V	16	VDD	Р	DSP Core Power Supply +1.8V
18      CLK      I      OSC Clock Input (12.288MHz)        19      VSSIO      G      I/O Power Supply GND        20      VDDIO      P      I/O Power Supply GND        21      RESETb      I      Reset (RESETb='0': DSP Reset)        22      TEST1      I      for test (connect to VDDIO)        23      TEST2      I      for test (connect to VSSIO)        24      TEST3      I      for test (connect to VSSIO)        25      AD1/5DIN      I      I'C Address (I'C mode) / Serial enable (4-wire serial mode)        26      AD2/SSb      I      I'C Address (I'C mode) / Serial Out (4-wire serial mode)        27      SCL/SCK      I      I'C SDA (I'C mode) / Serial Out (4-wire serial mode)        28      SDA/SDOUT      I/O      I'C SDA (I'C mode) / Serial Out (4-wire serial mode)        29      VDD      P      DSP Core Power Supply H.8V        30      VSS      G      DSP Core Power Supply GND        31      VSSIO      G      I/O Power Supply GND        32      VDDIO      P      I/O Power Supply H.3.V       33      MCK      AUD, D/A	17	CLKOUT	0	OSC Clock Output
19    VSSIO    G    I/O Power Supply GND      20    VDDIO    P    I/O Power Supply +3.3V      21    RESETb    I    Reset (RESETb='0: DSP Reset)      22    TEST1    I    for test (connect to VDDIO)      23    TEST2    I    for test (connect to VSSIO)      24    TEST3    I    for test (connect to VSSIO)      25    AD1/SDIN    I    I*C Address (I*C mode) / Serial anable (4-wire serial mode)      26    AD2/SSb    I    I*C Address (I*C mode) / Serial clock (4-wire serial mode)      27    SCL/SCK    I    I*C SDA (I*C mode) / Serial clock (4-wire serial mode)      28    SDA/SDOUT    I/O    I*C SDA (I*C mode) / Serial Out (4-wire serial mode)      29    VDD    P    DSP Core Power Supply GND      31    VSSIO    G    I/O Power Supply GND      32    VDDIO    P    I/O Power Supply GND      33    MCK    O    A/D, D/A clock output (buffer output of a CLK pin)      34    BCKO    O    Bit Clock Output      35    LRO    O    LR clock Output ch.3 (Surround channel (LS/RS) output)	18	CLK	I	OSC Clock Input (12.288MHz)
20  VDDIO  P  I/O Power Supply +3.3V    21  RESETb  I  Reset (RESETb='0': DSP Reset)    22  TEST1  I  for test (connect to VDDIO)    23  TEST2  I  for test (connect to VSSIO)    24  TEST3  I  for test (connect to VSSIO)    25  AD1/SDIN  I  I'C Address (I'C mode) / Serial enable (4-wire serial mode)    26  AD2/SSb  I  I'C C Cl C mode) / Serial clock (4-wire serial mode)    27  SCL/SCK  I  I'C SDA (I'C mode) / Serial clock (4-wire serial mode)    28  SDA/SDOUT  I/O  I'C SDA (I'C mode) / Serial clock (4-wire serial mode)    29  VDD  P  DSP Core Power Supply 1.8V    30  VSS  G  DSP Core Power Supply GND    31  VSSIO  G  I/O Power Supply GND    32  VDDIO  P  I/O Power Supply 43.3V    33  MCK  O  A/D, D/A clock output (buffer output of a CLK pin)    34  BCKO  O  Bit Clock Output    35  LRO  O  LR clock Output    36  SDO3  O  Audio Data Output ch.3 (Surround channel (LS/RS) output)    38  SDO1  O  Audio Data Output ch.1 (Front channel (L/S) output)<	19	VSSIO	G	I/O Power Supply GND
21    RESETb    I    Reset (RESETb='0': DSP Reset)      22    TEST1    I    for test (connect to VDDIO)      23    TEST2    I    for test (connect to VSSIO)      24    TEST3    I    for test (connect to VSSIO)      25    AD1/SDIN    I    I <sup>2</sup> C Address (I <sup>2</sup> C mode) / Serial ln (4-wire serial mode)      26    AD2/SSb    I    I <sup>2</sup> C Address (I <sup>2</sup> C mode) / Serial clock (4-wire serial mode)      27    SCL/SCK    I    I <sup>2</sup> C SCL (I <sup>2</sup> C mode) / Serial clock (4-wire serial mode)      28    SDA/SDOUT    I/O    I <sup>2</sup> C SDA (I <sup>2</sup> C mode) / Serial clock (4-wire serial mode)      29    VDD    P    DSP Core Power Supply 41.8V      30    VSS    G    DSP Core Power Supply GND      31    VSSIO    G    I/O Power Supply GND      32    VDDIO    P    I/O Power Supply 43.3V      33    MCK    O    A/D, D/A clock output (buffer output of a CLK pin)      34    BCKO    O    Et Clock Output      35    LRO    O    LR clock Output ch.3 (Surround channel (LS/RS) output)      37    SDO2    O    Audio Data Output ch.3 (Wonito	20	VDDIO	Р	I/O Power Supply +3.3V
22    TEST1    I    for test (connect to VDDIO)      23    TEST2    I    for test (connect to VSSIO)      24    TEST3    I    for test (connect to VSSIO)      25    AD1/SDIN    I    I <sup>C</sup> Address (I <sup>C</sup> mode) / Serial In (4-wire serial mode)      26    AD2/SSb    I    I <sup>C</sup> Address (I <sup>C</sup> mode) / Serial enable (4-wire serial mode)      27    SCL/SCK    I    I <sup>C</sup> C SDA (I <sup>C</sup> mode) / Serial Out (4-wire serial mode)      28    SDA/SDOUT    I/O    I <sup>C</sup> C SDA (I <sup>C</sup> mode) / Serial Out (4-wire serial mode)      29    VDD    P    DSP Core Power Supply +1.8V      30    VSS    G    DSP Core Power Supply GND      31    VSSIO    G    I/O Power Supply GND      32    VDDIO    P    I/O Power Supply +3.3V      33    MCK    O    Adio Data Output to 1a CLK pin)      34    BCKO    O    Bit Clock Output      35    LRO    O    LR Clock Output th.3 (Surround channel (LS/RS) output)      36    SDO3    O    Audio Data Output th.1 (Front channel (L/R) output)      39    SDO0    O    Audio Data Output th.0 (Monitor out	21	RESETb	I	Reset (RESETb='0': DSP Reset)
23    TEST2    I    for test (connect to VSSIO)      24    TEST3    I    for test (connect to VSSIO)      25    AD1/SDIN    I    I <sup>2</sup> C Address (I <sup>2</sup> C mode) / Serial In (4-wire serial mode)      26    AD2/SSb    I    I <sup>2</sup> C Address (I <sup>2</sup> C mode) / Serial enable (4-wire serial mode)      27    SCL/SCK    I    I <sup>2</sup> C SOL (I <sup>2</sup> C mode) / Serial Cuts (4-wire serial mode)      28    SDA/SDOUT    I/O    I <sup>2</sup> C SOL (I <sup>2</sup> C mode) / Serial Out (4-wire serial mode)      29    VDD    P    DSP Core Power Supply +1.8V      30    VSS    G    DSP Core Power Supply GND      31    VSSIO    G    I/O Power Supply GND      32    VDDIO    P    I/O Power Supply 41.3V      33    MCK    O    ADL /A clock output (buffer output of a CLK pin)      34    BCKO    O    Bit Clock Output      35    LRO    O    LR Clock Output      36    SDO3    O    Audio Data Output ch.3 (Surround channel (LS/RS) output)      38    SDO1    O    Audio Data Output ch.0 (Monitor output)      39    SDO0    O    Audio Data Output ch.0 (Monitor outp	22	TEST1	I	for test (connect to VDDIO)
24    TEST3    I    for test (connect to VSSIO)      25    AD1/SDIN    I    I <sup>2</sup> C Address (I <sup>2</sup> C mode) / Serial enable (4-wire serial mode)      26    AD2/SSb    I    I <sup>2</sup> C Address (I <sup>2</sup> C mode) / Serial enable (4-wire serial mode)      27    SCL/SCK    I    I <sup>2</sup> C SCL (I <sup>2</sup> C mode) / Serial clock (4-wire serial mode)      28    SDA/SDOUT    I/O    I <sup>2</sup> C SDA (I <sup>2</sup> C mode) / Serial Out (4-wire serial mode)      29    VDD    P    DSP Core Power Supply +1.8V      30    VSS    G    DSP Core Power Supply GND      31    VSSIO    G    I/O Power Supply GND      32    VDDIO    P    I/O Power Supply +3.3V      33    MCK    O    A/D, D/A clock output (buffer output of a CLK pin)      34    BCKO    O    Bit Clock Output      35    LRO    O    LR Clock Output      36    SDO3    O    Audio Data Output ch.3 (Surround channel (LS/RS) output)      38    SDO1    O    Audio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)      39    SDO0    O    Audio Data Output ch.2 (Monitor output)      40    VDDIO    P	23	TEST2	I	for test (connect to VSSIO)
25    AD1/SDIN    1    I*C Address (I*C mode) / Serial In (4-wire serial mode)      26    AD2/SSb    1    I*C Address (I*C mode) / Serial enable (4-wire serial mode)      27    SCL/SCK    1    I*C SCL (I*C mode) / Serial Ock (4-wire serial mode)      28    SDA/SDOUT    I/O    I*C SDA (I*C mode) / Serial Out (4-wire serial mode)      29    VDD    P    DSP Core Power Supply +1.8V      30    VSS    G    DSP Core Power Supply GND      31    VSSIO    G    I/O Power Supply GND      32    VDDIO    P    I/O Power Supply GND      33    MCK    O    A/D, D/A clock output (buffer output of a CLK pin)      34    BCKO    O    Bit Clock Output      35    LRO    O    LR Clock Output ch.3 (Surround channel (LS/RS) output)      36    SDO3    O    Audio Data Output ch.3 (Surround channel (LS/RS) output)      38    SDO1    O    Audio Data Output ch.3 (Surround channel (L/R) output)      39    SDO0    O    Audio Data Output ch.3 (Monitor output)      40    VDDIO    P    I/O Power Supply GND      41    VSSIO    G	24	TEST3		for test (connect to VSSIO)
26    AD2/SSb    I    I*C Address (I*C mode) / Serial enable (4-wire serial mode)      27    SCL/SCK    I    I*C SCL (I*C mode) / Serial clock (4-wire serial mode)      28    SDA/SDOUT    I/O    I*C SCL (I*C mode) / Serial Out (4-wire serial mode)      29    VDD    P    DSP Core Power Supply 1.8V      30    VSS    G    DSP Core Power Supply GND      31    VSSIO    G    I/O Power Supply H3.3V      33    MCK    O    A/D, D/A clock output (buffer output of a CLK pin)      34    BCKO    O    Bit Clock Output      35    LRO    O    LR Clock Output      36    SDO3    O    Audio Data Output ch.3 (Surround channel (LS/RS) output)      37    SDO2    O    Audio Data Output ch.1 (Front channel (L/R) output)      38    SDO1    O    Audio Data Output ch.0 (Monitor output)      40    VDDIO    P    I/O Power Supply GND      41    VSSIO    G    DSP Core Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply GND      44 <td>25</td> <td>AD1/SDIN</td> <td></td> <td>I'C Address (I'C mode) / Serial In (4-wire serial mode)</td>	25	AD1/SDIN		I'C Address (I'C mode) / Serial In (4-wire serial mode)
27SCL/SCKII*C SCL (I*C mode) / Serial clock (4-wire serial mode)28SDA/SDOUTI/OI*C SDA (I*C mode) / Serial Out (4-wire serial mode)29VDDPDSP Core Power Supply +1.8V30VSSGDSP Core Power Supply GND31VSSIOGI/O Power Supply GND32VDDIOPI/O Power Supply +3.3V33MCKOA/D, D/A clock output (buffer output of a CLK pin)34BCKOOBit Clock Output35LROOLR Clock Output ch.3 (Surround channel (LS/RS) output)37SDO2OAudio Data Output ch.3 (Surround channel (L/R) output)38SDO1OAudio Data Output ch.1 (Front channel (L/R) output)39SDO0OAudio Data Output ch.0 (Monitor output)41VSSIOGI/O Power Supply GND42VSSGDSP Core Power Supply GND43VDDPDSP Core Power Supply GND44SDI3IAudio Data Input ch.345SDI2IAudio Data Input ch.345SDI2IAudio Data Input ch.246SDI1IAudio Data Input ch.147SDI0IAudio Data Input ch.048III48III48II48II	26	AD2/SSb		1 <sup>c</sup> C Address (I <sup>c</sup> C mode) / Serial enable (4-wire serial mode)
28SDA/SDOUTI/OI'C SDA (I'C mode) / Serial Out (4-wire serial mode)29VDDPDSP Core Power Supply +1.8V30VSSGDSP Core Power Supply GND31VSSIOGI/O Power Supply GND32VDDIOPI/O Power Supply +3.3V33MCKOA/D, D/A clock output (buffer output of a CLK pin)34BCKOOBit Clock Output35LROOLR Clock Output36SDO3OAudio Data Output ch.3 (Surround channel (LS/RS) output)37SDO2OAudio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)38SDO1OAudio Data Output ch.0 (Monitor output)40VDDIOPI/O Power Supply H3.3V41VSSIOGI/O Power Supply GND42VSSGDSP Core Power Supply GND43VDDPDSP Core Power Supply GND44SDI3IAudio Data Input ch.345SDI2IAudio Data Input ch.345SDI2IAudio Data Input ch.147SDI0IAudio Data Input ch.048LBIILB Clock Input	27	SCL/SCK	I	I <sup>2</sup> C SCL (I <sup>2</sup> C mode) / Serial clock (4-wire serial mode)
29VDDPDSP Core Power Supply +1.8V30VSSGDSP Core Power Supply GND31VSSIOGI/O Power Supply GND32VDDIOPI/O Power Supply +3.3V33MCKOA/D, D/A clock output (buffer output of a CLK pin)34BCKOOBit Clock Output35LROOLR Clock Output ch.3 (Surround channel (LS/RS) output)36SDO3OAudio Data Output ch.3 (Surround channel (LS/RS) output)38SDO1OAudio Data Output ch.1 (Front channel (L/R) output)39SDO0OAudio Data Output ch.0 (Monitor output)40VDDIOPI/O Power Supply +3.3V41VSSIOGI/O Power Supply GND42VSSGDSP Core Power Supply GND43VDDPDSP Core Power Supply GND44SDI3IAudio Data Input ch.345SDI2IAudio Data Input ch.345SDI2IAudio Data Input ch.246SDI1IAudio Data Input ch.047SDI0IAudio Data Input ch.048LRIII R Clock Input f	28	SDA/SDOUT	I/O	I <sup>2</sup> C SDA (I <sup>2</sup> C mode) / Serial Out (4-wire serial mode)
30VSSGDSP Core Power Supply GND31VSSIOGI/O Power Supply GND32VDDIOPI/O Power Supply +3.3V33MCKOA/D, D/A clock output (buffer output of a CLK pin)34BCKOOBit Clock Output35LROOLR Clock Output36SDO3OAudio Data Output ch.3 (Surround channel (LS/RS) output)37SDO2OAudio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)38SDO1OAudio Data Output ch.1 (Front channel (L/R) output)39SDO0OAudio Data Output ch.0 (Monitor output)40VDDIOPI/O Power Supply H3.3V41VSSIOGI/O Power Supply GND42VSSGDSP Core Power Supply GND43VDDPDSP Core Power Supply GND44SDI3IAudio Data Input ch.345SDI2IAudio Data Input ch.345SDI2IAudio Data Input ch.147SDI0IAudio Data Input ch.148IIIR Clock Input f	29	VDD	Р	DSP Core Power Supply +1.8V
31VSSIOGI/O Power Supply GND32VDDIOPI/O Power Supply +3.3V33MCKOA/D, D/A clock output (buffer output of a CLK pin)34BCKOOBit Clock Output35LROOLR Clock Output36SDO3OAudio Data Output ch.3 (Surround channel (LS/RS) output)37SDO2OAudio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)38SDO1OAudio Data Output ch.1 (Front channel (L/R) output)39SDO0OAudio Data Output ch.0 (Monitor output)40VDDIOPI/O Power Supply H.3.3V41VSSIOGI/O Power Supply GND42VSSGDSP Core Power Supply GND43VDDPDSP Core Power Supply H.8.V44SDI3IAudio Data Input ch.345SDI2IAudio Data Input ch.147SDI0IAudio Data Input ch.147SDI0IAudio Data Input ch.148LBLIL R Clock Input	30	VSS	G	DSP Core Power Supply GND
32    VDDIO    P    I/O Power Supply +3.3V      33    MCK    O    A/D, D/A clock output (buffer output of a CLK pin)      34    BCKO    O    Bit Clock Output      35    LRO    O    LR Clock Output      36    SDO3    O    Audio Data Output ch.3 (Surround channel (LS/RS) output)      37    SDO2    O    Audio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)      38    SDO1    O    Audio Data Output ch.1 (Front channel (L/R) output)      39    SDO0    O    Audio Data Output ch.0 (Monitor output)      40    VDDIO    P    I/O Power Supply +3.3V      41    VSSIO    G    I/O Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply +1.8V      44    SDI3    I    Audio Data Input ch.3      45    SDI2    I    Audio Data Input ch.2      46    SDI1    I    Audio Data Input ch.1      47    SDI0    I    Audio Data Input ch.0      48    LRI    I    LR Clock Input	31	VSSIO	G	I/O Power Supply GND
33MCKOA/D, D/A clock output (buffer output of a CLK pin)34BCKOOBit Clock Output35LROOLR Clock Output36SDO3OAudio Data Output ch.3 (Surround channel (LS/RS) output)37SDO2OAudio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)38SDO1OAudio Data Output ch.1 (Front channel (L/R) output)39SDO0OAudio Data Output ch.0 (Monitor output)40VDDIOPI/O Power Supply +3.3V41VSSIOGI/O Power Supply GND42VSSGDSP Core Power Supply GND43VDDPDSP Core Power Supply +1.8V44SDI3IAudio Data Input ch.345SDI2IAudio Data Input ch.146SDI1IAudio Data Input ch.147SDI0IAudio Data Input ch.048LRIILR Clock Input	32	VDDIO	P	I/O Power Supply +3.3V
34    BCKO    O    Bit Clock Output      35    LRO    O    LR Clock Output      36    SDO3    O    Audio Data Output ch.3 (Surround channel (LS/RS) output)      37    SDO2    O    Audio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)      38    SDO1    O    Audio Data Output ch.1 (Front channel (L/R) output)      39    SDO0    O    Audio Data Output ch.0 (Monitor output)      40    VDDIO    P    I/O Power Supply +3.3V      41    VSSIO    G    I/O Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply H.8V      44    SDI3    I    Audio Data Input ch.3      45    SDI2    I    Audio Data Input ch.2      46    SDI1    I    Audio Data Input ch.1      47    SDI0    I    Audio Data Input ch.0      48    LRI    I    LR Clock Input	33	MCK	0	A/D, D/A clock output (buffer output of a CLK pin)
35LROOLR Clock Output36SDO3OAudio Data Output ch.3 (Surround channel (LS/RS) output)37SDO2OAudio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)38SDO1OAudio Data Output ch.1 (Front channel (L/R) output)39SDO0OAudio Data Output ch.0 (Monitor output)40VDDIOPI/O Power Supply +3.3V41VSSIOGI/O Power Supply GND42VSSGDSP Core Power Supply GND43VDDPDSP Core Power Supply +1.8V44SDI3IAudio Data Input ch.345SDI2IAudio Data Input ch.146SDI1IAudio Data Input ch.147SDI0IAudio Data Input ch.048LRIILR Clock Input ch.0	34	BCKO	0	Bit Clock Output
36    SD03    O    Audio Data Output ch.3 (Surround channel (LS/RS) output)      37    SD02    O    Audio Data Output ch.2 (Center/Sub Woofer channel (C/SW) output)      38    SD01    O    Audio Data Output ch.1 (Front channel (L/R) output)      39    SD00    O    Audio Data Output ch.0 (Monitor output)      40    VDDIO    P    I/O Power Supply +3.3V      41    VSSIO    G    I/O Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply +1.8V      44    SDI3    I    Audio Data Input ch.3      45    SDI2    I    Audio Data Input ch.2      46    SDI1    I    Audio Data Input ch.1      47    SDI0    I    Audio Data Input ch.0      48    L RI    I    I R Clock Input	35	LRO	0	LR Clock Output
37    SDO2    O    Audio Data Output ch.2 (Center/Sub Wooter channel (C/SW) output)      38    SDO1    O    Audio Data Output ch.1 (Front channel (L/R) output)      39    SDO0    O    Audio Data Output ch.0 (Monitor output)      40    VDDIO    P    I/O Power Supply +3.3V      41    VSSIO    G    I/O Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply +1.8V      44    SDI3    I    Audio Data Input ch.3      45    SDI2    I    Audio Data Input ch.2      46    SDI1    I    Audio Data Input ch.1      47    SDI0    I    Audio Data Input ch.0      48    L RI    I    I R Clock Input	36	SD03	0	Audio Data Output ch.3 (Surround channel (LS/RS) output)
38    SDO1    O    Audio Data Output ch.1 (Front channel (L/R) output)      39    SDO0    O    Audio Data Output ch.0 (Monitor output)      40    VDDIO    P    I/O Power Supply +3.3V      41    VSSIO    G    I/O Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply +1.8V      44    SDI3    I    Audio Data Input ch.3      45    SDI2    I    Audio Data Input ch.2      46    SDI1    I    Audio Data Input ch.1      47    SDI0    I    Audio Data Input ch.0      48    I.BI    I.B. Clock Input	37	SDO2	0	Audio Data Output ch.2 (Center/Sub Wooter channel (C/SW) output)
39    SDO0    O    Audio Data Output ch.0 (Monitor output)      40    VDDIO    P    I/O Power Supply +3.3V      41    VSSIO    G    I/O Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply +1.8V      44    SDI3    I    Audio Data Input ch.3      45    SDI2    I    Audio Data Input ch.2      46    SDI1    I    Audio Data Input ch.1      47    SDI0    I    Audio Data Input ch.0      48    LBI    I    LB Clock Input	38	SD01	0	Audio Data Output ch.1 (Front channel (L/R) output)
40    VDDIO    P    I/O Power Supply 43.3V      41    VSSIO    G    I/O Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply +1.8V      44    SDI3    I    Audio Data Input ch.3      45    SDI2    I    Audio Data Input ch.2      46    SDI1    I    Audio Data Input ch.1      47    SDI0    I    Audio Data Input ch.0      48    I BI    I B Clock Input	39	SDOU	0	Audio Data Output cn.0 (Monitor output)
41    VSSIO    G    I/O Power Supply GND      42    VSS    G    DSP Core Power Supply GND      43    VDD    P    DSP Core Power Supply +1.8V      44    SDI3    I    Audio Data Input ch.3      45    SDI2    I    Audio Data Input ch.2      46    SDI1    I    Audio Data Input ch.1      47    SDI0    I    Audio Data Input ch.0      48    I RI    I R Clock Input	40	VDDIO	P	I/O Power Supply +3.3V
42  VSS  G  DSP Core Power Supply GND    43  VDD  P  DSP Core Power Supply +1.8V    44  SDI3  I  Audio Data Input ch.3    45  SDI2  I  Audio Data Input ch.2    46  SDI1  I  Audio Data Input ch.1    47  SDI0  I  Audio Data Input ch.0    48  I RI  I  I R Clock Input	41	VSSIU	G	I/O Power Supply GND
43  VDD  P  DSP Core Power Supply +1.8V    44  SDI3  I  Audio Data Input ch.3    45  SDI2  I  Audio Data Input ch.2    46  SDI1  I  Audio Data Input ch.1    47  SDI0  I  Audio Data Input ch.0    48  I.Bl  I.B. Clock Input	42	V35	G	DSP Core Power Supply GND
44  SDIS  1  Audio Data Input Ch.3    45  SDI2  I  Audio Data Input ch.2    46  SDI1  I  Audio Data Input ch.1    47  SDI0  I  Audio Data Input ch.0    48  I RI  I  I R Clock Input	43			LOF OULE FOWEL OUPPLY + 1.0V
45  SDi2  1  Audio Data Input Ch2    46  SDI1  I  Audio Data Input ch.1    47  SDI0  I  Audio Data Input ch.0    48  I RI  I  I R Clock Input	44	0000 0100		Audio Data Input di
40  3011  1  Audio Data Input Ch.1    47  SDI0  I  Audio Data Input ch.0    48  I.Rl  I. I.R.Clock Input	40	5012 9011		Audio Data Input di 1.2
48 I RI I I R Clock Input	40			Audio Data Input ch.
	48			I R Clock Input

Note1: I: Input, O: Output, OD: Open-Drain Output, I/O: Bidirectional, P: +Power, G: GND

Note2: I/O with \* operate as bidirectional pins when test. Connect with VDDIO or VSSIO through 3.3k-ohm resistance.

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### 1. Audio Interface

The serial audio interface carries audio data to and from the NJU26220. Industry standard serial data formats of I<sup>2</sup>S, MSB-first left-justified or MSB-first right-justified are supported. Table 2 shows pin description of input pin and output pin of NJU26220.

Pin No.	Symbol	Description
47	SDI0	Stereo L/R input
46	SDI1	(Pin select)
45	SDI2	C/SW input
44	SDI3	SL/SR input
39	SDO0	Monitor output
38	SDO1	L/R output
37	SDO2	C/SW output
36	SDO3	SL/SR output

Table 2 Serial Audio Input/Output Pin Description

L/R: Front channel, C/SW: Center channel and Sub woofer, SL/SR: Surround channel.

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The NJU26220 has a pair of bit clock lines (BCKI and BCKO) and a pair of left/right clock lines (LRI and LRO). The clock inputs BCKI and LRI are used to accept timing signals from an external device when the NJU26220 operates in SLAVE mode.

The clock outputs BCKO and LRO are provided for delta-sigma A/D and D/A converters when the NJU26220 operates in MASTER mode. In SLAVE mode, the output of BCKO and LRO are the buffered output of BCKI and LRI.

The MCK always generates the system clock supplied to the NJU26220 expect RESET sequence.





#### Host Interface 2.

The NJU26220 can be controlled via Serial Host Interface (SHI) using either of two serial bus format: I<sup>2</sup>C bus or 4-Wire serial bus. Data transfers are in 8 bit packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The SEL pin controls the serial bus mode. When the SEL is low during the NJU26220 initialization, I<sup>2</sup>C bus is available. When the SEL is high during the NJU26220 initialization, 4-Wire serial bus is available.

		enace Fin Description	
Pin No.	Symbol		
	(I <sup>2</sup> C / Serial)	I <sup>2</sup> C bus Format	4-Wire Serial bus Format
27	SCL/SCK	Serial Clock	Serial Clock
28	SDA/SDOUT	Serial Data	Serial Data Output
25	AD1/SDIN	I <sup>2</sup> C bus address Bit1	Serial Data Input
26	AD2/SSb	I <sup>2</sup> C bus address Bit2	SLAVE Select

Table 3	Serial Host Interface Pin Description
I adie J	Scharting internate Fill Description

Note: When I<sup>2</sup>C is selected, SDA/SDOUT pin is a bi-directional open drain. SDA/SDOUT pin, which is assigned for I<sup>2</sup>C, requires a pull-up resister. When 4-Wire Serial bus is selected, SDA/SDOUT pin is CMOS output.

#### 2.1 I<sup>2</sup>C Bus

When the NJU26220 is configured for I<sup>2</sup>C bus communication in SEL="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistor. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. This offers additional flexibility in a system design by offering two different possible SLAVE addresses for which the NJU26220 will respond to.

An address can be arbitrarily set up with an internal setup and these AD1/AD2 pins.

		Ta	able 4 l <sup>4</sup>	C Bus SL	AVE Add	ress		
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	0	0	1	1	1	AD2*1	AD1*1	R/W
*,	1 SL	AVE addre	ess is 0 whe	n AD1 is "L	ow". SLAVE	E address is	3 1 when AD	D1 is "Hiah".

SLAVE address is 0 when AD1 is "Low". SLAVE address is 1 when AD1 is "High".

The figure on the following shows the basic timing relationships for transfers. A transfer is initiated with a START condition, followed by the SLAVE address byte. The SLAVE address consists of the seven-bit SLAVE address followed by a read/write (R/W) bit. When an address with an effective serial host interface is detected, the acknowledgement bit which sets a SDA line to "Low" in the ninth bit clock cycle is returned.

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The R/W bit in the SLAVE address byte sets the direction of data transmission until a STOP condition terminates the transfer. R/W = "Low" indicates the host will send to the NJU26220 while R/W = "High" indicates the host will receive data from the NJU26220.



Fig. 5 I<sup>2</sup>C Bus Format

The serial host interface supports "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" I<sup>2</sup>C bus data transfer.

#### 2.2 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL="High" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb="Low". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte(MSB) which is latched on the falling transitions of SSb. SDOUT is always CMOS output. SDOUT does not require a pull-up resistor.

#### 3. Pin setting

The NJU26220 operates default command setting after resetting the NJU26220. In addition, the NJU26220 restricts operation at power on by setting PROC pin and MUTEb pin. These pins are input pin. However, these pins operate as bi-directional pins when test for internal. Connect with VDDIO or VSSIO through 3.3k-ohm resistance.

Pin	Setting	Function		
PROC	HIGH	The NJU26220 operates default setting after reset.		
	LOW	The NJU26220 does not operate after reset. Sending start command		
		is required for starting operation.		
MUTEb	HIGH	Master volume is set 0dB after reset.		
	LOW	Master volume is set mute after reset.		

Table 5 The function of a functional setting bin	Table 5	The function of a functional setting pin
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#### 4 Watchdog Clock

The NJU26220 outputs clock pulse through WDC (Pin No.8) during normal operation. The WDC clock is useful to check the status of the NJU26220 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26220. When the WDC clock pulse is lost or not normal clock cycle, the NJU26220 does not operate correctly. Then reset the NJU26220 and set up the NJU26220 again.

The WDC pin is open drain output. Connect with VDDIO through 3.3k-ohm resistance when WDC is useful. Connect with VSSIO through 3.3k-ohm resistance when WDC is not useful. Do not open WDC pin.

Note: The cycle of WDC output is rough. Because WDC output inserts in the process of sound processing. In slave mode, when there is no input of BCKI/LRI, WDC can not output. It is required to set up a sampling rate correctly.

#### NJU26220 Command Table 5.

Host processor can control the NJU26220 via I<sup>2</sup>C bus interface or 4-Wire serial bus. The following table summarizes the available user commands.

No.	Command	Command Description
1	SET_TASK_CMD	Decode Mode: Pro Logic II, Dolby Virtual Speaker, Dolby Headphone,
		Pink Noise Generator, Downmix, Delay select, LFE Generator
2	PRO2MODE_CMD	Mode setting: Pro Logic II (Movie, Music etc.,), Panorama mode
3	PRO2CDCFG_CMD	Dimension setting, Center Width Control
4	PRO2FLAGS_CMD	Mode setting: Auto Balance, 3 stereo, Phantom Center etc.,
5	DVS_DH_CMD	DVS/DH select, DVS output speaker layout, DVS/DH output mode
6	SAMPLERATE_CMD	32.0kHz, 44.1kHz, 48.0kHz
7	PNG_MODE_CMD	Pink Noise Generator output channel configuration
8	DELAY_CMD	Delay time at Center and Surround Channel
9	GAIN_CMD	Each Channel Trimmer
10	SYSTEM_STATE_CMD	Serial audio interface format, Clock, Master/Slave
11	WATCHDOG_CMD	Watchdog Clock interval
12	SMOOTH_CMD	Smooth Control time
13	OUTPUT_SEL_CMD	Output select
14	LFE_CONFIG_CMD	LFE cutoff frequency select
15	REINIT_CMD	Re-initialization command
16	SOFTWARE_RESET_CMD	Software RESET
17	START_CMD	Start Command at Power on
18	NOP_CMD	NOP command

#### License

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[CAUTION]