Ordering number : ENA1345A

SANYO Semiconductors
DATA SHEET

CMOS IC

LC07410LG — Monaural CODEC + Audio I/F + Video Driver

Overview

The LC07410LG is an IC that integrates a video driver with audio CODEC developed for digital still cameras and other portable equipment. Incorporating 16-bit A/D and D/A converters as well as a microphone amplifier and speaker driver that are necessary for audio recording and playback, the one-chip IC is ideal for use to create audio interfaces.

Functions

■ Audio Block

- ΔΣ method 16-bit monaural A/D and D/A converters
- Generates bias voltage (2.3V) for microphone
- Supports microphone amplifier
  differential inputs (0/+20/+26dB)
- Amplifier with automatic level control (ALC)
  (-14dB to +34dB) for recording system
- Wind cut HPF
- Two programmable digital filter
  HSF/Notch filter/LPF/EQ
- Digital volume with
  automatic level control (ALC) for playback system
  Supports zerocross detection and soft switching
- Line output
  On-chip MUTE and POP-noise suppression circuits
- Speaker driver
  Supports $V_{DD}S$ = 5V (piezoelectric speaker supported)
  BTL drive, rated output of 350mW at 8Ω, $V_{DD}S$ = 3V
  1W at 8Ω, $V_{DD}S$ = 5V
  Idling current adjustable
  Supports BEEP input, volume level switchable
- Audio interfaces
  I^2S, Left-justified mode, Right-justified mode
- PLL
  Input: 12MHz, 13.5MHz, 24MHz, 27MHz
  Sampling frequency: 7.86kHz to 48kHz
  PLL master mode/slave (EXT) mode
- Loopback: ADOUT to DAIN switch incorporated

■ Video Block

- DC direct coupling input/output
- Built-in 6th order low-pass filter (fc = 7.5MHz)
- Amplifier gain selectable (6dB or 12dB)
- Drive capacity 75Ω, 1 system

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■ REG Block

- 3.0V output linear regulator for Audio Block
- Overcurrent protective function (typ: 200mA)
- Quick discharge activity
- 3-line serial register control
- Digital I/O 1.8V supported

- Supply voltage
  $V_{DD}IO$ = 1.8V/3.3V (1.71 to 3.6V)
  $V_{DD}A$ = $V_{DD}P$ =3 .0V (2.7 to 3.6V)
  $V_{DD}R$ = 3.3V (3.2 to 3.6V)
  $V_{DD}V$ = DV_{DD} = 3.3V (2.7 to 3.6V)
  $V_{DD}S$ = 3.3/5V (2.7 to 5.5V)
- Operating ambient temperature: -20 to +80°C

Function comparison table of LC07410 and LC074146

Function	LC07410	LC074146
Logic I/O 1.8V accepted	○	×
3V Regulator	○	×
BEEP sound generator	○	×
PLL frequencies	flexible	Pre-fix
EXT-BEEP GAIN	0dB, -15/-18/-21dB	-12/-15/-18/-21dB
ALC attack speed	2step variable	monotonic
ALC recovery speed	3step variable	monotonic
ALC noise gate function	○	×
Digital filters	Wind cut HPF +2 programmable filters	Wind cut HPF + EQ (HSF) + Notch

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (5V system)	$V_{DD}5$ max	$V_{DD}S$	-0.3 to 7.0	V
Maximum supply voltage (3V system)	$V_{DD}3$ max	Other than $V_{DD}S$	-0.3 to 4.0	V
Input voltage	V_{IN} max		-0.3 to 4.0	V
Output voltage	V_{OUT} max		-0.3 to 4.0	V
Input/output voltage	V_{IO} max		-0.3 to 4.0	V
Allowable operating voltage range	V_{DD}SRANGE	$V_{DD}S$	2.7 to 5.5	V
	V_{DD}RRANGE	$V_{DD}R$	3.2 to 3.6	V
	V_{DD}ARANGE	$V_{DD}A$, $V_{DD}P$, $V_{DD}V$, DV_{DD}	2.7 to 3.6	V
	V_{DD}IORANGE	$V_{DD}IO$	1.71 to 3.6	V
Allowable power dissipation	Pd max	Ta = 80°C *	500	mW
Operating ambient temperature	Topr		-20 to +80	°C
Storage ambient temperature	Tstg		-55 to +125	°C

* Mounted on a specified board: 40mm×50mm×0.8mm, glass epoxy board 2S2P (4-layer board)

Recommended Operating Range at Ta = 25°C, $V_{SS}V = DV_{SS} = V_{SS}R = V_{SS}A = 0V$

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage	$V_{DD}IO$	$V_{DD}IO$ pin	1.71	3.3	3.6	V
	DV_{DD}	DV_{DD} pin	2.7	3.3	3.6	V
	$V_{DD}ana$	$V_{DD}P$, $V_{DD}A$ pin	2.7	3.0	3.6	V
	$V_{DD}V$	$V_{DD}V$ pin	2.7	3.3	3.6	V
	$V_{DD}R$	$V_{DD}R$	3.2	3.3	3.6	V
	$V_{DD}S$	$V_{DD}S$ pin	2.7	3.3/5.0	5.5	V
Supply voltage gap	$V_{DD}DV$	DV_{DD}-$V_{DD}V$			0.3	V
	$V_{DD}DR$	DV_{DD}-$V_{DD}R$			0.3	V
	$V_{DD}ID$	$V_{DD}IO$-DV_{DD}			0.3	V
	$V_{DD}PR$	$V_{DD}P$-$V_{DD}R$			0.3	V
	$V_{DD}PA$	$V_{DD}P$-$V_{DD}A$			0.3	V
	$V_{DD}AS$	$V_{DD}A$-$V_{DD}S$			0.3	V
	$V_{DD}VS$	$V_{DD}V$-$V_{DD}S$			0.3	V
Inpupt high level voltage	V_{IH}	(*1)	0.8×$V_{DD}IO$		$V_{DD}IO$	V
Input low level voltage	V_{IL}	(*1)	DV_{SS}		0.2×$V_{DD}IO$	V
Input clock frequency	fMCLK	MCLKIN pin	2.012		27	MHz
Input clock duty	DutyMCLK	MCLKIN pin	0.45	0.50	0.55	%

(*1) Applicable pins: PDNB, CSB, SCK, SDA, TESTIN, DAIN, MCLKIN, BCLK, LRLK (in input mode)

Electrical Characteristics at Ta = 25±2°C, $V_{DD}IO$ = 1.71 to 3.6V, $V_{DD}A = V_{DD}P = V_{DD}V = DV_{DD}$ = 2.7 to 3.6V, $V_{DD}R$ = 3.2 to 3.6V, $V_{SS}S$ = 2.7 to 5.5V, $V_{SS}V = DV_{SS} = V_{SS}R = V_{SS}A = 0V$

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Input high level current	I_{IH}	$V_I = V_{DD}IO$ (*1)			+1	μA
Inputp low level current	I_{IL}	$V_I = DV_{SS}$ (*1)	-1			μA
Output high level voltage	$V_{OH}1$	I_{OH} = -1mA (*2)	0.8×$V_{DD}IO$			V
Output low level voltage	$V_{OL}1$	I_{OL} = 1mA (*2)			0.2×$V_{DD}IO$	V

(*1) Applicable pins: PDNB, CSB, SCK, SDA, TESTIN, DAIN, MCLKIN, BCLK, LRCK (in input mode)

(*2) Applicable pins: ADOUT, BCLK, LRCK (in output mode)

Analog Characteristics at Ta = 25°C, $V_{DD}A = V_{DD}P$ = 3.0V, $V_{DD}IO = DV_{DD} = V_{DD}S = V_{DD}V = V_{DD}R$ = 3.3V, fs=48kHz

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Current drain						
REC time	$I_{DD}RA1$	REG/PLL/MIC/PGA/ADC on, no input signal	9.0	13.8	18.0	mA
PB (LINE) time	$I_{DD}PA2$	REG/PLL/DAC/LINE on, no input signal	8.0	12.2	16.0	mA
PB (SPK) time	$I_{DD}PA3$	REG/PLL/DAC/SPK on, no input signal	11.0	15.2	21.0	mA
Video block 1	$I_{DD}V1$	$V_{DD}V$, no input signal	4.0	6.1	8.0	mA
Video block 2	$I_{DD}V2$	$V_{DD}V$, Video in = white 50%	8.0	12.8	16.0	mA
Power down time current	$I_{DD}PD$	$V_{DD}A$+$V_{DD}P$+$V_{DD}R$+$V_{DD}S$+$V_{DD}V$+DV_{DD}+$V_{DD}IO$, clock stopped		1.0	10	μA
MIC						
MIC amplifier gain	$V_G$mic	V_{IN} = -30dBV, 1kHz, MGAIN[1:0] = 01	-1	0	1	dB
		V_{IN} = -30dBV, 1kHz, MGAIN[1:0] = 10	19	20	21	dB
		V_{IN} = -30dBV, 1kHz, MGAIN[1:0] = 11	25	26	27	
MIC amplifier output THD+N	THDNmic	V_{IN} = -30dBV, 1kHz, MGAIN[1:0] = 11		-80	-70	dB
MIC amplifier output noise voltage	V_{NO}mic	MIC IN no signal, A-weighted, MGAIN[1:0] = 11		-88	-82	dBV
MIC bias output voltage	Vmicpwr	R_L = 5kΩ	2.2	2.3	2.4	V

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Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
ALC						
Gain change	DGalc			1		dB
Gain control range	VGalc		-14		+34	dB
ADC: ALCIN input, ALCOFF, PGA Gain = 0dB						
Analog input voltage	Vinad	0dBFS, 1kHz		$0.6\times V_{DD}A$		Vp-p
THD+N	THDNad	-1dBFS, 1kHz		-80	-74	dB
Dynamic range	DRad	-60dBFS, A-weighted	80	86		dB
S/N ratio	SNad	ALCIN no signal, A-weighted	80	86		dB
DAC						
Digital volume change	DGvol1	+12dB to -10dB		0.5		dB
	DGvol2	-11dB to -42dB		1		dB
	DGvol3	-44dB to -64dB		2		dB
LINE: DAC→LINE Gain = 0dB, DVOL = 0dB						
Analog output voltage	Voutda	0dBFS, 1kHz		$0.6\times V_{DD}A$		Vp-p
THD+N	THDNda	0dBFS, 1kHz		-83	-74	dB
Dynamic range	DRda	-60dBFS, A-weighted	80	88		dB
S/N ratio	SNda	A-weighted	80	88		dB
SPK						
SPK amplifier gain	VGsp	SPKIN = -9dBV, 1kHz , BTL, R_L = 8Ω	11	12	13	dB
SPK output distortion	HDsp	SPKIN = -9dBV, 1kHz		0.2	1	%
SPK output noise voltage	VNOsp	SPKIN no signal, R_L = 8Ω		-86	-80	dBV
SPK maximum rated output	VOMsp	R_L = 8Ω, THD = 3%	300	350		mW
BEEP gain	VGbp	BTL, R_L=8Ω BPVOL[1:0] = 00	-2	0	2	dB
		BTL, R_L = 8Ω BPVOL[1:0] = 01	-16	-15	-14	dB
		BTL, R_L = 8Ω BPVOL[1:0] = 10	-19	-18	-17	dB
		BTL, R_L = 8Ω BPVOL[1:0] = 11	-22	-21	-20	dB
Regulator						
Regulator output voltage	$V_O$reg	I_{OUT} = 20mA	2.9	3.0	3.1	V
Video driver						
Video amplifier gain	$V_G$video	VGAIN[1:0] = 00, VDIN = 1Vp-p 100% white	5	6	7	dB
		VGAIN[1:0] = 10, VDIN = 0.5Vp-p 100% white	11	12	13	dB
Frequency characteristics	Fva	f = 8MHz/100kHz		-4.5	0	dB
		f = 20MHz/100kHz		-40	-35	dB
Input impedance	Rvin		100	120		kΩ

ADC Filter Characteristics

Parameter	Conditions	Ratings			unit	Remarks
		min	typ	max		
Resolution			16		Bit	
Passband	±0.045dB	0		0.4535fs		21.8kHz@fs = 48kHz
Stopband		0.5465fs				26.2kHz@fs = 48kHz
Passband ripple	0 to 20kHz			±0.045	dB	
Stopband attenuation		-69			dB	
Output data delay			58		1/fs	
HPF cutoff frequency	-3dB		0.0000385fs		Hz	1.85Hz@fs = 48kHz

DAC Filter Characteristics

Parameter	Conditions	Ratings			unit	Remarks
		min	typ	max		
Resolution			16		Bit	
Passband	±0.015dB	0		0.4535fs		21.8kHz@fs = 48kHz
Stopband		0.5465fs				26.2kHz@fs = 48kHz
Passband ripple				±0.015	dB	
Stopband attenuation		-63			dB	
Output data delay			48		1/fs	
HPF cutoff frequency	-3dB		0.0000385fs		Hz	1.85Hz@fs = 48kHz

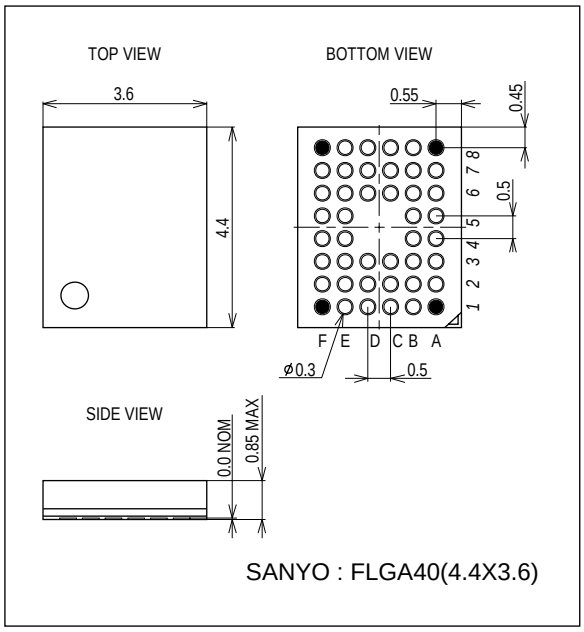
Switching Characteristics

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
PLL						
CKIN frequency	fCKI	PLL used	12		27	MHz
		EXT input present	2.012		24.576	MHz
BCLK frequency	fBCK	FBCLK = 0		64fs		
		FBCLK = 1		32fs		
BCLK duty cycle	dtBK		45	50	55	%
LRCK frequency	fLR		7.86		48	kHz
LRCK duty cycle	dtLR		45	50	55	%
CLK transition time ↑	trCK	Rise time, MCLKIN/BCLK/LRCK inputs present			10	ns
CLK transition time ↓	tfCK	Fall time, MCLKIN/BCLK/LRCK inputs present			10	ns

Package Dimensions

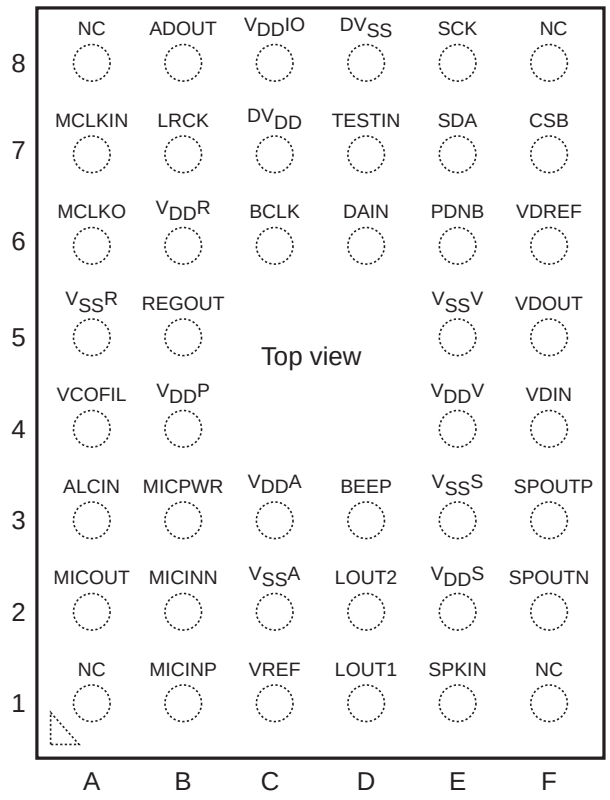
unit : mm (typ)

3370

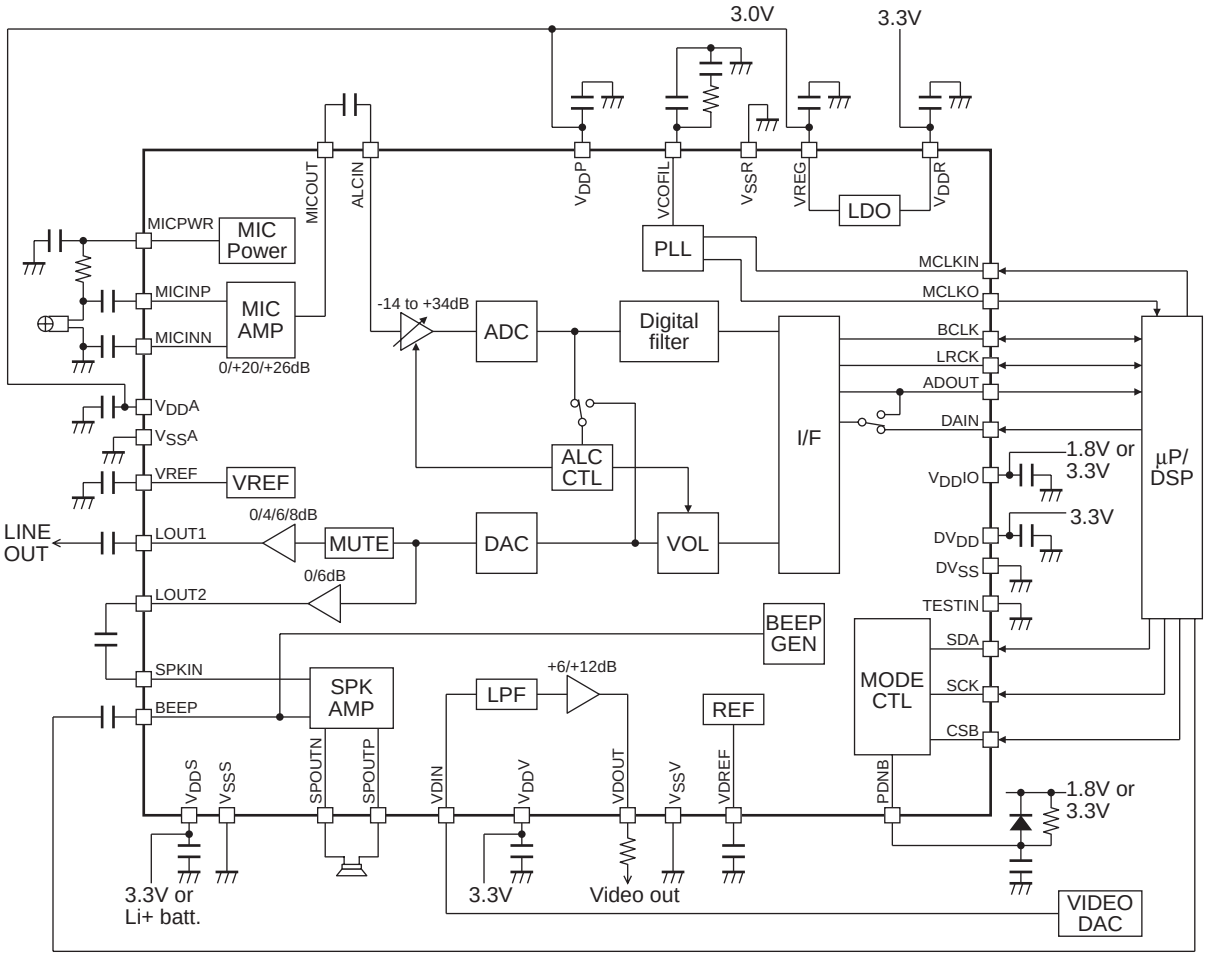


SANYO : FLGA40(4.4X3.6)

Pin Assignment

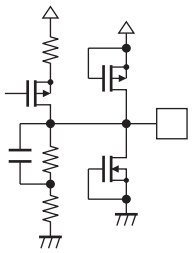
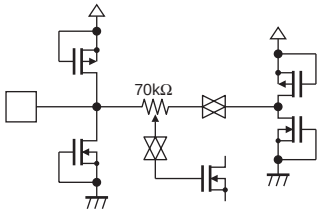
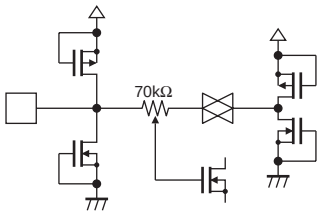
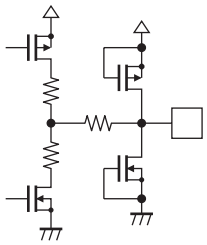
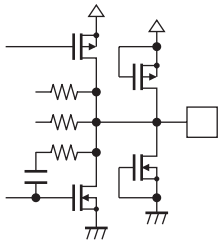
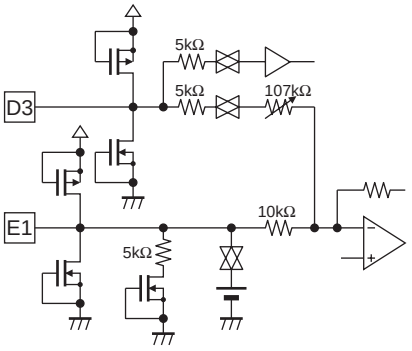


Block Diagram



Pin Function

(Note) I/O: I => input, Is => Schmitt input, O => output, IO s=> Schmitt input/output

Pin No.	Pin name	I/O	Function	Equivalent circuit
B3	MICPWR	O	Microphone power supply output (2.3V)	
B1	MICINP	I	Microphone amplifier input (+ side)	
B2	MICINN	I	Microphone amplifier input (- side)	
C3	$V_{DD}A$	–	Analog block power supply (3V)	
C1	VREF	O	3V analog power supply reference voltage output	
C2	$V_{SS}A$	–	Analog block ground (0V)	
D1	LOUT1	O	Line output 1	
D2	LOUT2	O	Line output 2	
D3	BEEP	I	BEEP signal input, mixed to speaker amplifier	
E1	SPKIN	I	Speaker amplifier input	

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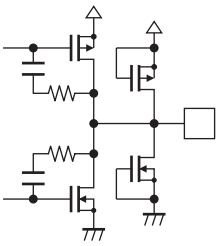
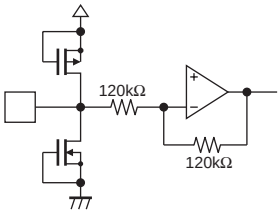
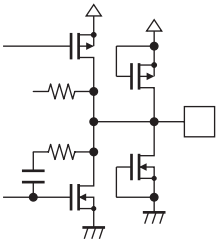
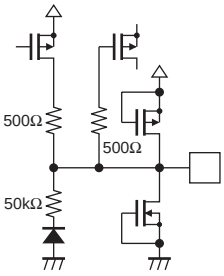
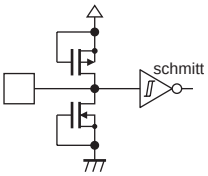
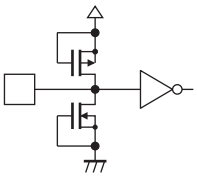
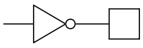
Pin No.	Pin name	I/O	Function	Equivalent circuit
E2	$V_{DD}S$	–	Speaker analog power supply	
F2	SPOUTN	O	Speaker output (-)	
F3	SPOUTP	O	Speaker output (+)	
E3	$V_{SS}S$	–	Speaker analog ground	
E4	$V_{DD}V$	–	Video driver analog power supply	
F4	VDIN	I	Video signal input	
F5	VDOUT	O	Video signal output	
F6	VDREF	O	Video VREF	
E5	$V_{SS}V$	–	Video driver ground	
E6	PDNB	Is	Reset (negative polarity)	
F7	CSB	Is	Chip select (negative polarity) Microcontroller IF	
E8	SCK	Is	Serial clock Microcontroller IF	
E7	SDA	Is	Serial data input Microcontroller IF	
D8	DV_{SS}	–	Digital ground (0V)	
C7	DV_{DD}	–	Digital power supply (3.3V)	
C8	$V_{DD}IO$	–	Digital I/O power supply (3.3V/1.8V)	
D7	TESTIN	I	Test input (V_{SS} fixed in normal operation)	
D6	DAIN	I	DAC serial data input	
B8	ADOUT	O	ADC serial data output	

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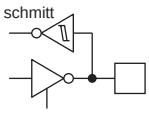
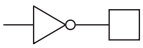
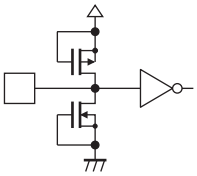
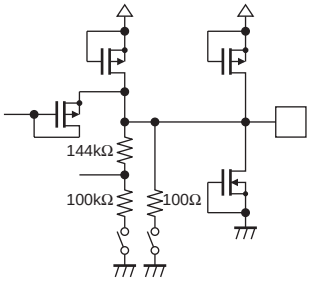
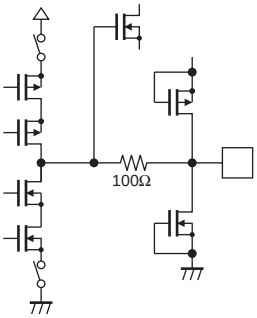
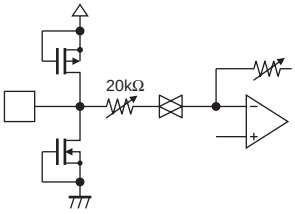
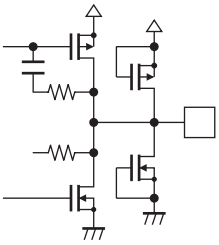
Pin No.	Pin name	I/O	Function	Equivalent circuit
B7	LRCK	IOs	LR clock input	
C6	BCLK	IOs	Bit clock input	
A6	MCLKO	O	Master clock output (Default: Set to Low, serial setting enables output/Addr: 16h)	
A7	MCLKIN	I	Master clock input	
B6	$V_{DD}R$	–	Regulator power supply input (3.3V)	
B5	REGOUT	O	Regulator output pin	
A5	$V_{SS}R$	–	Regulator block ground	
A4	VCOFIL	O	VCO filter pin	
B4	$V_{DD}P$	–	PLL block supply (3.0V)	
A3	ALCIN	I	ALC amplifier input	
A2	MICOUT	O	Microphone amplifier output	

Interface Timing Characteristics

Parameter	Symbol	Ratings			unit
		min	typ	max	
Microcontroller serial interface timing					
SCLK cycle time	tCYC	4T	8T		ns
SCLK high period	tSH	2T	4T		ns
SCLK low period	tSL	2T	4T		ns
Data setup time	tSU	2T	4T		ns
Data hold time	tHD	2T	4T		ns
CSX rise to SCLK wait time	tWSCLK	0T	2T		ns
SCLK to CSX rise wait time	tWCSX	4T	6T		ns
Rise time	tSR			50	ns
Fall time	tSF			50	ns
Audio data timing					
Clock phase (Note 2)	tPH	75			ns
Clock phase (Note 3)	tPH		1/(128fs)		ns
Data delay time	tDD	0		75	ns
Data setup time	tSUA	1T			ns
Data hold time	tHDA	1T			ns

Note 1: T = 1/fMCLK, fMCLK: Frequency of MCLKIN pin; example: when fMCLK = 10MHz, T = 100ns, 2T = 200ns

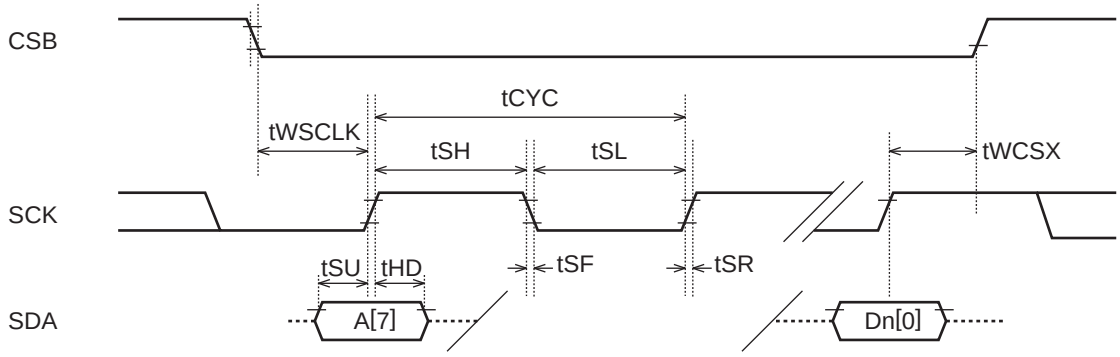
Note 2: LRCK and BCLK are inputs in Slave mode.

The MCLK timing needs only to be synchronized with LRCK and BCLK and its phase is irrelevant.

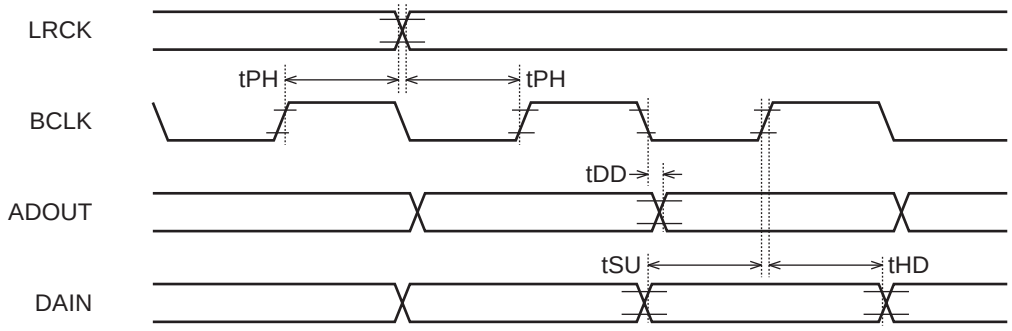
Note 3: In master mode, LRCK and BCLK are output in master mode and fs is the sampling frequency.

Note 4: The load of output pin: 30pF.

Microcontroller Serial Interface Timing Diagram

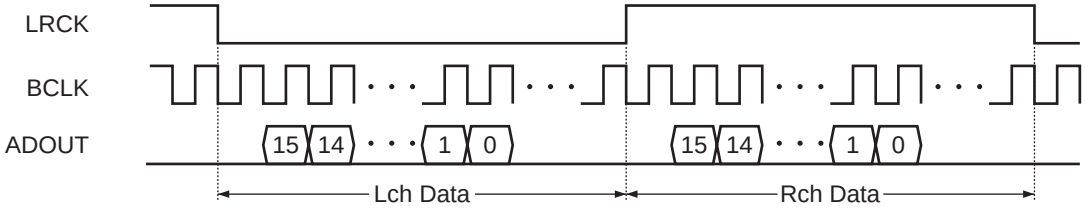


Audio Data Timing Diagram

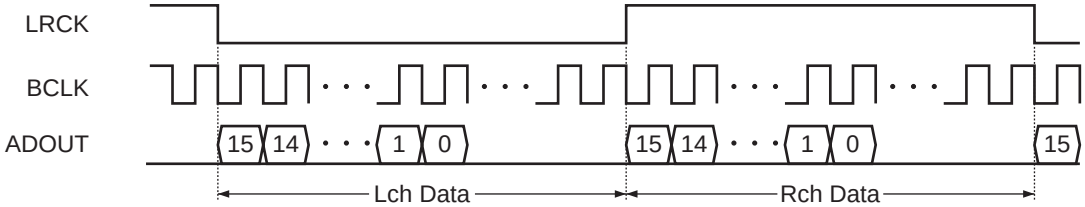


Audio Data Formats

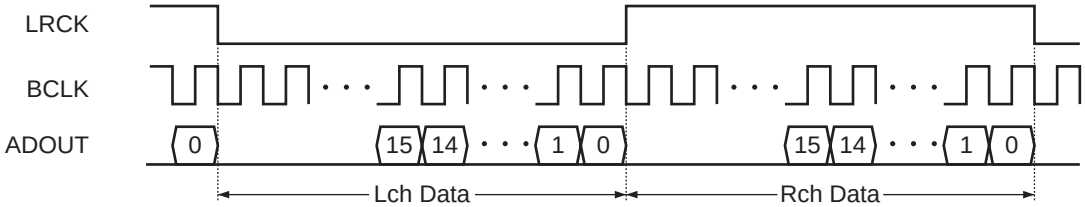
• I^2S mode



• Left-justified mode



• Right-justified mode



PLL/BCLK/LRCK Master/Slave

Pin No.	Pin Name	Slave Mode (PLL: OFF)	Master Mode (PLL: ON)
A7	MCLKIN	Input	Input
A6	MCLKO	Output (through)	Output (PLL = 256fs)

Pin No.	Pin Name	Slave Mode (ADF_MASTER = 0)	Master Mode (ADF_MASTER = 1)
B7	LRCK	Input	Output
C6	BCLK	Input	Output

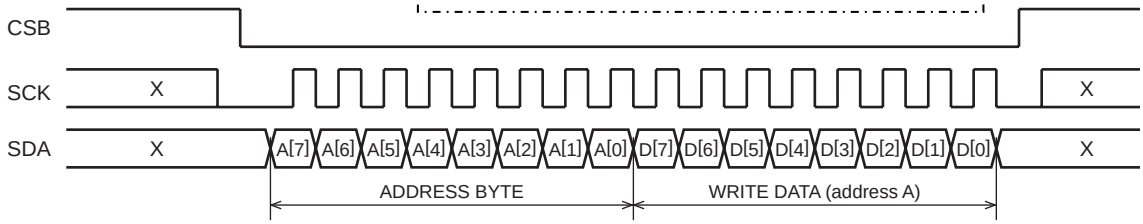
Microcontroller Serial Interface

The internal registers values are written by the serial interface consisting of the three CSB, SCK, and SDA lines. When the CSB pin is set low, the LC07410LG is switched into the mode that enables operation. The data is received on a byte basis with MSB first.

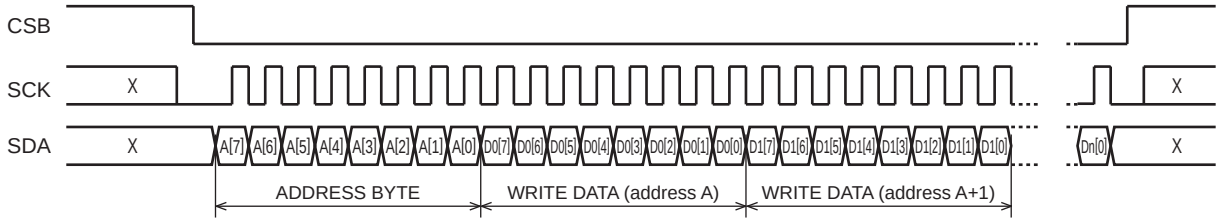
Continuous access (burst access) is also possible, and the addresses incremented by 1 are accessed in sequence with each byte following access to the register specified by the address byte. If the size of data exceeding the highest address (39h) is accessed in this process, the data concerned is treated as invalid. In other word, the address never wraps around to 00h.

Transferring data to one address

A[7:0] : Designated address
D[7:0] : Register data
X : Invalid



Transferring data to contiguous addresses



Specification Details

• Power down/system reset

When the PDNB pin is set to 0, all the circuits are set to power down mode regardless of the power down settings for each block. A 0 on the PDNB pin also triggers a system reset.
After the power is first applied, the system must be reset without fail.
[See the section on "Checkpoint_2) Resetting"]
After resetting, the contents of the serial port register are initialized.
The VREF buffer is activated by releasing power down mode by setting the PDNB pin from 0 to 1, and then by setting VREF_BIAS[1:0] to 01. When VREF_BIAS [1:0] is set to 10, VREF starts. Along with the start of VREF, the LINE output pin is biased to $1/2V_{DD}A$. Once the VREF voltage has stabilized, VREF_BIAS [1:0] must be set to 11 (normal state).

Reference voltage generator circuit

VREF_BIAS: Voltage Reference Bias * Bold letters indicate initial settings.

ADRS	Bit	Name	Init	Description
01h	[5:4]	VREF_BIAS	00b	Sets the reference voltage circuit (VREF pin). 11: Normal operation (standard resistor value) 10: Quick rise to reference voltage <*1> 01: Activates IREF bias, VREF OFF **00: Power down**

<*1> The target voltage is reached quickly by connecting a low-resistance element in the "reference voltage generation circuit." During normal operation, a standard resistance is recommended in order to save power.

Power Control

ADRS	Bit	Name	Init	Description
00h	[7]	MIC_PDX	0b	MIC amplifier circuit, power control 1: power on **0: power down**
	[6]	MIC_PWR_PDX	0b	MIC power circuit (MIC_PWR pin), power control 1: power on **0: power down**
	[5]	PGA_PDX	0b	PGA circuit, power control 1: power on **0: power down**
	[4]	ADC_PDX	0b	ADC circuit, power control 1: power on **0: power down**
	[3]	DAC_PDX	0b	DAC circuit, power control 1: power on **0: power down**
	[2]	SEL_PDX	0b	Selector ($L_{OUT}2$) circuit, power control 1: power on **0: power down**
	[1]	LO_PDX	0b	Line out circuit ($L_{OUT}1$) circuit, power control 1: power on **0: power down**
	[0]	SP_PDX	0b	Speaker amplifier circuit, power control 1: power on **0: power down**
01h	[2]	PLL_PDX	0b	PLL circuit, power control 1: power on **0: power down** (PLL-EXT mode)
	[1]	REG_PDX	0b	Regulator circuit, power control 1: power on **0: power down**
	[0]	VD_PDX	0b	Video driver circuit, power control 1: power on **0: power down**

Sampling Frequency Setting

Set sampling frequency used by FS [4:0] register. This is necessary to make it for correctly setting digital frequency characteristic and ALC damping time constant. The setting is adjusted to a value that is the closest to fs used.

ADRS	Bit	Name	Init	Description
15h	[3:0]	FS	1000b	Sampling Frequency Setting **1000: 48kHz**/0111: 44.1kHz/0110: 32kHz/0101: 24kHz 0100: 22.05kHz/0011: 16kHz/0010: 12kHz/0001: 11.025kHz 0000: 8kHz

Note: This setting doesn't synchronize with PLL setting. It is necessary to set it individually respectively.
Refer to the page of PLL function explanation for PLL setting.

- **3V Regulator**

Built-in 3V Regulator for $V_{DD}A$,$V_{DD}P$.
The regulator starts by setting as REG_PDX = 1.
Output current is 100mA (typ).
It provides with max 200mA (typ) output current limiter for over-current protective function.

- **Microphone (MIC) amplifier**

The microphone amplifier has a differential input and a gain of +26dB (typ).
Its gain can also be set to +20dB or 0dB by register MGAIN [1:0]. Its input resistance is 70kΩ (typ). The MICPWR is a power output pin for the microphone, and its output voltage is 2.3V (typ 0.767×$V_{DD}A$).
The maximum output current is 20mA.
The microphone amplifier is placed in the power down mode by setting MIC_PDX to 0.
When MIC_PWR_PDX is set to 0, the microphone power supply circuit is placed in the power down mode.

ADRS	Bit	Name	Init	Description
02h	[5:4]	MIC_GAIN	01b	MIC amplifier circuit, gain setting 11: 26dB 10: 20dB **01: 0dB** 00: 0dB

- **Recording system automatic level control (ALC)**

The amplifier gain of the PGA (Programmable Gain Amplifier) must be automatically adjusted so that the A/D converter output audio level is setup to the predetermined value. The gain can be varied within a range (maximum) of -14dB to +34dB.
When using ALC in the recording system, set REC_ALC to 1 and PB_ALC to 0 (recording system ALC mode).
When REC_ALC is set to 0 and PB_ALC is set to 0 (ALC off mode), the PGA is placed in the manual mode, and the amplifier gain is fixed to the value of the ALC_GAIN register setting.
When PGA_PDX is set to 0, the PGA is placed in the power down mode. During normal use, the state of PGA_PDX must be switched at the same time as ADC_PDX.
For further details on operation, refer to "Description of ALC/limiter (Automatic Level Control) operation."
Any of eight recording ALC levels (in 1dB steps from -3dBFS to -10dBFS) can be set using the ALC_VAL register.

ADRS	Bit	Name	Init	Description
03h	[6:4]	ALC_VAL	001b	Set the ALC limiter level 000: -3dBFS **001: -4dBFS** 010: -5dBFS 011: -6dBFS 100: -7dBFS 101: -8dBFS 110: -9dBFS 111: -10dBFS
	[2:0]	ALC_FA1	010b	Attack coefficient 1 setting
04h	[6:4]	ALC_THA	010b	Set the attack speed switch over thresh
	[2:0]	ALC_FA2	100b	Attack coefficient 2 setting
05h	[6:4]	ALC_THR1	011b	Set the recovery speed switch over thresh1
	[2:0]	ALC_FR1	100b	Recovery coefficient 1 setting
06h	[6:4]	ALC_THR2	011b	Set the recovery speed switch over thresh2
	[2:0]	ALC_FR2	100b	Recovery coefficient 2 setting
07h	[2:0]	ALC_FR3	100b	Recovery coefficient 3 setting
08h	[7]	ALC_FULLEN	0b	Sets the full scale detection mode 1: Performs attack operation regardless of the ALCZCD setting when a full scale is detected. **0: Normal operation**
	[6]	ALC_ZCD	1b	Controls the gain change operation at zerocross timing. **1: Changes the gain at zerocross timing.** 0: Changes the gain without waiting for a zerocross timing.
	[5:4]	ALC_ZCDTM	01b	Set the zerocross detection timeout time. Valid when [ALC_ZCD] = 1. 11: 8192/fs 10: 4096/fs **01: 2048/fs** 00: 1024/fs * It becomes the above-mentioned 1/4 times at fs 8k to12kHz, It becomes the above-mentioned 1/2 times at fs 16k to 24kHz.
	[3:2]	ALC_TLIM	01b	Set the inter-zerocross attack limit. 11: 4dB 10: 2dB **01: 1dB** 00: 0.5dB Valid when [ALC_ZCD] = 1
	[1:0]	ALC_RWT	10b	Set the recovery alert time 11: 1024/fs **10: 512/fs** 01: 256/fs 00: 128/fs * It becomes the above-mentioned 1/4 times at fs 8k to 12kHz, It becomes the above-mentioned 1/2 times at fs 16k to 24kHz.

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ADRS	Bit	Name	Init	Description
09h	[7]	ALC_NGEN	0b	Set the noise gate function 1: Valid **0: Invalid**
	[6:4]	ALC_NGTH	100b	Set the noise gate silent detection thresh level
	[3:2]	ALC_NGDT	10b	Set the noise gate silent detection time/See the gain attenuation time
	[1:0]	ALC_NGRT	01b	Set the noise gate reset time
0Bh	[5:0]	ALC_VMAX	0Eh	Set the maximum PGA gain value (Init value = 0Eh: 0dB) Refer to “ALC Circuit Gain Setting Table.”
0Ch	[5:0]	ALC_GAIN	0Eh	Set the manual mode PGA gain value (Init value = 0Eh: 0dB) Refer to “ALC Circuit Gain Setting Table.”
0Dh	[1:0]	REC_ALC PB_ALC	10b	ALC mode setting **10: REC ALC, PB manual gain setting** 01: PB ALC, REC manual gain setting 00/11: ALC OFF, REC/PB manual gain setting

See the section on "Description of ALC Operation."

• Attack coefficient 1

FA1[2:0]	1dB Attenuation time*	fs = 48kHz 24kHz 12kHz
000	1/fs	20.83μs
001	2/fs	41.67μs
010	**4/fs**	**83.33μs**
011	8/fs	166.7μs
100	16/fs	333.3μs
101	32/fs	666.6μs
110	64/fs	1.333ms
111	128/fs	2.666ms

• Attack coefficient 2

FA2[2:0]	1dB Attenuation time*	fs = 48kHz 24kHz 12kHz
000	1/fs	20.83μs
001	2/fs	41.67μs
010	4/fs	83.33μs
011	8/fs	166.7μs
100	**2^9/fs**	**10.66ms**
101	2^{10}/fs	21.33ms
110	2^{11}/fs	42.67ms
111	2^{12}/fs	85.33ms

* At fs = 32k to 48kHz setting. 1/4 times at 8k to 12kHz, 1/2 times at 16k to 24kHz (48kHz, 24kHz, 12kHz become the same speed).

• Attack speed switch over thresh level

THA[2:0]	Level to ALC_VAL
000	+1dB
001	+2dB
010	**+3dB**
011	+4dB
100	+5dB
101	+6dB
110	+7dB
111	+8dB

• Recovery coefficient 1

FR1[2:0]	FS/s*
000	13.2
001	6.6
010	3.3
011	1.65
100	**0.828**
101	0.424
110	0.212
111	0.106

• Recovery coefficient 2

FR2[2:0]	FS/s*
000	3.3
001	1.65
010	0.828
011	0.424
100	**0.212**
101	0.106
110	0.053
111	0.026

• Recovery coefficient 3

FR3[2:0]	FS/s*
000	0.828
001	0.424
010	0.212
011	0.106
100	**0.053**
101	0.026
110	0.013
111	0.006

* Value at fs = 48kHz, 24kHz, 12kHz

• Recovery speed switch over thresh level 1

THR1[2:0]	Level to ALC_VAL
000	-26dB
001	-24dB
010	-22dB
011	**-20dB**
100	-18dB
101	-16dB
110	-14dB
111	Prohibition

• Recovery speed switch over thresh level 2

THR2[2:0]	Level to ALC_VAL
000	-20dB
001	-18dB
010	-16dB
011	**-14dB**
100	-12dB
101	-10dB
110	-8dB
111	Prohibition

• Zerocross timeout period

ZCDTM[1:0]	Timeout period*	fs = 48k/24k/12kHz
00	1024/fs	21.33ms
01	**2048/fs**	**42.67ms**
10	4096/fs	85.33ms
11	8192/fs	170.7ms

• Recovery alert time

RWT[1:0]	Standby time	fs = 48k/24k/12kHz
00	128/fs	2.67ms
01	256/fs	5.33ms
10	**512/fs**	**10.67ms**
11	1024/fs	21.33ms

* At fs = 32k to 48kHz setting. 1/4 times at 8k to 12kHz, 1/2 times at 16k to 24kHz (48kHz, 24kHz, 12kHz become the same speed).

ALC Circuit Gain Setting Table ALC_VMAX[5:0]/ALC_GAIN[5:0]

[5:0]	GAIN	[5:0]	GAIN	[5:0]	GAIN	[5:0]	GAIN	[5:0]	GAIN
00h	-14dB	0Ah	-4dB	14h	6dB	1Eh	16dB	28h	26dB
01h	-13dB	0Bh	-3dB	15h	7dB	1Fh	17dB	29h	27dB
02h	-12dB	0Ch	-2dB	16h	8dB	20h	18dB	2Ah	28dB
03h	-11dB	0Dh	-1dB	17h	9dB	21h	19dB	2Bh	29dB
04h	-10dB	**0Eh**	**0dB**	18h	10dB	22h	20dB	2Ch	30dB
05h	-9dB	0Fh	1dB	19h	11dB	23h	21dB	2Dh	31dB
06h	-8dB	10h	2dB	1Ah	12dB	24h	22dB	2Eh	32dB
07h	-7dB	11h	3dB	1Bh	13dB	25h	23dB	2Fh	33dB
08h	-6dB	12h	4dB	1Ch	14dB	26h	24dB	30h	34dB
09h	-5dB	13h	5dB	1Dh	15dB	27h	25dB		

• Noise gate silent detection thresh

NGTH[2:0]	Thresh
000	-35dBFS
001	-41dBFS
010	-47dBFS
011	-53dBFS
100	**-59dBFS**
101	-65dBFS
110	-71dBFS
111	-77dBFS

• Noise gate silent detection time/Gain attenuation speed (0dB → -35dB)

NGDT[1:0]	Detection time*	fs = 48kHz 24kHz 12kHz	Gain attenuation time*	fs = 48kHz 24kHz 12kHz
00	2^{13}/fs	0.17s	30×2^{10}/fs	0.64s
01	2^{14}/fs	0.34s	30×2^{11}/fs	1.28s
10	**2^{15}/fs**	**0.68s**	**30×2^{12}/fs**	**2.56s**
11	2^{16}/fs	1.36s	30×2^{13}/fs	5.12s

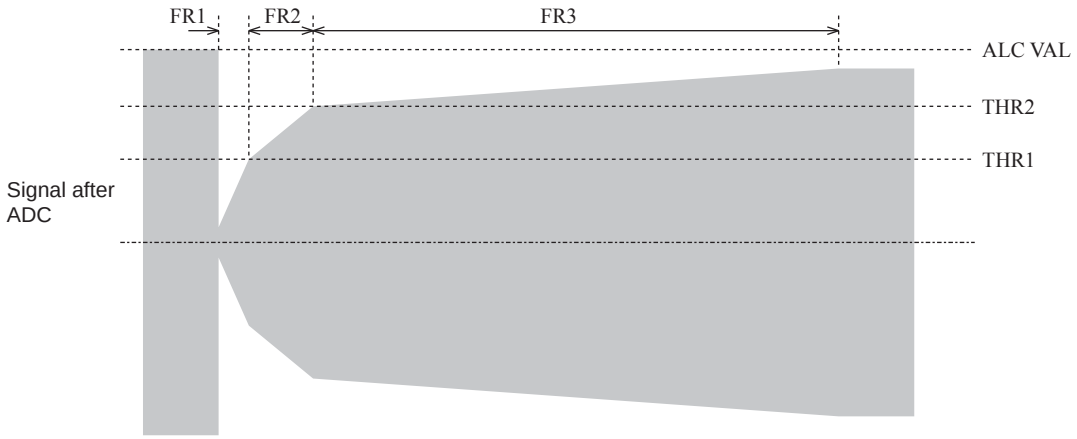
* At fs = 32k to 48kHz setting. 1/4 times at 8k to 12kHz, 1/2 times at 16k to 24kHz

• Noise gate reset time (-35dB → 0dB)

NGRT[1:0]	Gain reset time*	fs = 48kHz 24kHz 12kHz
00	30×2^{8}/fs	0.16s
01	**30×2^{9}/fs**	**0.32s**
10	30×2^{10}/fs	0.64s
11	30×2^{11}/fs	1.28s

* At fs = 32k to 48kHz setting. 1/4 times at 8k to 12kHz, 1/2 times at 16k to 24kHz (48kHz, 24kHz, 12kHz become the same speed).

Relation Between Output level and Recovery Speed (FR,THR)



FR value is shown by inclination (FS/s) of the shape of recovery waves. (FS = Full Scale = 0dBFS)

Description of ALC/Limiter (automatic level control) operation

Note: Whatever is contained inside the parentheses “ ” is applicable in the PB-ALC mode.
The amplifier gain “digital volume value” of the PGA (programmable gain amplifier) is automatically adjusted so that the A/D converter output audio level “digital volume output” is set to the ALC value “ALC_VAL [2:0]”. The PGA “digital volume” gain can be varied in the -14dB to +34dB range. The maximum value “ALC_VMAX [5:0]” can be set in this variable range.

• ALC settings

· Power-saving function
When [PGA_PDX] is 0, the ALC circuit and PGA circuit are set to power down mode.

· Manual function (ALC OFF)
At REC_ALC = PB_ALC = 0, it become manual mode.
PGA gain is fixed by value of ALC_GAIN [5:0]
Digital volume value is fixed by EVR_GAIN [6:0]

· System operation
ALC is performed by feeding back the A/D converter “digital volume” data. Accordingly, configure the settings as shown in the table below in order for the ALC functions to be activated.

Resister	Mode	
	REC-ALC	PB-ALC
PGA_PDX	1	0
ADC_PDX	1	x
DAC_PDX	x	1
REC_ALC	1	0
PB_ALC	0	1

(1) Attack operations
When the ADC “digital volume” output exceeds the ALC limiter level, ALC_VAL[2:0], the PGA gain “digital volume value” is lowered. When the rate of gain attenuation is ALC_THA[2:0] or more, ALC_FA1[1:0] results, but when the value is less than ALC_THA[2:0], ALC_FA2[1:0] results.
When zero-cross detection ALC_ZCD is set to 1, the gain attenuation from zero-cross to zero-cross is limited by the limit value ALC_TLIM[1:0].

(2) Recovery operations

When the ADC “digital volume” output is less than 2dB of the ALC limiter level, ALC_VAL[1:0], and this status continues for the recovery wait time, ALC_RWT[1:0], the PGA gain “digital volume value” is increased.
The rate of gain increase is performed using the recovery coefficients given below according to the amplitude.

Recovery coefficients by level

Output level	<THR1	THR1< <THR2	THR2< <VALC-2dB
FR	FR1	FR2	FR3

The increase in PGA gain “digital volume value” is carried out continuously while the ADC “digital volume” remains less than 2dB of ALC_VAL[1:0]. The amount of increase in zero-cross to zero-cross PGA gain “digital volume value” is at most 1dB.

Functions common to (1) and (2)

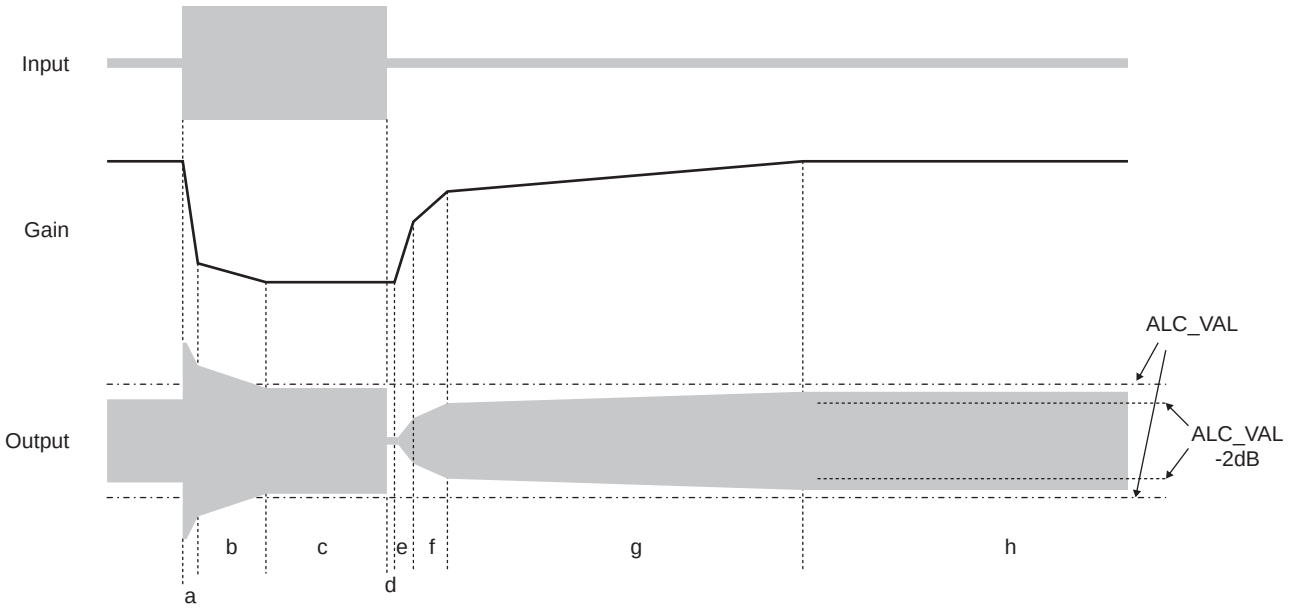
- Zero cross detection

When [ALC_ZCD] is set to 0, the PGA gain “digital volume value” changes regardless of the zero cross timing of the A/D converter “digital volume” output.
When [ALC_ZCD] is set to 1, the PGA gain “digital volume value” changes at the zero cross timing of the A/D converter “digital volume” output.

- Zero cross timeout

Even if the PGA “digital volume” output does not cross zero, as long as there is no zero cross signal during the zero-cross timeout value, ALC_ZCDTM[1:0], a zero-cross signal is generated internally and the PGA gain “digital volume value” is changed.

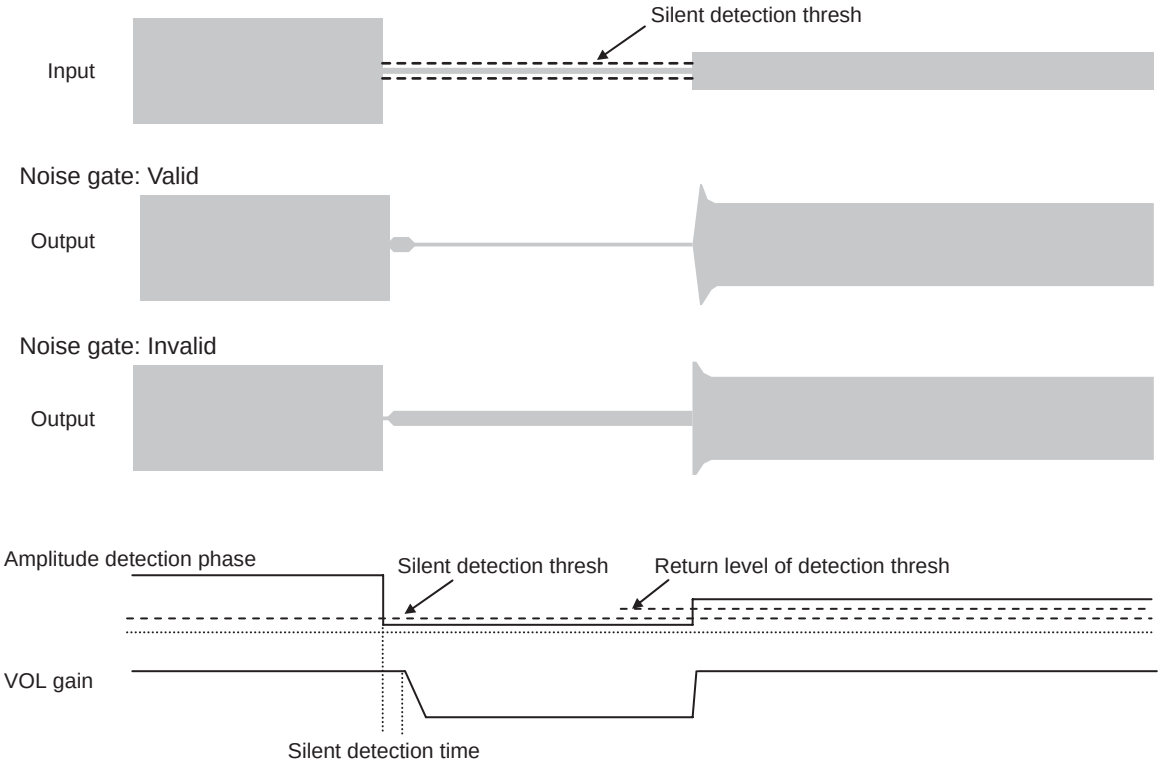
ALC Wave Forms



a: Attack (FA1) b: Attack (FA2) d: Recovery wait time (RWT)
e: Recovery (FR1) f: Recovery (FR2) g: Recovery (FR3)
c, h: Stable

• Noise gate function

The noise gate function is enabled when NGEN is 1. This function cannot be used during PB-ALC mode.
If the PGA input level continues at or below NGTH[2:0] for the period NGDT[1:0], the volume after ADC output is decreased from 0dB to approximately -35dB at the rate NGDT[1:0].
If the PGA input level rises to NGTH+6dB or more, the volume after ADC output is increased from approximately -35dB to 0dB at the rate NGRT[1:0].



• ADC

PGA output undergoes AD conversion and is output as 16-bit serial audio data. The three formats, I^2S, left justified, and right justified are supported.
If ADC_PDX is set to 0, the ADC block is powered down. An interval of 64/fs is used as the ADC initialization interval (initialization + data delay) from the point power down is canceled. When power is turned on, initialization is required when switching the system clock.
A digital HPF for canceling DC offset is built-in. The cut-off frequency, fc, is 1.85Hz (@fs = 48kHz).
The full-scale voltage (0dBFS) is $0.6\times V_{DD}A$.

• DAC

16-bit serial audio data undergoes DA conversion. The three formats, I^2S, left justified, and right justified are supported.
If DAC_PDX is set to 0, the DAC block is powered down. An interval of 58/fs is used as the DAC initialization interval (initialization + data delay) from the point power down is canceled. When power is turned on, initialization is required when switching the system clock.
The full-scale voltage (0dBFS) is $0.6\times V_{DD}A$.

Audio Data Formats

ADRS	Bit	Name	Init	Description
0Dh	[3]	AD_MUTE	0b	Sets the ADC output MUTE 1: Enables MUTE function **0: Disables MUTE function**
	[2]	FBCLK	0b	Sets the BCLK frequency 1: 32fs **0: 64fs**
0Eh	[4]	ADF_MASTER	0b	ADF circuit 1: Master mode, BCLK and LRCLK pins are set for output. **0: Slave mode, BCLK and LRCLK pins are set for input.**
	[3]	ADF_DAC_INV	0b	Sets the DAC input data of the ADF circuit. 1: Inverted **0: Non-inverted**
	[2]	ADF_ADC_INV	0b	Sets the ADC input data of the ADF circuit. 1: Inverted **0: Non-inverted**
	[1:0]	ADF_MODE	00b	Define the data format of the ADF circuit. 11, 10: Right justification (right-justified) 01: Left justification (left-justified) **00: I^2S**

See the section on "Audio Data Formats."

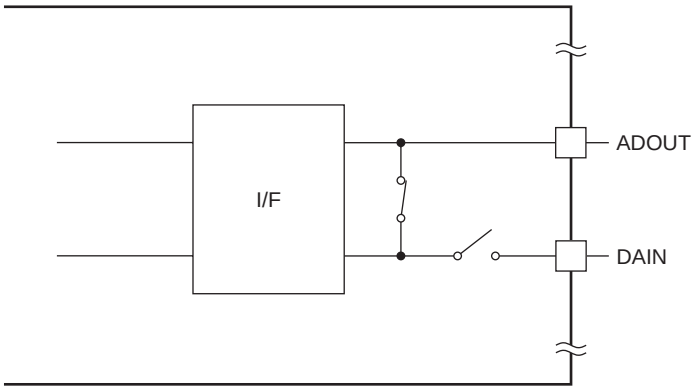
• Loopback

(a) Loopback mode (ADF_LB = 1)

Internal connect between ADOUT and DAIN, This enables the MIC input to be output to the line or speaker without recording or playback operation. In this case, external output through ADOUT is enabled but external input through DAIN is disabled.

(b) Standard mode (ADF_LB = 0)

The DAIN external input is enabled and the internal switch for ADOUT and DAIN is released.



ADRS	Bit	Name	Init	Description
0Fh	[5]	ADF_LB	0b	Loopback setting 1: ADC→Internal loopback in DAC is done **0: ADC→Internal loopback in DAC is not done**

Programmable Digital Filter

• Windcut HPF (1st order)

WIND_CUT [5:4] turns off the high-pass filter (through) when initialized to (00).

Regardless of the sampling frequency (fs), the cutoff frequency (fc) is 400Hz when WIND_CUT [5:4] is set at 11, 300Hz at 10, 200Hz at 01 and OFF at 00.

ADRS	Bit	Name	Init	Description
0Dh	[5:4]	WIND_CUT	00b	WIND_CUT Function (HPF fc setting) 11: 400Hz 10: 300Hz 01: 200Hz 00: OFF

• Programmable Filter

A second order biquad filter that allows coefficients to be freely set is used for the programmable filter.
A notch filter, LPF, or other filter can be configured by setting the coefficients, a1, a2, b0, b1, and b2, in 16-bit 2's complement notation in a register. Make sure that the corresponding filter is OFF when setting or modifying coefficients.

ADRS	Bit	Name	Init	Description
0Dh	[7]	FILTER2	0b	Set the programmable filter2 1: ON **0: OFF**
	[6]	FILTER1	0b	Set the programmable filter1 1: ON **0: OFF**
1Bh	[7:0]	A1[15:8]	00h	Set the programmable filter1 coefficient a1
1Ch	[7:0]	A1[7:0]	00h	
1Dh	[7:0]	A2[15:8]	00h	Set the programmable filter1 coefficient a2
1Eh	[7:0]	A2[7:0]	00h	
1Fh	[7:0]	B0[15:8]	40h	Set the programmable filter1 coefficient b0
20h	[7:0]	B0[7:0]	00h	
21h	[7:0]	B1[15:8]	00h	Set the programmable filter1 coefficient b1
22h	[7:0]	B1[7:0]	00h	
23h	[7:0]	B2[15:8]	00h	Set the programmable filter1 coefficient b2
24h	[7:0]	B2[7:0]	00h	
25h	[7:0]	A1[15:8]	00h	Set the programmable filter2 coefficient a1
26h	[7:0]	A1[7:0]	00h	
27h	[7:0]	A2[15:8]	00h	Set the programmable filter2 coefficient a2
28h	[7:0]	A2[7:0]	00h	
29h	[7:0]	B0[15:8]	40h	Set the programmable filter2 coefficient b0
2Ah	[7:0]	B0[7:0]	00h	
2Bh	[7:0]	B1[15:8]	00h	Set the programmable filter2 coefficient b1
2Ch	[7:0]	B1[7:0]	00h	
2Dh	[7:0]	B2[15:8]	00h	Set the programmable filter2 coefficient b2
2Eh	[7:0]	B2[7:0]	00h	

• DSP Route Setting

The route of digital filter is selected by the SEL_USE_DSP register.

ADRS	Bit	Name	Init	Description
0Fh	[1]	SEL_USE_DSP	0b	DSP Route setting 1: DSP inserted in PB (DAC) side **0: DSP inserted in REC (ADC) side**

Note: Programmable Filter and Wind Cut HPF functions serve as the DSP functions.

- Digital Volume

Contained inside the D/A converter is a digital volume control, and by setting EVR_GAIN [6:0], the gain level can be attenuated from +12dB (max) to -64dB or muted.

When EVR_ZCD is 0, the gain is changed immediately after setting EVR_GAIN [6:0].

When EVR_ZCD is 1, after setting EVR_GAIN [6:0] the gain is changed at the zero cross timing of the audio signals. The timeout time for zero cross detection can be set using EVR_ZCDTM [1:0].

When EVR_SOFTSW is 1, the soft switching operation is performed, and after the EVR_GAIN [6:0] setting has been changed, the gain automatically changes in 1-step increments until it arrives at the predetermined value. The period of gain change can be set using EVR_SSC [1:0].

If EVR-SOFTSW is set to 1 and EVR_ZCD is set to 1, the D/A converter, after the lapse of the time defined by EVR_SSC[1:0], repeats the cycle of waiting for the next zero cross point and changing the gain by 1 increment, until the predetermined volume value is reached.

ADRS	Bit	Name	Init	Description
10h	[7]	EVR_MUTE	1b	Controls the mute function of the EVR (digital) circuit. **1: Enables MUTE function.** 0: Disables MUTE function.
	[6:0]	EVR_GAIN	00h	Controls the gain function of the EVR (digital) circuit. **00h: -64dB** 57h: +12dB to 2Ch: -9.5dB/0.5dB step 2Bh: -10dB to 0Ch: -41dB/1.0dB step 0Bh: -42dB to 00h: -64dB/2.0dB step
11h	[6]	EVR_VOLZCD	1b	Controls the gain change operation of the EVR (digital) circuit at zerocross timing. **1: Changes the gain at the zerocross timing.** 0: Changes the gain without waiting for a zerocross timing.
	[5:4]	EVR_ZCDTM	01b	Set the zerocross detection timeout time of the EVR (digital) circuit. 11: 8192/fs 10: 4096/fs **01: 2048/fs** 00: 1024/fs Valid when [EVR_ZCD] = 1
	[2]	EVR_SOFTSW	1b	Controls the soft switch function of the EVR (digital) circuit. **1: ON** 0: OFF
	[1:0]	EVR_VOLTM	00b	Set the time of the soft switch function of the EVR (digital) circuit (dos not depend on fs). 11, 10: Inhibited 01: 2.278ms/step, (200ms: When +12dB⇔MUTE) **00: 1.142ms/step**, (100ms: When +12dB⇔MUTE)

Digital EVR Circuit Gain Setting Table EVR_GAIN [6:0]

[6:0]	GAIN	[6:0]	GAIN	[6:0]	GAIN	[6:0]	GAIN	[6:0]	GAIN
00h	**-64dB**	12h	-35dB	24h	-17dB	36h	-4.5dB	48h	+4.5dB
01h	-62dB	13h	-34dB	25h	-16dB	37h	-4dB	49h	+5dB
02h	-60dB	14h	-33dB	26h	-15dB	38h	-3.5dB	4Ah	+5.5dB
03h	-58dB	15h	-32dB	27h	-14dB	39h	-3dB	4Bh	+6dB
04h	-56dB	16h	-31dB	28h	-13dB	3Ah	-2.5dB	4Ch	+6.5dB
05h	-54dB	17h	-30dB	29h	-12dB	3Bh	-2dB	4Dh	+7dB
06h	-52dB	18h	-29dB	2Ah	-11dB	3Ch	-1.5dB	4Eh	+7.5dB
07h	-50dB	19h	-28dB	2Bh	-10dB	3Dh	-1dB	4Fh	+8dB
08h	-48dB	1Ah	-27dB	2Ch	-9.5dB	3Eh	-0.5dB	50h	+8.5dB
09h	-46dB	1Bh	-26dB	2Dh	-9dB	3Fh	+0dB	51h	+9dB
0Ah	-44dB	1Ch	-25dB	2Eh	-8.5dB	40h	+0.5dB	52h	+9.5dB
0Bh	-42dB	1Dh	-24dB	2Fh	-8dB	41h	+1dB	53h	+10dB
0Ch	-41dB	1Eh	-23dB	30h	-7.5dB	42h	+1.5dB	54h	+10.5dB
0Dh	-40dB	1Fh	-22dB	31h	-7dB	43h	+2dB	55h	+11dB
0Eh	-39dB	20h	-21dB	32h	-6.5dB	44h	+2.5dB	56h	+11.5dB
0Fh	-38dB	21h	-20dB	33h	-6dB	45h	+3dB	57h	+12dB
10h	-37dB	22h	-19dB	34h	-5.5dB	46h	+3.5dB		
11h	-36dB	23h	-18dB	35h	-5dB	47h	+4dB		

• Playback System Automatic Level Control (ALC)

When REC_ALC is set to 0 and PB_ALC is set to 1 (playback system ALC mode), the digital volume control functions as the playback system ALC. Subject the volume value to automatic adjustment so that the digital volume output level is set to the predetermined value.

For further details on operation, refer to "Description of ALC/limiter (automatic level control) operation."

Noise gate function (NGEN) setting is disabled if playback system ALC mode.

When REC_ALC is set to 0 and PB_ALC is set to 0 (ALC off mode), the digital volume control is set to manual mode, and the gain is fixed to the EVR_GAIN [6:0] register setting.

• Line Amplifier

The line amplifier provides a gain of 0dB, +4dB, +6dB or +8dB.

When LO_MUTE is set to 1, the line output is muted.

When LO_PDX is set to 0, the line amplifier is placed in the power down mode.

If the line output is set to the high-impedance state when the line amplifier is placed in the power down mode, LO_VREFSW must be set to 0.

ADRS	Bit	Name	Init	Description
12h	[7]	LO_MUTE	1b	Controls the mute function of the line out circuit. **1: Enables MUTE function.** 0: Disables MUTE function.
	[6]	LO_VREFSW	1b	State setting when power of line output id downed* **1: Connects to the reference power source (VREF).** 0: Does not connect to the reference power source (VREF).
	[5:4]	LO_GAIN	10b	Select the gain of the line out circuit. 11: +8dB **10: +6dB** 01: +4dB 00: 0dB

* It is not possible to connect between LINE OUT and VREF by setting LO_VREFSW to 1 even if LO_PDX is set to 1.

• Speaker amplifier

The speaker amplifier must be started after the selector amplifier output (LOUT2) has been activated and the voltage has stabilized. Either 0dB or +6dB can be selected as the selector amplifier gain using the SEL_GAIN setting.

V_{DD}S in the range of 2.7V to 5.5V is supported. (Piezoelectric speaker supported)

The amplifier gain is 6dB (+12dB with the BTL output). (With an 8Ω load)

The SPKIN input resistance is 10kΩ (type).

When SP_PDX is set to 0, the speaker amplifier is placed in the power down mode.

Depending on V_{DD}S, one of the four speaker terminal voltages can be selected using SP_BAIS [1:0] to achieve an optimal dynamic range.

• Thermal Shutdown

If a chip temperature of 140°C or higher is detected while SP_TSD_EN is set 1, the speaker amplifier is placed in the power down mode for protection.

The thermal shutdown function is disabled if SP_TSD_EN is set to 0.

ADRS	Bit	Name	Init	Description
12h	[2]	SEL_GAIN	0b	Selector circuit, gain selection 1: +6dB **0: 0dB**
	[1:0]	SEL_IN	01b	Selector input selection setting 00: Prohibition **01: DAC** 10: ALC 11: Prohibition
13h	[3:2]	SP_IDL	10b	Set the idling current of the speaker amplifier circuit 11: 2.0mA **10: 1.0mA** 01: 0.67mA 00: 0.5mA
	[1:0]	SP_BIAS	00b	Set the bias control of the speaker amplifier circuit 11: 0.833×V_{DD}A 10: 0.766×V_{DD}A 01: 0.666×V_{DD}A **00: 0.5×V_{DD}A**
14h	[7]	SP_OUT_EN	0b	Enables or disables the speaker amplifier circuit 1: ON **0: OFF**
	[6]	SP_TSD_EN	1b	Enables or disables the thermal shutdown function of the speaker amplifier circuit **1: ON** 0: OFF

See the section on "Speaker Amplifier Start/Stop Sequence"

• BEEP output

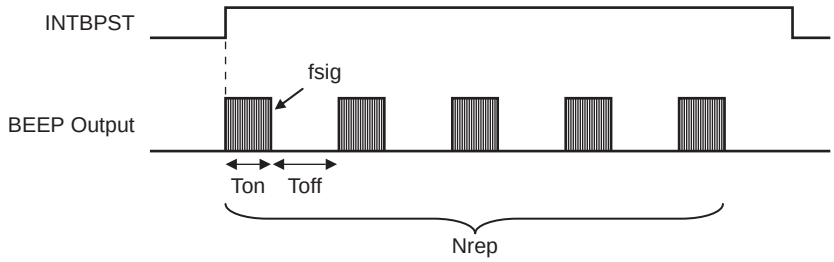
A signal input from the BEEP pin or a BEEP sound (pulse wave) generated within the IC can be output from the speaker.

(a) EXT-BEEP operation

When BPMODE is 01, the signal input to the BEEP pin is output from the speaker.

(b) INT-BEEP operation

When BPMODE is 10/11, a BEEP signal generated within the IC is output from the speaker.



Use the BPHZ register to set the pulse frequency, fsig ,the BPTON and BPTOFF registers to set the on/off duty, and the BPCNT register to set the repeat count, Nrep. Then set INTBPST = 0→1 to output the BEEP sound. Output stops automatically when the specified number of beeps output.
When BPMODE is 10 (serial control mode), INTBPST control is carried out according to registers.
When BPMODE is 11 (parallel control mode), INTBPST control is carried out using the BEEP pin.

Note: When the transition INTBPST = 0→1 is detected, the BEEP sound starts. When BPMODE is 10 (serial control mode), the BEEP sound is not output even if INTBPST = 1 is sent when INTBPST is set to 1.

If toff is 0, the continuous BEEP sound is output during the period given by ton*Nrep.
If Nrep is set to infinite, the ton/toff cycle repeats infinitely and stops when INTBPST is set to 0.
Output stops when INTBPST is set to 0, even in the middle of BEEP output.

The gain from the start of BEEP input until BTL output can be varied within the range -15dB to -21dB, based on the SP_BPVOL[1:0] setting.
It is also possible to adjust the sound volume using an external resistor and by setting of 0dB.
[Againof approximately -21dB (typ) results with an external 100kΩ connection.]

ADRS	Bit	Name	Init	Description
13h	[7:6]	BPMODE	00b	BEEP output mode setting 11: INT-BEEP operation/parallel control mode 10: INT-BEEP operation/serial control mode 01: EXT-BEEP operation **00: OFF**
	[5:4]	BPVOL	11b	BEEP gain selection **11: -21dB** 10: -18dB 01: -15dB 00: 0dB
2Fh	[7:5]	BPTON	010b	INT-BEEP on duty (ton) setting
	[4:0]	BPTOFF	00110b	INT-BEEP off duty (toff) setting
30h	[7]	INTBPST	0b	INT-BEEP starting control (At BPMODE = 10, Valid)
	[6:4]	BPHZ	011b	INT-BEEP frequency (fsig) setting
	[3:0]	BPCNT	0110b	INT-BEEP number of cycles (Nrep) setting

BPHZ[2:0]	fsig
000	1kHz
001	2kHz
010	3kHz
011	4kHz
100	5kHz
101	6kHz
110	7kHz
111	8kHz

BPTON[2:0]	Ton
000	20ms
001	40ms
010	60ms
011	80ms
100	100ms
101	120ms
110	140ms
111	160ms

BPTOFF[4:0]	Toff	BPTOFF[4:0]	Toff
00000	0ms	01011	210ms
00001	10ms	01100	230ms
00010	30ms	01101	250ms
00011	50ms	01110	270ms
00100	70ms	01111	290ms
00101	90ms	10000	310ms
00110	110ms	10001	330ms
00111	130ms	10010	350ms
01000	150ms	10011	370ms
01001	170ms	10100	390ms
01010	190ms		

BPCNT[3:0]	Nrep	BPCNT[3:0]	Nrep
0000	infinite	1000	8
0001	1	1001	9
0010	2	1010	10
0011	3	1011	11
0100	4	1100	12
0101	5	1101	13
0110	6	1110	14
0111	7	1111	15

● PLL

(a) PLL mode (PLL_PDX = 1)

In this mode, the 256fs clock (MCLK) used by the CODEC block is generated from the clock (12, 13.5, 24 and 27MHz frequencies supported) which is input from MCLKIN, and BCLK and LRCK are output.
Sampling frequencies (fs) of 7.86kHz to 48kHz are supported.

fs setting

fs is set by setting the division ratio for each of the three frequency dividers (DIV1, DIV2, and DIV3) in respective registers.

1. Set FCKI[2:0] for the MCLKIN frequency, results in 12MHz or 13.5MHz as the frequency input to DIV1.
2. Set DIV1, DIV2, and DIV3, while referring to the division ratio setting example table.

$$f_{MCKOUT} = \frac{f_{MCLKIN} \times DIV2}{FCKI \times DIV1 \times DIV3} = 256fs$$

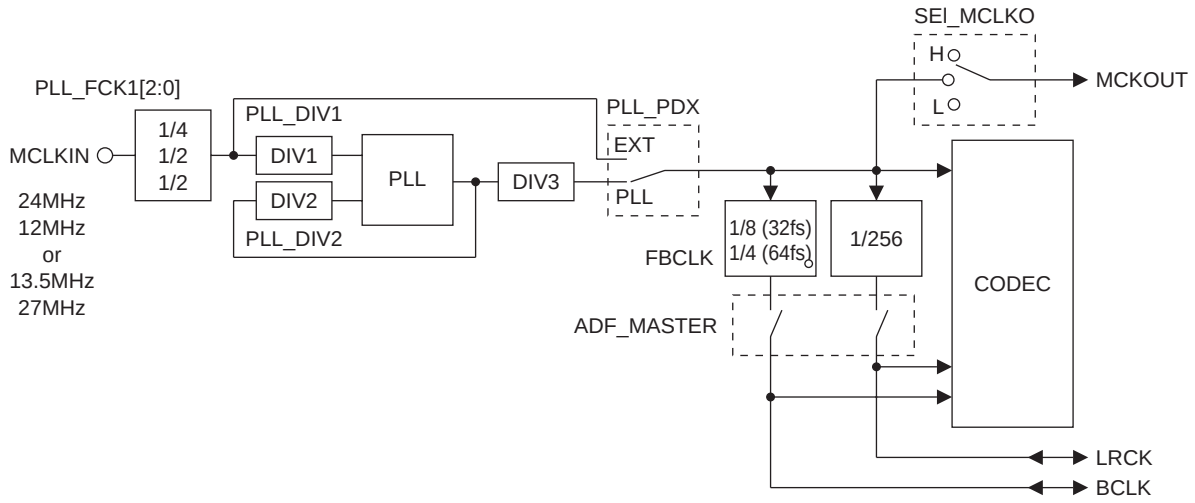
ex. "FCKI = 2, DIV1 = 125, DIV2 = 128, DIV3 = 2" in case of "MCLKIN = 24MHz, fs = 24kHz"

(b) EXT mode (PLL_PDX = 0)

In this mode, the 256fs clock (MCLK) from MCLKIN is input and used.
When ADF_MASTER is 1, BCLK and LRCK whose frequency is obtained by dividing the frequency of MCLKIN are output.
When ADF_MASTER is 0, BLCK and LRCK are external inputs.

* In the CODEC block, BCLK and LRCK must be synchronized with MCLK.
In PLL mode (PLL_PDX = 1), operation must be performed in BCLK output mode (ADF_MASTER = 1). In EXT mode (PLL_PDX = 0) and when ADF_MASTER is 0, BCLK and LRCK synchronized with MCLK must be input.

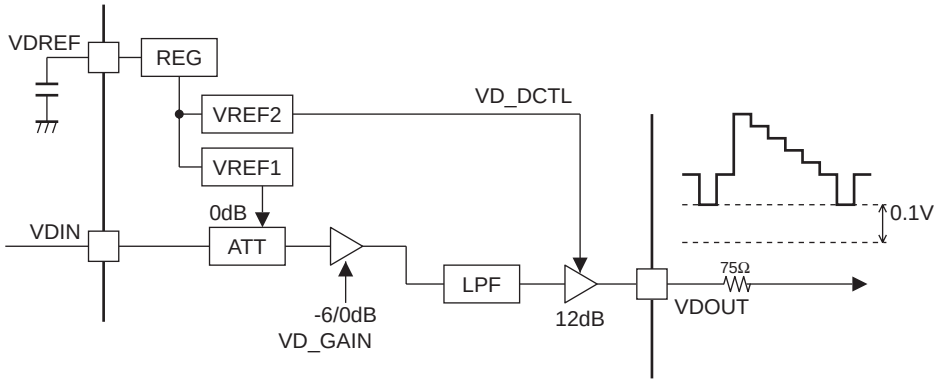
PLL Block Diagram



ADRS	Bit	Name	Init	Description
0Dh	[2]	FBCLK	0b	Sets the BCLK frequency **0: 64fs** 1: 32fs
0Eh	[4]	ADF_MASTER	0b	Sets the BCLK, LRCK master/slave **0: slave** 1: master
16h	[5:4]	SEL_MCLKO	00b	MCLKO output selection **00: "L"** 10: "H" 01/11: MCLKIN[PLL_PDX = 0] or PLL output [PLL_PDX = 1]
16h 17h	[0] [7:0]	PLL_DIV1	07Dh	Sets the basis clock frequency ratio (DIV1) 000h: Prohibition 001h: 1/1 to 1FFh: 1/511 default: 07Dh(125)
18h 19h	[0] [7:0]	PLL_DIV2	080h	Sets the VCO output frequency ratio (DIV2) 000h: Prohibition 001h: 1/1 to 1FFh: 1/511 default: 080h(128)
1Ah	[1:0]	PLL_DIV3	00b	Sets the MCLK output frequency ratio (DIV3) **00: 1/1** 01: 1/2 10: 1/4 11: 1/4
	[5:4]	PLL_FCKI	00b	Sets the MCLKIN input frequency ratio **00: 1/1** 01: 1/2 10: 1/4 11: 1/4

Frequency Ratio Setting Example		DIV1 input = 12MHz			DIV1 input = 13.5MHz		
Target frequency		Frequency Ratio Value			Frequency Ratio Value		
fs(kHz)	256fs(MHz)	DIV1	DIV2	DIV3	DIV1	DIV2	DIV3
48	12.288	125	128	1	245	223	1
44.1	11.29	304	286	1	171	143	1
32	8.192	271	185	1	206	125	1
24	6.144	125	128	2	245	223	2
22.05	5.6448	304	286	2	171	143	2
16	4.096	271	185	2	206	125	2
12	3.072	125	128	4	245	223	4
11.025	2.8224	304	286	4	171	143	4
8	2.048	271	185	4	206	125	4

• Video Driver



VDIN Sync DC: State of -12.5mV to 162.5mV (At 12.5mV/step, +12dB),
-25mV to 325mV (25mV/step, At +6dB) is adjustable to VDOUT Sync DC (100mV).

Either 6dB or 12dB can be selected as the total gain of the video amplifier using the internal register setting (VD_GAIN). When the input sync level is within the -12.5mV to 162.5mV (At +12dB)/-25mV to 325mV (At 6dB) range, the output sync level can be adjusted to 100mV using the internal register settings (VD_DCTL [3 : 0]).

ADRS	Bit	Name	Init	Description
14h	[4]	VD_GAIN	0b	Selects the driver gain of the video circuit **0: +6dB** 1: +12dB
	[3:0]	VD_DCTL	0001b	Selects the input sync level DC OFFSET of the video circuit 0000: -25mV to 1110: 325mV (+6dB) 0000: -12.5mV to 1110: 162.5mV (+12dB)

Video Driver Sync DC Level Adjustment Table

VD_DCTL[3:0]	Input_Sync_DC At +6dB	Input_Sync_DC At +12dB	Output_Sync_DC
0000	-25mV	-12.5mV	100mV
0001	0mV	0mV	100mV
0010	25mV	12.5mV	100mV
0011	50mV	25mV	100mV
0100	75mV	37.5mV	100mV
0101	100mV	50mV	100mV
0110	125mV	62.5mV	100mV
0111	150mV	75mV	100mV
1000	175mV	87.5mV	100mV
1001	200mV	100mV	100mV
1010	225mV	112.5mV	100mV
1011	250mV	125mV	100mV
1100	275mV	137.5mV	100mV
1101	300mV	150mV	100mV
1110	325mV	162.5mV	100mV
1111	0mV	0mV	100mV

Register Table

ADRS (Address): displayed in hexadecimal notation,
Init (initial value): displayed in hexadecimal notation
Register bits indicated by "0" must be set to 0.
Registers indicated with a gray background are for IC testing and their initial values are fixed.
All registers (addresses: 00 to 25h) must be loaded with write data (including test registers).

Functions	ADRS [7:0]	Init	Register Data D[7:0]							
			7	6	5	4	3	2	1	0
PM1	00h	00h	MIC_PDX	MIC_PWR_PDX	PGA_PDX	ADC_PDX	DAC_PDX	SEL_PDX	LO_PDX	SP_PDX
PM2	01h	00h	SYNC_CLR	0	VREF_BIAS[1]	VREF_BIAS[0]	0	PLL_PDX	REG_PDX	VD_PDX
MIC	02h	10h	0	0	MIC_GAIN[1]	MIC_GAIN[0]	0	0	0	0
ALC1	03h	12h	0	ALC_VAL[2]	ALC_VAL[1]	ALC_VAL[0]	0	ALC_FA1[2]	ALC_FA1[1]	ALC_FA1[0]
ALC2	04h	24h	0	ALC_THA[2]	ALC_THA[1]	ALC_THA[0]	0	ALC_FA2[2]	ALC_FA2[1]	ALC_FA2[0]
ALC3	05h	34h	0	ALC_THR1[2]	ALC_THR1[1]	ALC_THR1[0]	0	ALC_FR1[2]	ALC_FR1[1]	ALC_FR1[0]
ALC4	06h	34h	0	ALC_THR2[2]	ALC_THR2[1]	ALC_THR2[0]	0	ALC_FR2[2]	ALC_FR2[1]	ALC_FR2[0]
ALC5	07h	04h	0	0	0	0	0	ALC_FR3[2]	ALC_FR3[1]	ALC_FR3[0]
ALC6	08h	56h	ALC_FULLEN	ALC_ZCD	ALC_ZCDTM[1]	ALC_ZCDTM[0]	ALC_TLIM[1]	ALC_TLIM[0]	ALC_RWT[1]	ALC_RWT[0]
ALC7	09h	49h	ALC_NGEN	ALC_NGTH[2]	ALC_NGTH[1]	ALC_NGTH[0]	ALC_NGDT[1]	ALC_NGDT[0]	ALC_NGRT[1]	ALC_NGRT[0]
ALC8	0Ah	0Ah	0	0	0	0	1	0	1	0
ALC9	0Bh	0Eh	0	0	ALC_VMAX[5]	ALC_VMAX[4]	ALC_VMAX[3]	ALC_VMAX[2]	ALC_VMAX[1]	ALC_VMAX[0]
ALC10	0Ch	0Eh	0	0	ALC_GAIN[5]	ALC_GAIN[4]	ALC_GAIN[3]	ALC_GAIN[2]	ALC_GAIN[1]	ALC_GAIN[0]
CODEC1	0Dh	02h	FILTER2	FILTER1	WIND_CUT[1]	WIND_CUT[0]	AD_MUTE	FBCLK	REC_ALC	PB_ALC
CODEC2	0Eh	00h	0	0	0	ADF_MASTER	ADF_DAC_INV	ADF_ADC_INV	ADF_MODE[1]	ADF_MODE[0]
CODEC3	0Fh	00h	0	0	ADF_LB	0	0	0	SEL_USE_DSP	0
EVR1	10h	80h	EVR_MUTE	EVR_GAIN[6]	EVR_GAIN[5]	EVR_GAIN[4]	EVR_GAIN[3]	EVR_GAIN[2]	EVR_GAIN[1]	EVR_GAIN[0]
EVR2	11h	54h	0	EVR_VOLZCD	EVR_ZCDTM[1]	EVR_ZCDTM[0]	0	EVR_SOFTSW	EVR_VOLTM[1]	EVR_VOLTM[0]
LINE/SEL	12h	E1h	LO_MUTE	LO_VREFSW	LO_GAIN[1]	LO_GAIN[0]	0	SEL_GAIN	SEL_IN[1]	SEL_IN[0]
SPK1	13h	38h	BPMODE[1]	BPMODE[0]	BPVOL[1]	BPVOL[0]	SP_IDL[1]	SP_IDL[0]	SP_BIAS[1]	SP_BIAS[0]
SPK2/VIDEO	14h	41h	SP_OUT_EN	SP_TSD_EN	0	VD_GAIN	VD_DCTL[3]	VD_DCTL[2]	VD_DCTL[1]	VD_DCTL[0]
FS	15h	08h	0	0	0	0	FS[3]	FS[2]	FS[1]	FS[0]
PLL1_1	16h	00h	0	0	SEL_MCLKO[1]	SEL_MCLKO[0]	0	0	0	PLL_DIV1[8]
PLL1_2	17h	7Dh	PLL_DIV1[7]	PLL_DIV1[6]	PLL_DIV1[5]	PLL_DIV1[4]	PLL_DIV1[3]	PLL_DIV1[2]	PLL_DIV1[1]	PLL_DIV1[0]
PLL2_1	18h	00h	0	0	0	0	0	0	0	PLL_DIV2[8]
PLL2_2	19h	80h	PLL_DIV2[7]	PLL_DIV2[6]	PLL_DIV2[5]	PLL_DIV2[4]	PLL_DIV2[3]	PLL_DIV2[2]	PLL_DIV2[1]	PLL_DIV2[0]
PLL3	1Ah	00h	0	0	PLL_FCKI[1]	PLL_FCKI[0]	0	0	PLL_DIV3[1]	PLL_DIV3[0]
FILTER1_A1	1Bh	00h	A1[15]	A1[14]	A1[13]	A1[12]	A1[11]	A1[10]	A1[9]	A1[8]
FILTER1_A1	1Ch	00h	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
FILTER1_A2	1Dh	00h	A2[15]	A2[14]	A2[13]	A2[12]	A2[11]	A2[10]	A2[9]	A2[8]
FILTER1_A2	1Eh	00h	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]	A2[2]	A2[1]	A2[0]
FILTER1_B0	1Fh	40h	B0[15]	B0[14]	B0[13]	B0[12]	B0[11]	B0[10]	B0[9]	B0[8]
FILTER1_B0	20h	00h	B0[7]	B0[6]	B0[5]	B0[4]	B0[3]	B0[2]	B0[1]	B0[0]
FILTER1_B1	21h	00h	B1[15]	B1[14]	B1[13]	B1[12]	B1[11]	B1[10]	B1[9]	B1[8]
FILTER1_B1	22h	00h	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]
FILTER1_B2	23h	00h	B2[15]	B2[14]	B2[13]	B2[12]	B2[11]	B2[10]	B2[9]	B2[8]
FILTER1_B2	24h	00h	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]
FILTER2_A1	25h	00h	A1[15]	A1[14]	A1[13]	A1[12]	A1[11]	A1[10]	A1[9]	A1[8]
FILTER2_A1	26h	00h	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
FILTER1_A2	27h	00h	A2[15]	A2[14]	A2[13]	A2[12]	A2[11]	A2[10]	A2[9]	A2[8]
FILTER1_A2	28h	00h	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]	A2[2]	A2[1]	A2[0]

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Functions	ADRS [7:0]	Init	Register Data D[7:0]							
			7	6	5	4	3	2	1	0
FILTER1_B0	29h	40h	B0[15]	B0[14]	B0[13]	B0[12]	B0[11]	B0[10]	B0[9]	B0[8]
FILTER1_B0	2Ah	00h	B0[7]	B0[6]	B0[5]	B0[4]	B0[3]	B0[2]	B0[1]	B0[0]
FILTER1_B1	2Bh	00h	B1[15]	B1[14]	B1[13]	B1[12]	B1[11]	B1[10]	B1[9]	B1[8]
FILTER1_B1	2Ch	00h	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]
FILTER1_B2	2Dh	00h	B2[15]	B2[14]	B2[13]	B2[12]	B2[11]	B2[10]	B2[9]	B2[8]
FILTER1_B2	2Eh	00h	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]
SPK_BEEP1	2Fh	46h	BPTON[2]	BPTON[1]	BPTON[0]	BPTOFF[4]	BPTOFF[3]	BPTOFF[2]	BPTOFF[1]	BPTOFF[0]
SPK_BEEP2	30h	36h	INTBPST	BPHZ[2]	BPHZ[1]	BPHZ[0]	BPCNT[3]	BPCNT[2]	BPCNT[1]	BPCNT[0]
TEST1	31h	00h	0	0	0	0	0	0	0	0
TEST2	32h	00h	0	0	0	0	0	0	0	0
TEST3	33h	00h	0	0	0	0	0	0	0	0
TEST4	34h	9Dh	1	0	0	1	1	1	0	1
TEST5	35h	10h	0	0	0	1	0	0	0	0
TEST6	36h	A3h	1	0	1	0	0	0	1	1
TEST7	37h	01h	0	0	0	0	0	0	0	1
TEST8	38h	21h	0	0	1	0	0	0	0	1
TEST9	39h	00h	0	0	0	0	0	0	0	0

Register Description

ADRS	Bit	Name	Init	Description
00h	[7]	MIC_PDX	0b	MIC amplifier circuit, power control 1: power on **0: power down**
	[6]	MIC_PWR_PDX	0b	MIC Power circuit, power control 1: power on **0: power down**
	[5]	PGA_PDX	0b	PGA circuit, power control 1: power on **0: power down**
	[4]	ADC_PDX	0b	ADC circuit, power control 1: power on **0: power down**
	[3]	DAC_PDX	0b	DAC circuit, power control 1: power on **0: power down**
	[2]	SEL_PDX	0b	Selector circuit, power control 1: power on **0: power down**
	[1]	LO_PDX	0b	Line out circuit circuit, power control 1: power on **0: power down**
	[0]	SP_PDX	0b	Speaker amplifier circuit, power control 1: power on **0: power down**
01h	[7]	SYNC_CLR	0b	Internal logic clear 1: ON **0: OFF(normal operation)**
	[5] [4]	VREF_BIAS	00b	Reference voltage circuit (VREF pin) setting **00: Power down** 11: Normal operation 10: Quick rise to reference voltage 01: IREF ON/VREF OFF
	[2]	PLL_PDX	0b	PLL circuit, power control 1: power on **0: power down**
	[1]	REG_PDX	0b	REG circuit, power control 1: power on **0: power down**
	[0]	VD_PDX	0b	Video driver circuit, power control 1: power on **0: power down**
02h	[5:4]	MIC_GAIN	01b	MIC amplifier circuit, gain setting 11: +26dB 10: +20dB **01: 0dB** 00: 0dB
03h	[6:4]	ALC_VAL	001b	Set the ALC limiter level 000: -3dBFS 001: **-4dBFS** 010: -5dBFS 011: -6dBFS 100: -7dBFS 101: -8dBFS 110: -9dBFS 111: -10dBFS
	[2:0]	ALC_FA1	010b	Attack coefficient 1 setting
04h	[6:4]	ALC_THA	010b	Set the attack speed switch over thresh
	[2:0]	ALC_FA2	100b	Attack coefficient 2 setting
05h	[6:4]	ALC_THR1	011b	Set the recovery speed switch over thresh 1
	[2:0]	ALC_FR1	100b	Recovery coefficient 1 setting
06h	[6:4]	ALC_THR2	011b	Set the recovery speed switch over thresh 2
	[2:0]	ALC_FR2	100b	Recovery coefficient 2 setting
07h	[2:0]	ALC_FR3	100b	Recovery coefficient 3 setting

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ADRS	Bit	Name	Init	Description
08h	[7]	ALC_FULLEN	0b	Full scale detection mode setting. 1: ON **0: OFF**
	[6]	ALC_ZCD	1b	Controls the gain change operation at zerocross timing. **1: ON** 0: OFF
	[5:4]	ALC_ZCDTM	01b	Set the zerocross detection timeout time. Valid when [ALC_ZCD] = 1. 11: 8192/fs 10: 4096/fs **01: 2048/fs** 00: 1024/fs
	[3:2]	ALC_TLIM	01b	Set the inter-zerocross attack limit. 11: 4dB 10: 2dB **01: 1dB** 00: 0.5dB Valid when [ALC_ZCD] = 1
	[1:0]	ALC_RWT	10b	Set the recovery alert time 11: 1024/fs **10: 512/fs** 01: 256/fs 00: 128/fs
09h	[7]	ALC_NGEN	0b	Set the noise gate function 1: Valid **0: Invalid**
	[6:4]	ALC_NGTH	100b	Set the noise gate silent detection thresh level
	[3:2]	ALC_NGDT	10b	Set the noise gate silent detection time/Set the gain attenuation time
	[1:0]	ALC_NGRT	01b	Set the noise gate reset time
0Bh	[5:0]	ALC_VMAX	0Eh	Set the maximum PGA gain value (Init value 0Eh: 0dB)
0Ch	[5:0]	ALC_GAIN	0Eh	Set the manual mode PGA gain value (Init value 0Eh: 0dB)
0Dh	[7]	FILTER2	0b	Programmable Filter2 setting 1: ON **0: OFF**
	[6]	FILTER1	0b	Programmable Filter1 setting 1: ON **0: OFF**
	[5:4]	WIND_CUT	00b	WIND_CUT function (HPF fc setting) 11: 400Hz 10: 300Hz 01: 200Hz **00: OFF**
	[3]	AD_MUTE	0b	ADC output MUTE setting 1: Enables MUTE function **0: Disables MUTE**
	[2]	FBCLK	0b	Set the BCLK frequency 1: 32fs **0: 64fs**
	[1:0]	REC_ALC PB_ALC	10b	Set the ALC mode **10: REC ALC** 01: PB ALC 00/11: ALC OFF
0Eh	[4]	ADF_MASTER	0b	ADF circuit 1: Master mode **0: Slave mode**
	[3]	ADF_DAC_INV	0b	ADF circuit, DAC input data setting 1: Inverted **0: Non-inverted**
	[2]	ADF_ADC_INV	0b	ADF circuit, ADC input data setting 1: Inverted **0: Non-inverted**
	[1:0]	ADF_MODE	00b	ADF circuit, Format setting 11, 10: right-justified 01: left-justified **00: I^2S**
0Fh	[5]	ADF_LB	0b	Loopback setting 1: Internal loopback is done **0: Internal loopback is not done**
	[1]	SEL_USE_DSP	0b	DSP route setting 1: PB (DAC) side **0: REC(ADC) side**
10h	[7]	EVR_MUTE	1b	Controls the mute function of the EVR (digital) circuit. **1: Enables MUTE function.** 0: Disables MUTE function.
	[6:0]	EVR_GAIN	00h	Controls the gain function of the EVR (digital) circuit. **00h: -64dB** 57h: +12dB to 2Ch: -9.5dB /0.5dB step 2Bh: -10dB to 0Ch: -41dB /1.0dB step 0Bh: -42dB to 00h: -64dB /2.0dB step
11h	[6]	EVR_VOLZCD	1b	Controls the gain change operation of the EVR (digital) circuit at zerocross timing. **1: ON** 0: OFF
	[5:4]	EVR_ZCDTM	01b	Set the zerocross detection timeout time of the EVR (digital) circuit. 11: 8192/fs 10: 4096/fs **01: 2048/fs** 00: 1024/fs Valid when [EVR_ZCD] = 1
	[2]	EVR_SOFTSW	1b	Controls the soft switch function of the EVR (digital) circuit. **1: ON** 0: OFF
	[1:0]	EVR_VOLTM	00b	Set the time of the soft switch function of the EVR (digital) circuit (dos not depend on fs). 01: 2.278ms/step, (200ms: When +12dB⇔MUTE) **00: 1.142ms/step**, (100ms: When +12dB⇔MUTE) 11, 10: Set prohibition
12h	[7]	LO_MUTE	1b	Line out circuit, MUTE function **1: Enables MUTE function** 0: Disables MUTE function
	[6]	LO_VREFSW	1b	State setting when power of lineout is downed **1: Connects to the reference power source (VREF)** 0: Does not connects to the reference power source (VREF)
	[5:4]	LO_GAIN	10b	Line out circuit, gain selection 11: +8dB **10: +6dB** 01: +4dB 00: 0dB
	[2]	SEL_GAIN	0b	Selector circuit, gain selection 1: +6dB **0: 0dB**
	[1:0]	SEL_IN	01b	Selector input selection setting 00: Prohibition **01: DAC** 10: ALC 11: Prohibition
13h	[7:6]	BPMODE	00b	BEEP output mode setting 01: EXT-BEEP operation **00: OFF** 11: INT-BEEP operation/parallel control 10: INT-BEEP operation/serial control
	[5:4]	BPVOL	11b	BEEP gain selection **11: -21dB** 10: -18dB 01: -15dB 00: 0dB
	[3:2]	SP_IDL	10b	Set the idling current of the speaker amplifier circuit 11: 2.0mA **10: 1.0mA** 01: 0.67mA 00: 0.5mA
	[1:0]	SP_BIAS	00b	Set the bias control of the speaker amplifier circuit 11: 0.833×$V_{DD}A$ 10: 0.766×$V_{DD}A$ 01: 0.666×$V_{DD}A$ **00: 0.5×$V_{DD}A$**

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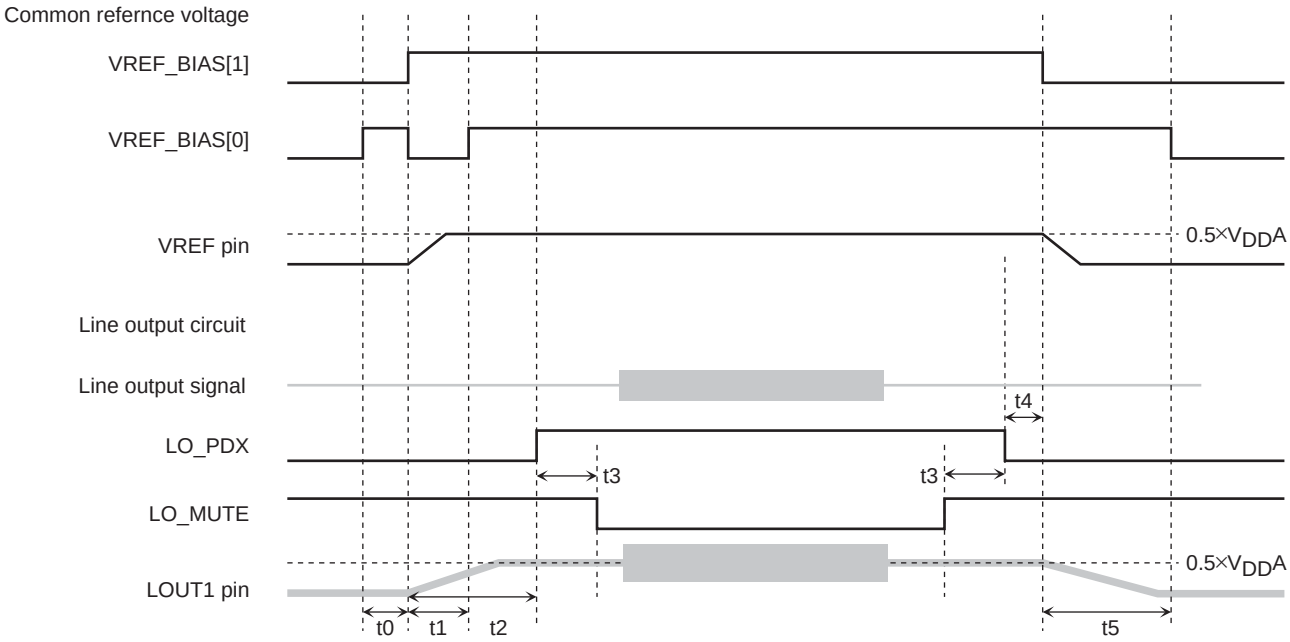
ADRS	Bit	Name	Init	Description
14h	[7]	SP_OUT_EN	0b	Enables or disables the speaker amplifier circuit 1: ON **0: OFF**
	[6]	SP_TSD_EN	1b	Enables or disables the thermal shutdown function of the speaker amplifier circuit **1: ON** 0: OFF
	[4]	VD_GAIN	0b	Selects the driver gain of video circuit **0: +6dB** 1: +12dB
	[3:0]	VD_DCTL	0001b	Select the Input Sync Level DC OFFSET of video circuit 0000: -25mV to 1110: 325mV (+6dB) 0000: -12.5mV to 1110: 162.5mV (+12dB)
15h	[3:0]	FS	1000b	Sampling frequency setting **1000: 48kHz** / 0111: 44.1kHz / 0110: 32kHz / 0101: 24kHz 0100: 22.05kHz / 0011: 16kHz / 0010: 12kHz / 0001: 11.025kHz/ 0000: 8kHz
16h	[5:4]	SEL_MCLKO	00b	MCLKO output selection **00: "L"** 00: "H" 01/11: MCLKIN [PLL_PDX = 0] or PLL output [PLL_PDX = 1]
16h 17h	[0] [7:0]	PLL_DIV1	07Dh	Sets the basis clock frequency ratio (DIV1) 000H: Prohibition 001h: 1/1 to 1FFh: 1/511 default: **07Dh(125)**
18h 19h	[0] [7:0]	PLL_DIV2	080h	Sets the VCO output frequency ratio (DIV2) 000H: Prohibition 001h: 1/1 to 1FFh: 1/511 default: **080h(128)**
1Ah	[5:4]	PLL_FCKI	00b	Sets the MCLKIN input frequency ratio **00: 1/1** 01: 1/2 10: 1/4 11: 1/4
	[1:0]	PLL_DIV3	00b	Sets the MCLK output frequency ratio (DIV3) **00: 1/1** 01: 1/2 10: 1/4 11: 1/4
1Bh	[7:0]	A1[15:8]	00h	Sets the programmable Filter1 coefficient a1
1Ch	[7:0]	A1[7:0]	00h	
1Dh	[7:0]	A2[15:8]	00h	Sets the programmable Filter1 coefficient a2
1Eh	[7:0]	A2[7:0]	00h	
1Fh	[7:0]	B0[15:8]	40h	Sets the programmable Filter1 coefficient b0
20h	[7:0]	B0[7:0]	00h	
21h	[7:0]	B1[15:8]	00h	Sets the programmable Filter1 coefficient b1
22h	[7:0]	B1[7:0]	00h	
23h	[7:0]	B2[15:8]	00h	Sets the programmable Filter1 coefficient b2
24h	[7:0]	B2[7:0]	00h	
25h	[7:0]	A1[15:8]	00h	Sets the programmable Filter2 coefficient a1
26h	[7:0]	A1[7:0]	00h	
27h	[7:0]	A2[15:8]	00h	Sets the programmable Filter2 coefficient a2
28h	[7:0]	A2[7:0]	00h	
29h	[7:0]	B0[15:8]	40h	Sets the programmable Filter2 coefficient b0
2Ah	[7:0]	B0[7:0]	00h	
2Bh	[7:0]	B1[15:8]	00h	Sets the programmable Filter2 coefficient b1
2Ch	[7:0]	B1[7:0]	00h	
2Dh	[7:0]	B2[15:8]	00h	Sets the programmable Filter2 coefficient b2
2Eh	[7:0]	B2[7:0]	00h	
2Fh	[7:5]	BPTON	010b	INT-BEEP on duty(ton) setting
	[4:0]	BPTOFF	00110b	INT-BEEP off duty(toff) setting
30h	[7]	INTBPST	0b	INT-BEEP starting control (At BPMODE = 10 valid)
	[6:4]	BPHZ	011b	INT-BEEP frequency (fsig) setting
	[3:0]	BPCNT	0110b	INT-BEEP number of cycles (Nrep) setting
31h to 39h		TEST		

MIC = Microphone amp
ALC = Automatic Level Control
ADC = AD Converter
DAC = DA Converter
EVR = Electronic Variable Resistor
ADF = Audio Data Format
PGA = Programmable Gain Amplifier
ADRS = Address
Init = Initial value
Nh = N denotes a hexadecimal number
Nb = N denotes a binary number

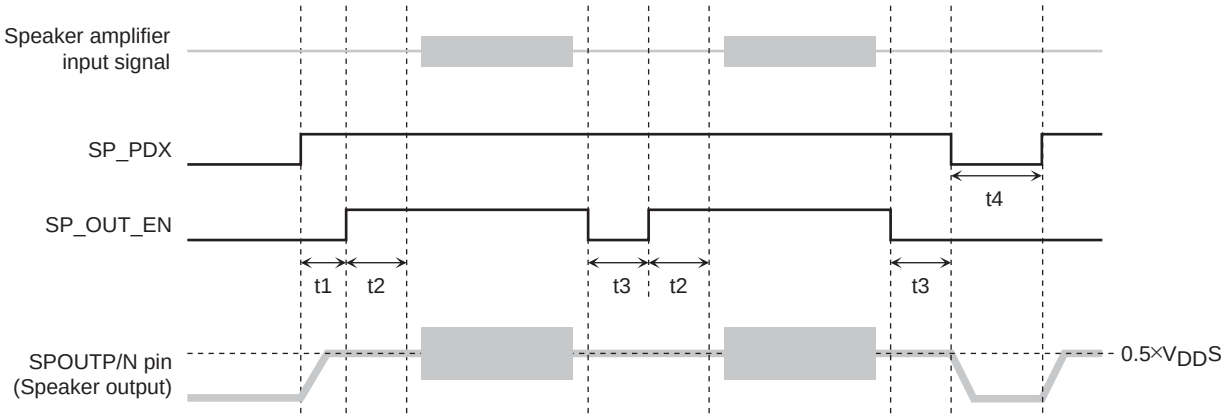
Control Sequence

Reference voltage, line out start/stop sequence



- Recommendation value
  - t0 > 1ms (Pull down period, at already when $L_{OUT}1$ pin is GND level.)
  - t1 > 100ms (Rapid charge period, at VREF pin connected capacity is 4.7μF)
  - t2 > 300ms ($L_{OUT}1$ charge time)
  - t3 > 1ms (Waiting time of MUTE ON/OFF)
  - t4 > 0s
  - t5 > 300ms (Pull down period)
- It makes it to LO_VREFSW = 1 usually.
- LO_VREFSW function at power down (LO_PDX = 0)
  - LO_VREFSW = 1: LOUT1 pin becomes VREF level output
  - LO_VREFSW = 0: LOUT1 pin becomes Hi-Z

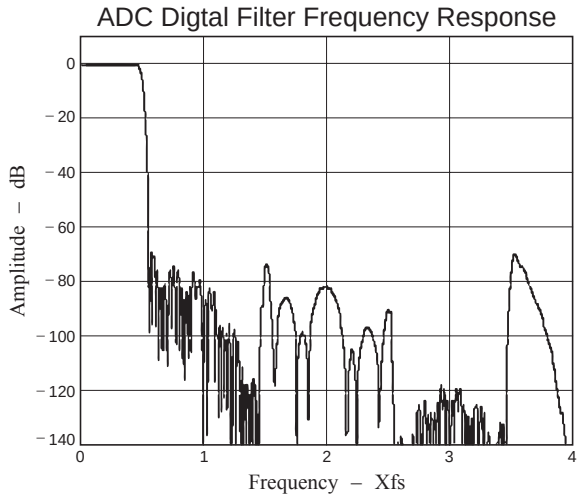
Speaker Amplifier Start/Stop Sequence

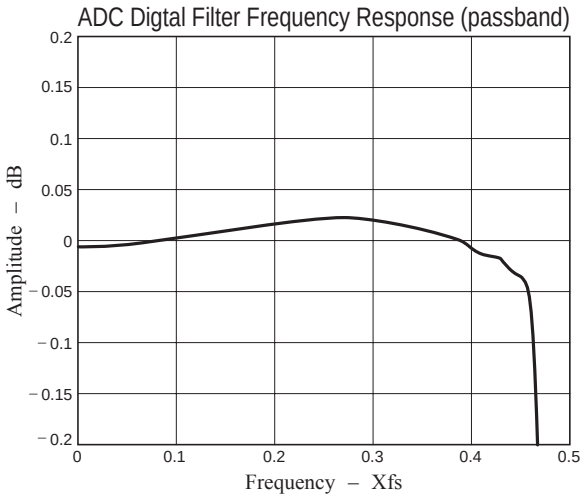


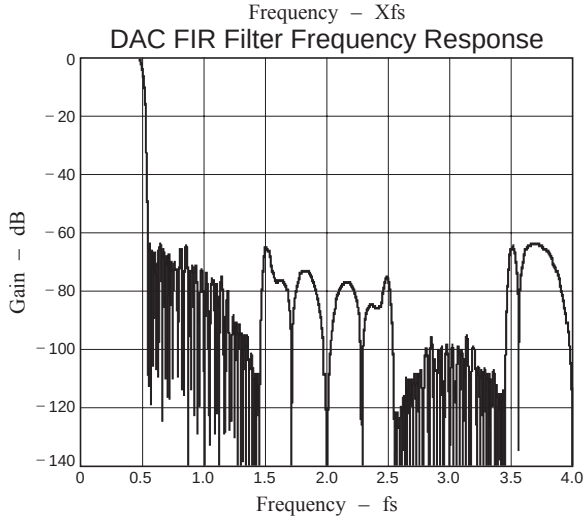
- Recommendation value
  - t1 > 5ms (Speaker bias start-up time)
  - t2 ≠ 10ms (Processing period when POP sound is decreased. Input signal recommends MUTE.)
  - t3 > 15ms
  - t4 > 1ms
- External capacitance connected to SPKIN pin is 0.1μF
- SP_OUT_EN must be set to 0 when power down (SP_PDX = 0) mode.

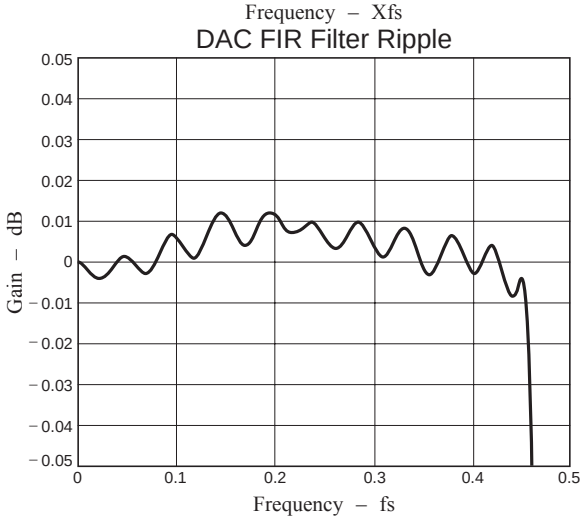
Digital Filter

ADC/DAC digital filters



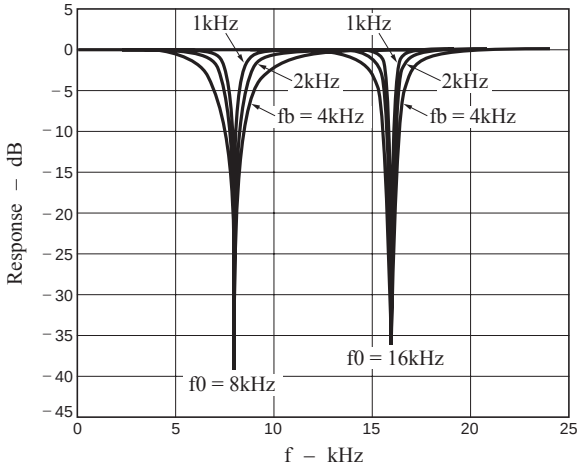




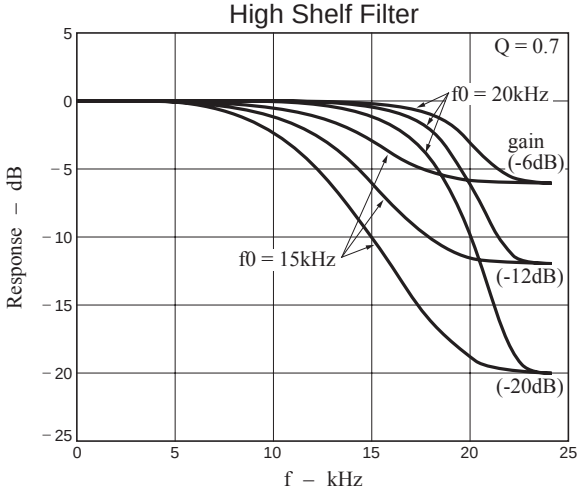


Programmable digital filter setting example @fs = 48kHz

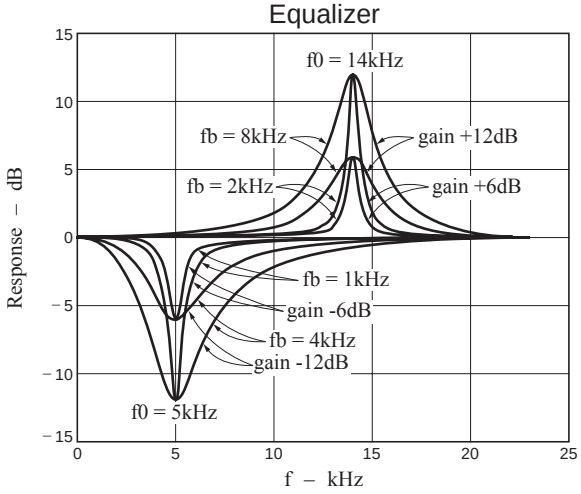
Notch Filter



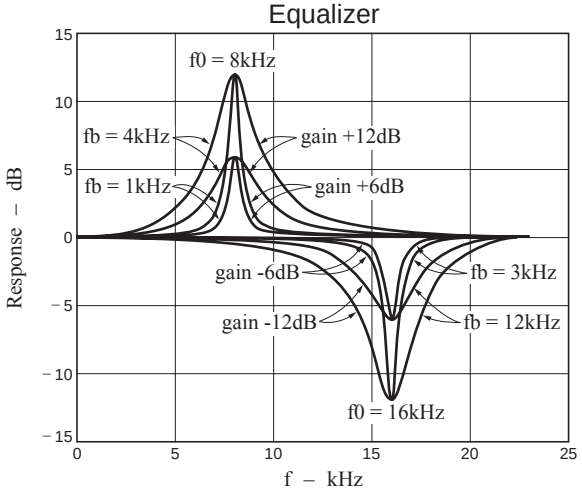
High Shelf Filter



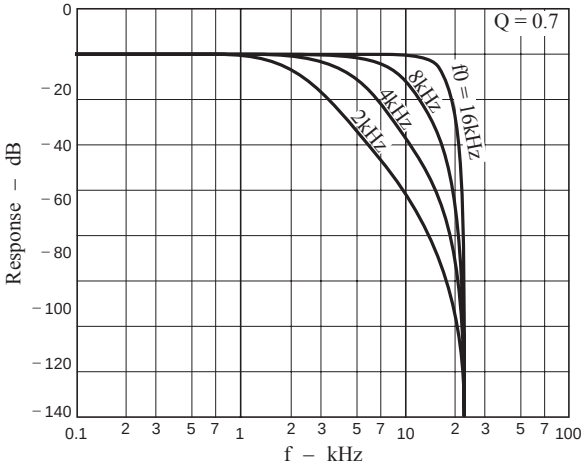
Equalizer



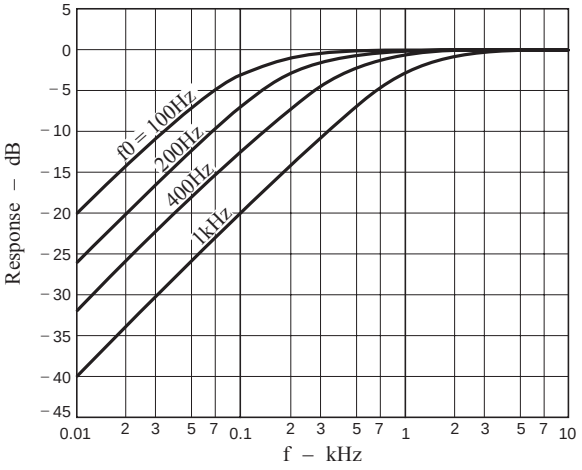
Equalizer



LPF



HPF



Checkpoints

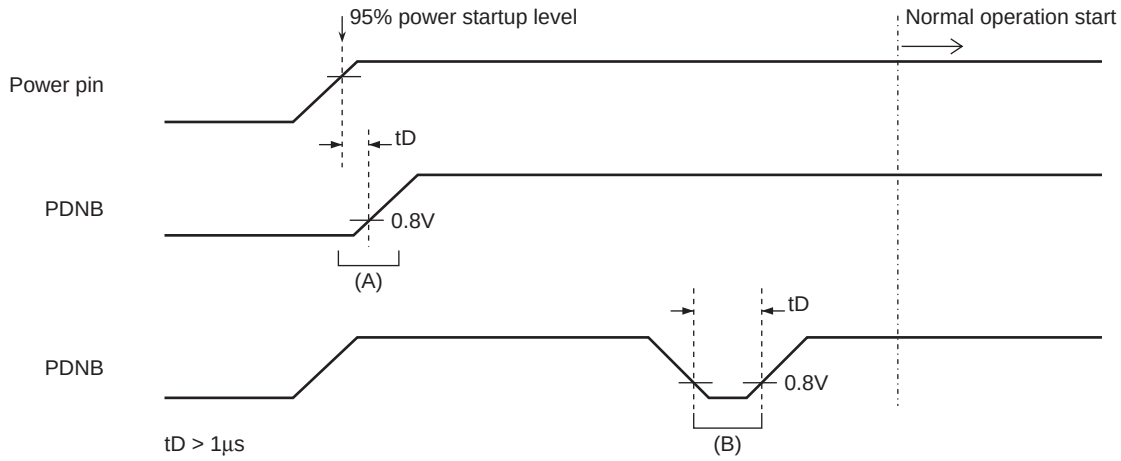
The user is responsible for ascertaining whether this IC can be adopted for the set to be mass production by the user, including the various condition for mounting in the set.

1) Power supply

- The 3.0V type and 3.0V/5.0V type are available as the power supply pins.
  1.8V type: Digital power supply I/O ($V_{DD}IO$)
  3.0V type: Digital power supply (V_{DD}), analog power supplies ($V_{DD}R$, $V_{DD}A$, $V_{DD}V$, $V_{DD}P$)
  3.0V/5.0V type: Analog power supply ($V_{DD}S$)
- The power-on sequence is such that the power is first applied in sequence starting with the circuits that operate using a high voltage and the power is turned off in sequence starting with the circuits that operate using a low voltage.

2) Resetting

- At power-on, the PDNB pin must be set to low without fail.
  (A) or (B) is executed as shown in the figure below.



Notes: (A) is reset at the same time as the power is first applied.
(B) is reset immediately after the power is first applied.
The MCLKIN pin clock input must be provided without fail during either the (A) or (B) period.

3) 3-line serial setting

- Whenever 3-line serial setting is to be performed, it must be done where the MCLKIN input has stabilized without fail.
- If garbled data is found, restart the IC (switching the state of the PDNB pin from low to high) and perform 3-line serial setting again.

Application Circuit Example