

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6A36S, JT6A36X-AS

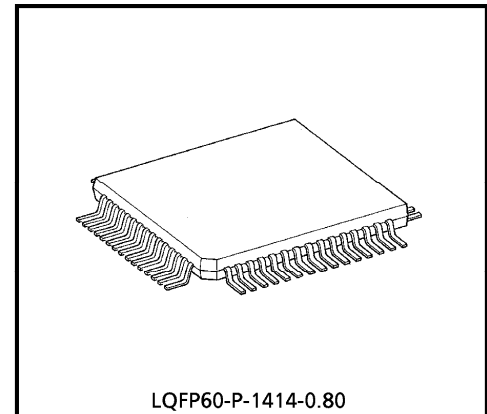
T6A36S, JT6A36X-AS CMOS 1 CHIP LSI FOR LCD ELECTRONIC CALCULATOR

The T6A36S, JT6A36X-AS is a 1 chip microcomputer for 8-digits 1-memory electronic calculator.

T6A36S, JT6A36X-AS can drive the liquid crystal display (LCD). Single power supply operation, low power consumption make it suitable for single battery operated pocketable calculator.

FEATURES

- 8 digits of data and one symbol digit for calculator.
- Algebraic calculation mode.
- Punctuation.
- Standard 4 functions (+, -, ×, ÷), mark up percent with automatic add-On / discount, automatic constant calculations, chain calculations, memory calculations with memory overflow protection.
- Internal keyboard decoding and denouncing.
- Complementary output buffer for direct driving of liquid crystal display (LCD : FEM type - 3.0V, 1/2 bias, 1/3 duty).
- Single power supply (- 1.5V typ.).
- Quad in line flat package (60 PIN).
- Very low power consumption (3.0 μ W typ. at wait).
- Very wide range of operating voltage ($V_{SS} = -1.2 \sim -2.0V$).
- Automatic power off (A time for about 7 min.).



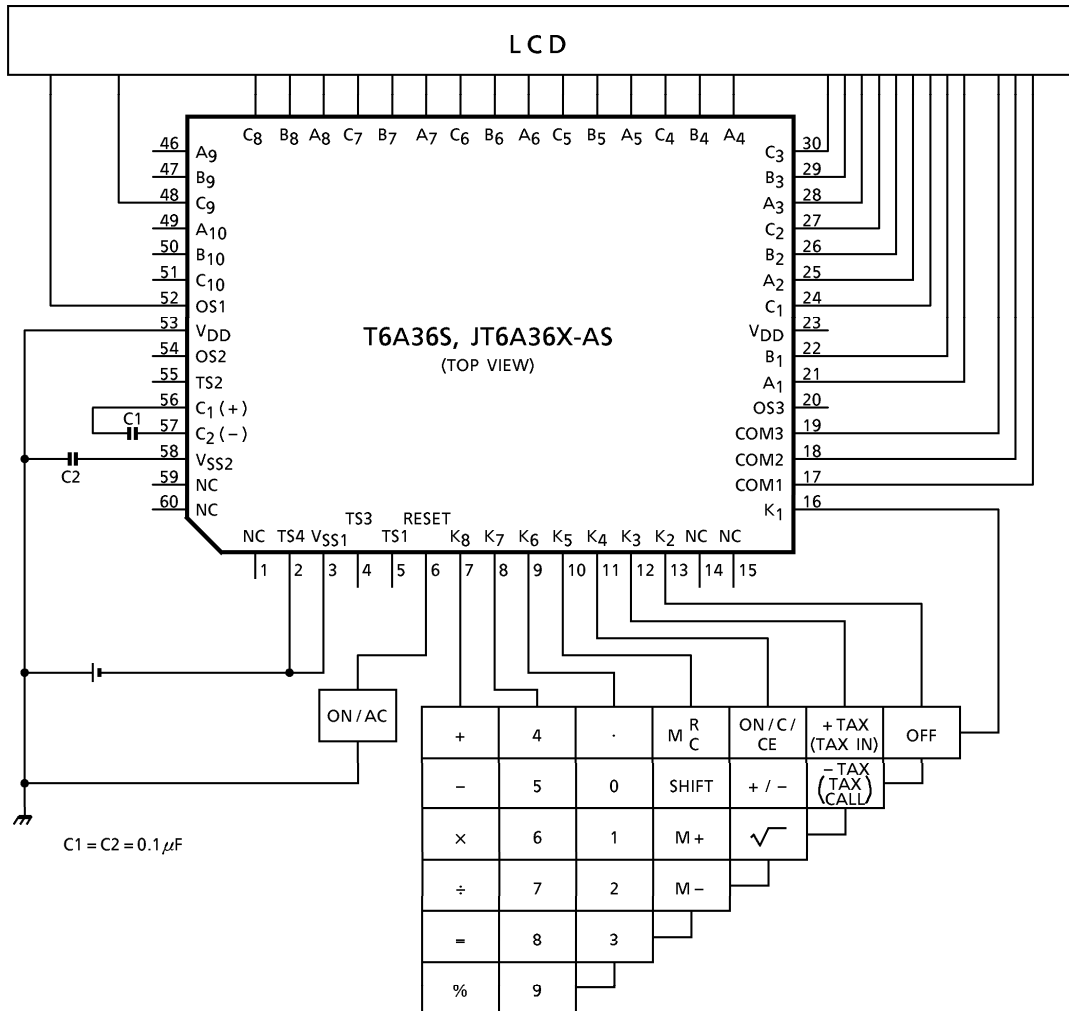
Weight : 0.66g (Typ.)

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SYSTEM BLOCK DIAGRAM

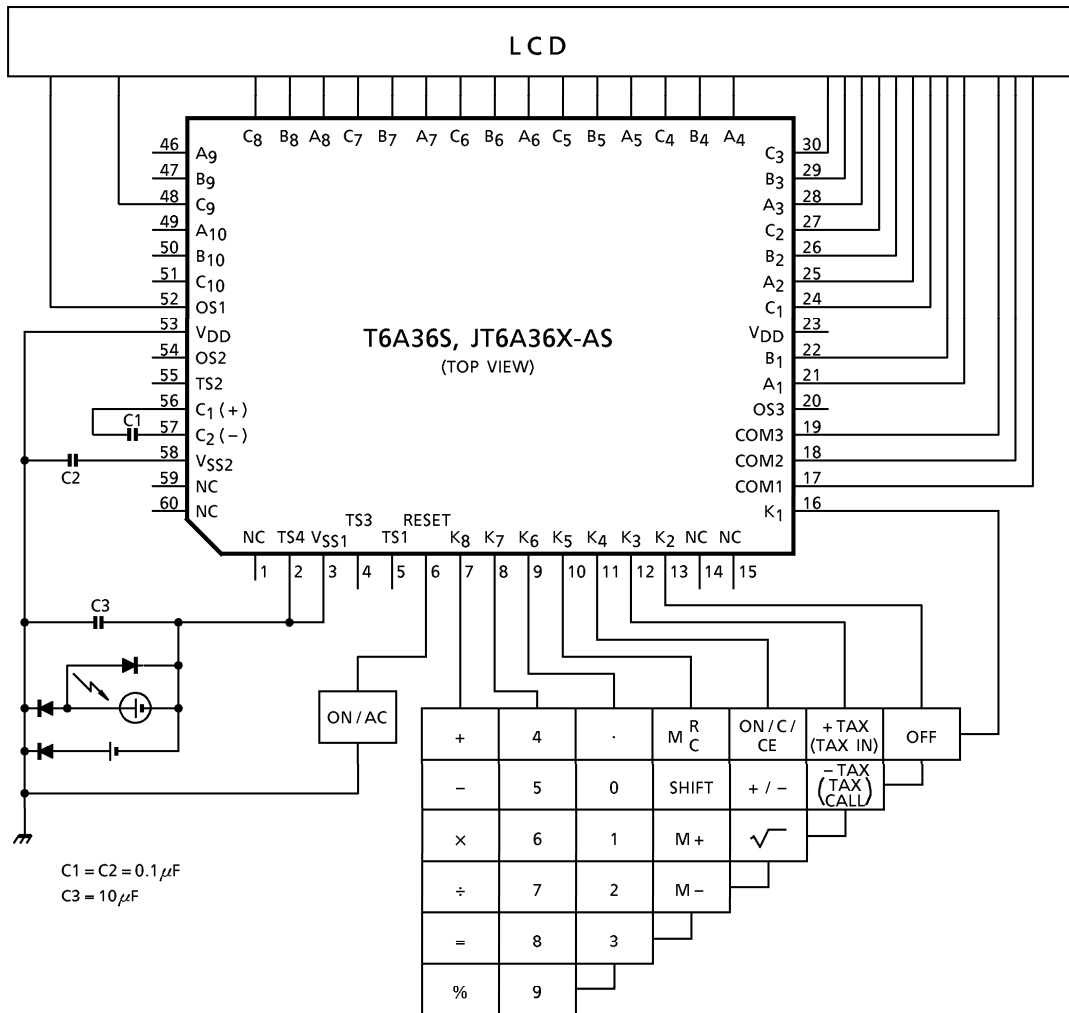
Battery Type



[NOTE]

TS4 $\begin{cases} V_{DD} & \dots\dots \text{OFF MODE DISABLE} \\ V_{SS1} & \dots\dots \text{OFF MODE ENABLE} \end{cases}$
 $R_{key} \leq 20k\Omega$ (- 1.2V)

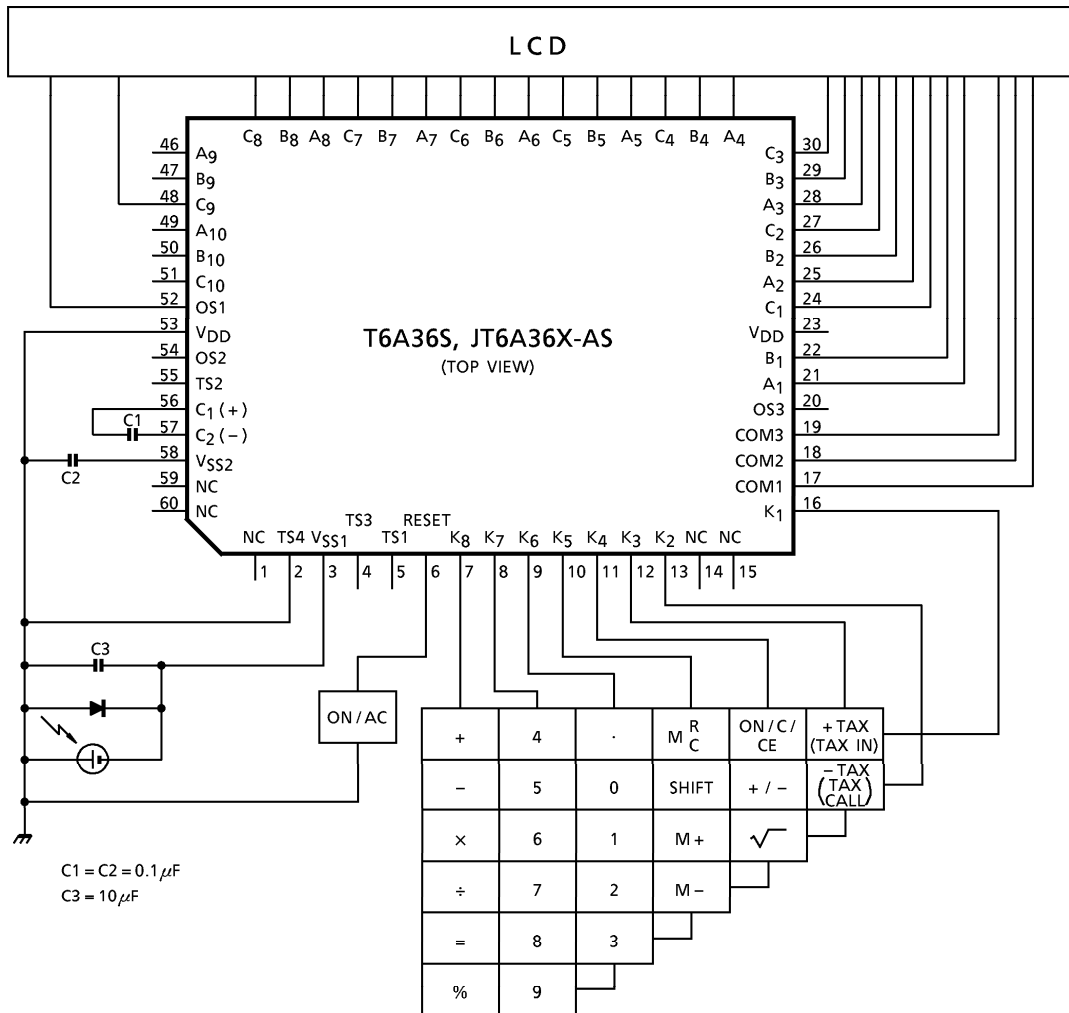
Dual Type



[NOTE]

TS4 { VDD OFF MODE DISABLE
VSS1 OFF MODE ENABLE
Rkey ≤ 20kΩ (-1.2V)

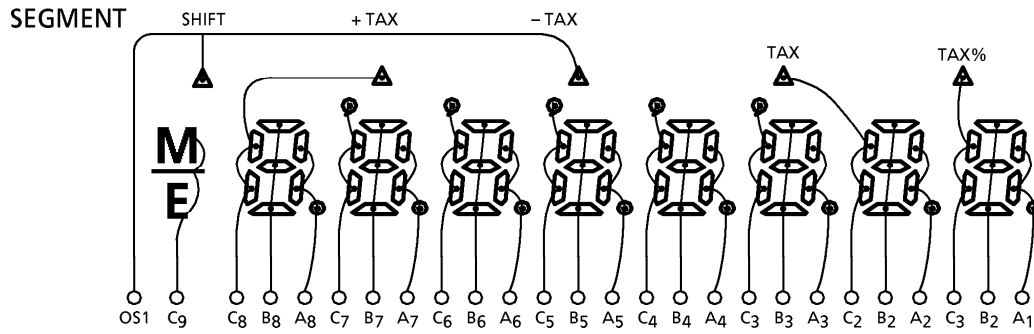
Solar Type



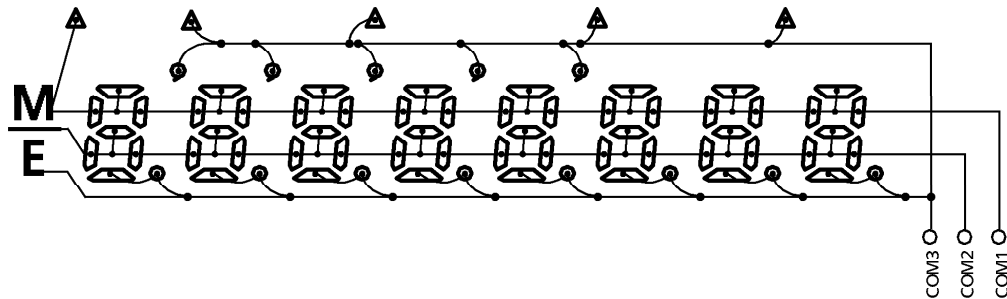
[NOTE]

TS4 { V_{DD} OFF MODE DISABLE
V_{SS1} OFF MODE ENABLE
R_{key} \leq 20k Ω (- 1.2V)

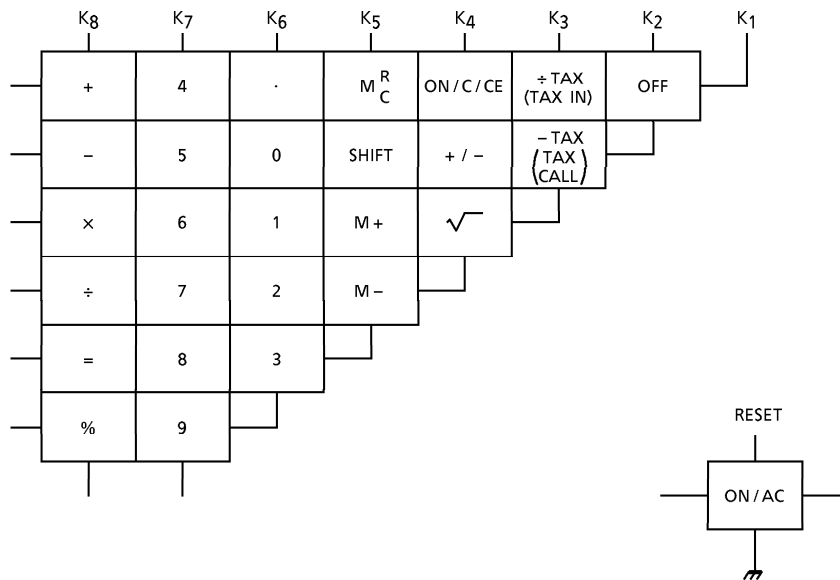
CONNECTION OF LCD



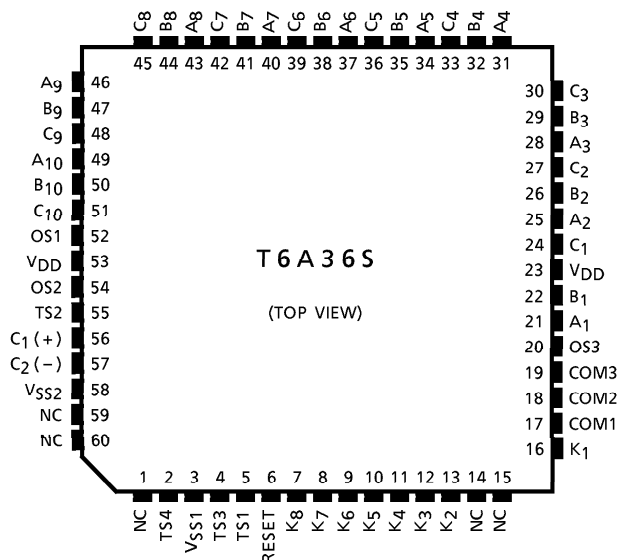
COMMON



KEY LAYOUT



PIN LAYOUT



SPECIFICATION OF CALCULATOR

Operational Features

- (1) 8 digits of data and one symbol digit.
- (2) Algebraic mode.
- (3) Full floating point.
- (4) Standard 4 functions +, -, ×, ÷.
- (5) Memory calculation and memory hold.
- (6) TAX calculation.
- (7) Percent with automatic add-on and discount.
- (8) Constant calculation (Automatic constant).
- (9) Chain calculation.
- (10) Leading zero suppression.
- (11) Trailing zero suppression.
- (12) Square root.
- (13) Change sign.

Capacity of Calculation

- (1) Numeral entry 8 digits
- (2) Addition / Subtraction 8 digits + (-) 8 digits = 8 digits
- (3) Multiplication / Division 8 digits × (÷) 8 digits = 8 digits
- (4) Memory calculation 8 digits + (-) 8 digits = 8 digits

Display Font



Arithmetic Operations

1. Addition

Key Op.	Display
A	A
$\boxed{+}$	A
B	B
$\boxed{+}$	A + B
C	C
$\boxed{=}$	A + B + C
D	D
$\boxed{+}$	D
E	E
$\boxed{+}$	D + E
$\boxed{=}$	D + E

2. Subtraction

(1)	A	A
	$\boxed{-}$	A
	B	B
	$\boxed{-}$	A - B
	C	C
	$\boxed{=}$	A - B - C
	$\boxed{-}$	A - B - C

	Key Op.	Display
	D	D
	$\boxed{+ / -}$	- D
	$\boxed{-}$	A - B - C + D
	$\boxed{=}$	- (A - B - C + D)
3. Multiplication		
(1)	A	A
	$\boxed{\times}$	A
	B	B
	$\boxed{=}$	A·B
	$\boxed{+}$	A·B
	C	C
	$\boxed{=}$	A·B + C
(2)	$\boxed{-}$	0.
	A	A
	$\boxed{\times}$	- A
	B	B
	$\boxed{=}$	- A·B
4. Division		
(1)	A	A
	$\boxed{\div}$	A
	B	B
	$\boxed{=}$	A / B
(2)	$\boxed{-}$	0.
	A	A.
	$\boxed{\div}$	- A
	B	B
	$\boxed{=}$	- A / B

5. Power calculation

	Key Op.	Display
(1)	A	A
	\times	A
	$=$	A^2
	$=$	A^3
(2)	A	A
	\div	A
	$=$	$1/A$
	$=$	$1/A^2$
(3)	$-$	0.
	A	A
	\times	$-A$
	$=$	A^2
(4)	$=$	$-A^3$
	$-$	0.
	A	A
	\div	$-A$
(5)	$=$	$-1/A$
	$=$	$1/A^2$
	A	A
	\times	A
	$=$	A^2
	\times	A^2
	$=$	A^4

6. Mixed calculation

(1)	A	A
	\times	A
	B	B
	$+$	$A \cdot B$
	C	C

7. Constant calculation

	Key Op.	Display
	\div	$A \cdot B + C$
	D	D
	$\frac{\square}{\square}$	$\frac{A \cdot B + C}{D}$
	E	E
	$=$	$\frac{A \cdot B + C}{D} - E$
(1)	A	A
	\times	A
	B	B
	$=$	$A \cdot B$
	C	C
	$=$	$A \cdot C$
(2)	\square	0.
	A	A
	\times	-A
	B	B
	$=$	$-A \cdot B$
	C	C
	$=$	$-A \cdot C$
(3)	A	A
	\div	A
	B	B
	$=$	A / B
	C	C
	$=$	C / B
	D	D
	\times	D
	$=$	D^2

	Key Op.	Display
(4)	A	A
	$\boxed{+}$	A
	B	B
	$\boxed{=}$	A + B
	C	C
	$\boxed{=}$	C + B
(5)	A	A
	$\boxed{-}$	A
	B	B
	$\boxed{=}$	A - B
	C	C
	$\boxed{=}$	C - B
(6)	A	A
	$\boxed{\times}$	A
	B	B
	$\boxed{=}$	A · B
	C	C
	$\boxed{\times}$	C
	D	D
	$\boxed{=}$	C · D
	E	E
	$\boxed{=}$	C · E
	$\boxed{\times}$	C · E
	F	F
	$\boxed{=}$	C · E · F
	G	G
	$\boxed{\div}$	G
H	H	
$\boxed{=}$	G / H	

	Key Op.	Display
	I	I
	$\boxed{=}$	I / H
(7)	A	A
	$\boxed{\times}$	A
	B	B
	$\boxed{\%}$	$A \cdot B / 100$
	C	C
	$\boxed{\%}$	$A \cdot C / 100$
	D	D
	$\boxed{\div}$	D
	E	E
	$\boxed{\%}$	$100 \cdot D / E$
	F	F
	$\boxed{\%}$	$100 \cdot F / E$

8. Mark-up/Discount calculator

(1)	A	A
	$\boxed{\times}$	A
	B	B
	$\boxed{+}$	$A \cdot B$
	$\boxed{=}$	$A + A \cdot B$
(2)	A	A
	$\boxed{\times}$	A
	B	B
	$\boxed{-}$	$A \cdot B$
	$\boxed{=}$	$A - A \cdot B$
(3)	A	A
	$\boxed{\times}$	A
	B	B
	$\boxed{\%}$	$A \cdot B / 100$

	Key Op.	Display
	$\boxed{+}$	$A \cdot B / 100$
	$\boxed{=}$	$A + A \cdot B / 100$
(4)	A	A
	$\boxed{\times}$	A
	B	B
	$\boxed{\%}$	$A \cdot B / 100$
	$\boxed{-}$	$A \cdot B / 100$
	$\boxed{=}$	$A - A \cdot B / 100$
(5)	A	A
	$\boxed{+}$	A
	B	B
	$\boxed{\%}$	$A + A \cdot B / 100$
(6)	A	A
	$\boxed{-}$	A
	B	B
	$\boxed{\%}$	$A - A \cdot B / 100$

9. Memory calculation

	Key Op.	Display	Memory
	A	A	0.
	$\boxed{M+}$	A (M)	A
	B	B (M)	A
	$\boxed{M+}$	B (M)	A + B
	C	C (M)	A + B
	$\boxed{M-}$	C (M)	A + B - C
	D	D (M)	A + B - C
	$\boxed{M^R_C}$	A + B - C (M)	A + B - C
	$\boxed{M^R_C}$	A + B - C	0.
(2)	A	A	0.
	$\boxed{+}$	A	0.

	Key Op.	Display	Memory
	B	B	0.
	$\boxed{M+}$	A + B (M)	A + B
	$\boxed{+}$	A + B (M)	A + B
	$\boxed{M+}$	A + B (M)	2 (A + B)
	C	C (M)	2 (A + B)
	$\boxed{M-}$	C (M)	2 (A + B) - C
(3)	A	A	0.
	$\boxed{\times}$	A	0.
	B	B	0.
	$\boxed{M+}$	A·B (M)	A·B
	C	C (M)	A·B
	$\boxed{\times}$	C (M)	A·B
	D	D (M)	A·B
	$\boxed{M-}$	C·D (M)	A·B - C·D
	$\boxed{M^R_C}$	A·B - C·D (M)	A·B - C·D
	$\boxed{M-}$	A·B - C·D	0.
(4)	A	A	0.
	$\boxed{\times}$	A	0.
	B	B	0.
	$\boxed{=}$	A·B	0.
	C	C	0.
	$\boxed{M+}$	C (M)	C
	$\boxed{=}$	A·C (M)	C
	D	D (M)	C
	$\boxed{M-}$	D (M)	C - D
	$\boxed{=}$	A·D (M)	C - D
(5)	A	A	0.
	$\boxed{M+}$	A (M)	A
	B	B (M)	A

	Key Op.	Display	Memory
	$M+$	B (M)	A + B
	M^R_C	A + B (M)	A + B
	\times	A + B (M)	A + B
	M^R_C	A + B (M)	A + B
	$+$	$(A + B)^2$ (M)	A + B
	C	C (M)	A + B
	$=$	$(A + B)^2 + C$ (M)	A + B
(6)	1.0000001	1.0000001	0.
	$M+$	1.0000001 (M)	1.0000001
	99999999	99999999. (M)	1.0000001
	$M+$	0. ($\frac{M}{E}$)	1.0000001
	ON/C/CE	0. (M)	1.0000001
	M^R_C	1.0000001 (M)	1.0000001

10. Square root

(1)	A	A
	$\sqrt{\quad}$	\sqrt{A}
	B	B
(2)	A	A
	\times	A
	B	B
	$\sqrt{\quad}$	\sqrt{B}
	$=$	$A\sqrt{B}$
(3)	A	A
	\times	A
	$\sqrt{\quad}$	\sqrt{A}
	B	B
	$=$	A·B
(4)	$-$	0.
	A	A

	Key Op.	Display	Memory
	$\boxed{=}$	- A	
	$\boxed{\sqrt{\quad}}$	\sqrt{A} (E)	
(5)	A	A	0.
	$\boxed{M+}$	A (M)	A
	$\boxed{M^R}$ \boxed{C}	A (M)	A
	$\boxed{\div}$	A (M)	A
	B	B (M)	A
	$\boxed{+/-}$	- B (M)	A
	$\boxed{\sqrt{\quad}}$	\sqrt{B} (M) E	A
	$\boxed{ON/C/CE}$	0. (M)	A

11. Percentage calculation

(1)	A	A	
	$\boxed{\times}$	A	
	B	B	
	$\boxed{\%}$	$A \cdot B / 100$	
	C	C	
	$\boxed{\%}$	$A \cdot C / 100$	
	D	D	
	$\boxed{\%}$	$A \cdot D / 100$	
(2)	A	A	
	$\boxed{\%}$	A	
	B	B	
	$\boxed{\%}$	B	
	C	C	
	$\boxed{\%}$	C	
(3)	A	A	
	$\boxed{-}$	A	
	B	B	
	$\boxed{\%}$	$A - A \cdot B / 100$	

	Key Op.	Display	Memory
	$\square -$	$A - A \cdot B / 100$	
	$\square +$	$A - A \cdot B / 100$	
	C		
	$\square \%$	$\left(A - \frac{A \cdot B}{100}\right) + \frac{\left(A - \frac{A \cdot B}{100}\right) \cdot C}{100}$	
12. Key correction			
(1)	A	A	0.
	$\square \times$	A	0.
	$\square \div$	A	0.
	$\square -$	A	0.
	$\square +$	A	0.
	$\square \sqrt{\quad}$	\sqrt{A}	0.
	$\square M+$	$A + \sqrt{A} (M)$	$A + \sqrt{A}$
	$\square + / -$	$- (A + \sqrt{A}) (M)$	$A + \sqrt{A}$
	$\square M^R_C$	$A + \sqrt{A} (M)$	$A + \sqrt{A}$
	$\square M^R_C$	$A + \sqrt{A} (M)$	0.
	B	B	0.
	$\square +$	B	0.
	$\square -$	B	0.
	$\square \times$	B	0.
	$\square \div$	B	0.
	$\square =$	1 / B	0.
13. Others			
(1)	A	A	
	$\square +$	A	
	$\square =$	A	
(2)	A	A	
	$\square \times$	A	
	$\square \div$	A	
	$\square =$	1 / A	

	Key Op.	Display	Memory
(3)	A	A	
	\div	A	
	+	A	
	=	A	
(4)	A	A	
	\times	A	
	-	A	
	=	-A	
(5)	A	A	
	\div	A	
	-	A	
	=	-A	
(6)	A	A	
	\times	A	
	ON / C / CE	0.	
	B	B	
(7)	=	B	
	A	A	
	\times	A	
	B	B	
	ON / C / CE	0.	
	C	C	
	=	A·C	

14. TAX Calculation

	Key Op.	Display
(1)	A	A
	$\boxed{\text{SHIFT}}$	A $\boxed{\text{SHIFT}}$
	$\boxed{+ \text{TAX}}$	A $\boxed{\text{TAX}\%}$
(2)	$\boxed{\text{SHIFT}}$	0. $\boxed{\text{SHIFT}}$
	$\boxed{- \text{TAX}}$	A $\boxed{\text{TAX}\%}$
(3)	B	B
	$\boxed{+ \text{TAX}}$	B (1 + A / 100) $\boxed{+ \text{TAX}}$
	$\boxed{+ \text{TAX}}$	B · A / 100 $\boxed{\text{TAX}}$
	$\boxed{+ \text{TAX}}$	B (1 + A / 100) $\boxed{+ \text{TAX}}$
	$\boxed{+ \text{TAX}}$	B · A / 100 $\boxed{\text{TAX}}$
(4)	B	B
	$\boxed{- \text{TAX}}$	B / (1 + A / 100) $\boxed{- \text{TAX}}$
	$\boxed{- \text{TAX}}$	B - B / (1 + A / 100) $\boxed{\text{TAX}}$
	$\boxed{- \text{TAX}}$	B / (1 + A / 100) $\boxed{- \text{TAX}}$
	$\boxed{- \text{TAX}}$	B - B / (1 + A / 100) $\boxed{\text{TAX}}$

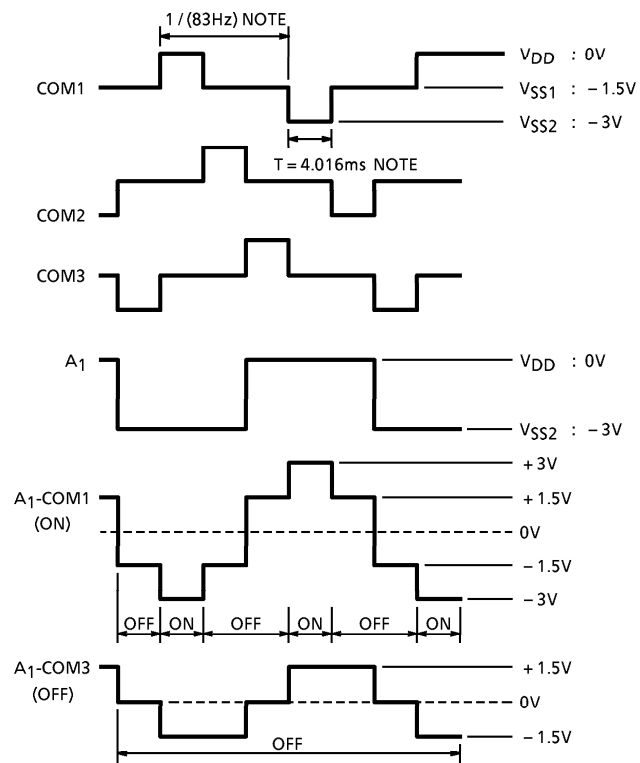
MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V _{SS1}	+0.3~ -2.2	V
Input Voltage	V _{IN}	+0.3~V _{DD1} -0.3	V
Operating Temperature	T _{opr}	+0.0~40	°C
Storage Temperature	T _{stg}	-55~125	°C

ELECTRICAL CHARACTERISTICS (V_{SS1} = -1.5V ± 0.2V, V_{SS2} = -3.0V ± 4.0V, V_{DD} = 0V, Ta = 25°C)

PARAMETER	SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V _{SS1}	—	—	—	-1.2	-1.5	-2.0	V	
VOLTAGE	Input "1"	V _{IH}	K ₂ ~K ₈ , RESET	—	V _{SS1} +0.4	—	V _{SS1}	V	
	Input "0"	V _{IL}	K ₂ ~K ₈ , RESET	—	0	—	-0.4	V	
	Output "1"	V _{OH}	Segment, Common	—	V _{SS2} +0.2	—	V _{SS2}	V	
	Output "0"	V _{OL}	Segment, Common	—	0	—	-0.2	V	
	Output "1"	V _{OH}	—	K ₁ ~K ₈ , RESET	—	V _{SS1} +0.2	—	V _{SS1}	V
	Output "0"	V _{OL}	—	K ₁ ~K ₆ , RESET	—	0	—	-0.2	V
Resistance	Output "1"	R _{OH}	Segment	V _{OUT} = V _{DD2} + 0.5V	—	—	70	kΩ	
	Output "0"	R _{OL}	Segment	V _{OUT} = -0.5V	—	—	70	kΩ	
	Output "1"	R _{OH}	Common	V _{OUT} = V _{DD2} + 0.5V	—	—	70	kΩ	
	Output "0"	R _{OL}	Common	V _{OUT} = -0.5V	—	—	70	kΩ	
	Pull Up	R _{KH}	—	K ₁ ~K ₈	V _{OUT} = 0V	60	400	1500	kΩ
		RESET	—	RESET	V _{OUT} = 0V	200	300	400	
Output "0"	R _{OL}	—	K ₁ ~K ₆	V _{OUT} = -0.5V	—	—	10	kΩ	
Supply Current 1 (On Display)	I _{DD1}	—	—	V _{SS1} = -1.5V (No Keys)	—	-2.2	-3.6	μA	
Supply Current 2 (Operation)	I _{DD2}	—	—	V _{SS1} = -1.2V (Peak OF A11 9√□)	—	-4.4	-6.6	μA	
Supply Current 3 (Off)	I _{DD3}	—	—	V _{SS1} = -1.5V (Off Status)	—	-0.5	-2.0	μA	
Oscillating Frequency	f _{osc} (WAIT)	—	—	V _{SS1} = -1.5V	On Display	5.4	9	12.6	kHz
	f _{osc} (OP)	—	—		On Operating	10.8	18	25.2	
Frame Frequency	f _F	—	—	V _{SS1} = -1.5V (Wait)	50	83	117	Hz	
Power off Timer	T timer	—	—	V _{SS1} = -1.5V	252	420	588	s	

WAVEFORMS FOR DISPLAY



NOTE : $f\phi = 9\text{kHz}$

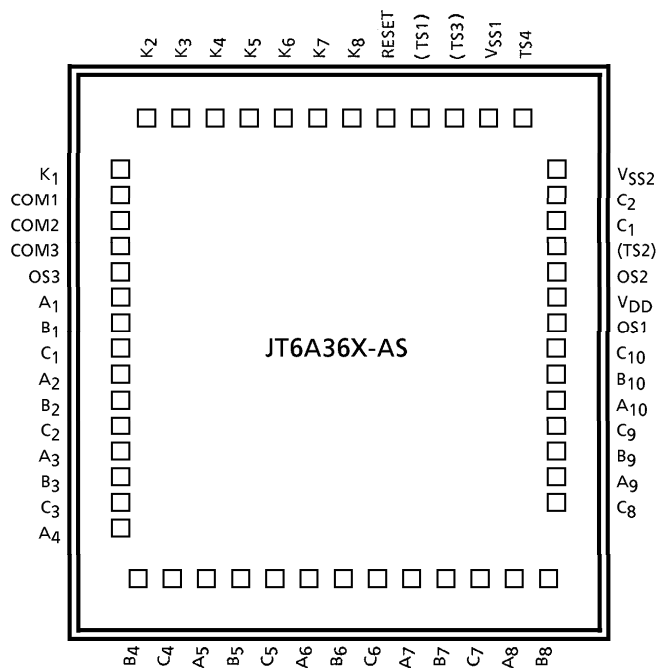
PAD LOCATION TABLE

(μm)

No.	NAME	X POINT	Y POINT
1	TS4	779	1086
2	V _{SS1}	628	1086
3	TS3	476	1086
4	TS1	324	1086
5	RESET	172	1086
6	K ₈	21	1086
7	K ₇	-131	1086
8	K ₆	-283	1086
9	K ₅	-434	1086
10	K ₄	-586	1086
11	K ₃	-738	1086
12	K ₂	-889	1086
13	K ₁	-1462	931
14	COM1	-1462	733
15	COM2	-1462	581
16	COM3	-1462	430
17	OS3	-1462	278
18	A ₁	-1462	126
19	B ₁	-1462	-26
20	C ₁	-1462	-177
21	A ₂	-1462	-329
22	B ₂	-1462	-481
23	C ₂	-1462	-632
24	A ₃	-1462	-784
25	B ₃	-1462	-936
26	C ₃	-1462	-1087
27	A ₄	-1462	-1239

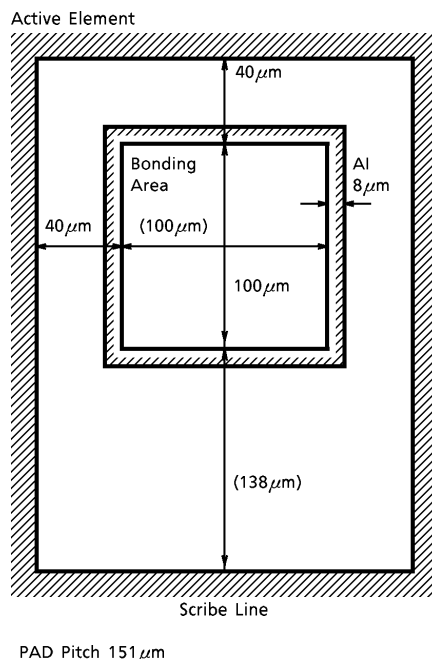
No.	NAME	X POINT	Y POINT
28	B ₄	-1097	-1412
29	C ₄	-946	-1412
30	A ₅	-794	-1412
31	B ₅	-642	-1412
32	C ₅	-491	-1412
33	A ₆	-339	-1412
34	B ₆	-187	-1412
35	C ₆	-36	-1412
36	A ₇	116	-1412
37	B ₇	268	-1412
38	C ₇	420	-1412
39	A ₈	571	-1412
40	B ₈	723	-1412
41	C ₈	1084	-1240
42	A ₉	1084	-1088
43	B ₉	1084	-936
44	C ₉	1084	-785
45	A ₁₀	1084	-633
46	B ₁₀	1084	-481
47	C ₁₀	1084	-330
48	OS1	1084	-178
49	V _{DD}	1084	-26
50	OS2	1084	125
51	TS2	1084	326
52	C ₁ (+)	1084	534
53	C ₂ (-)	1084	735
54	V _{SS2}	1084	937

CHIP LAYOUT



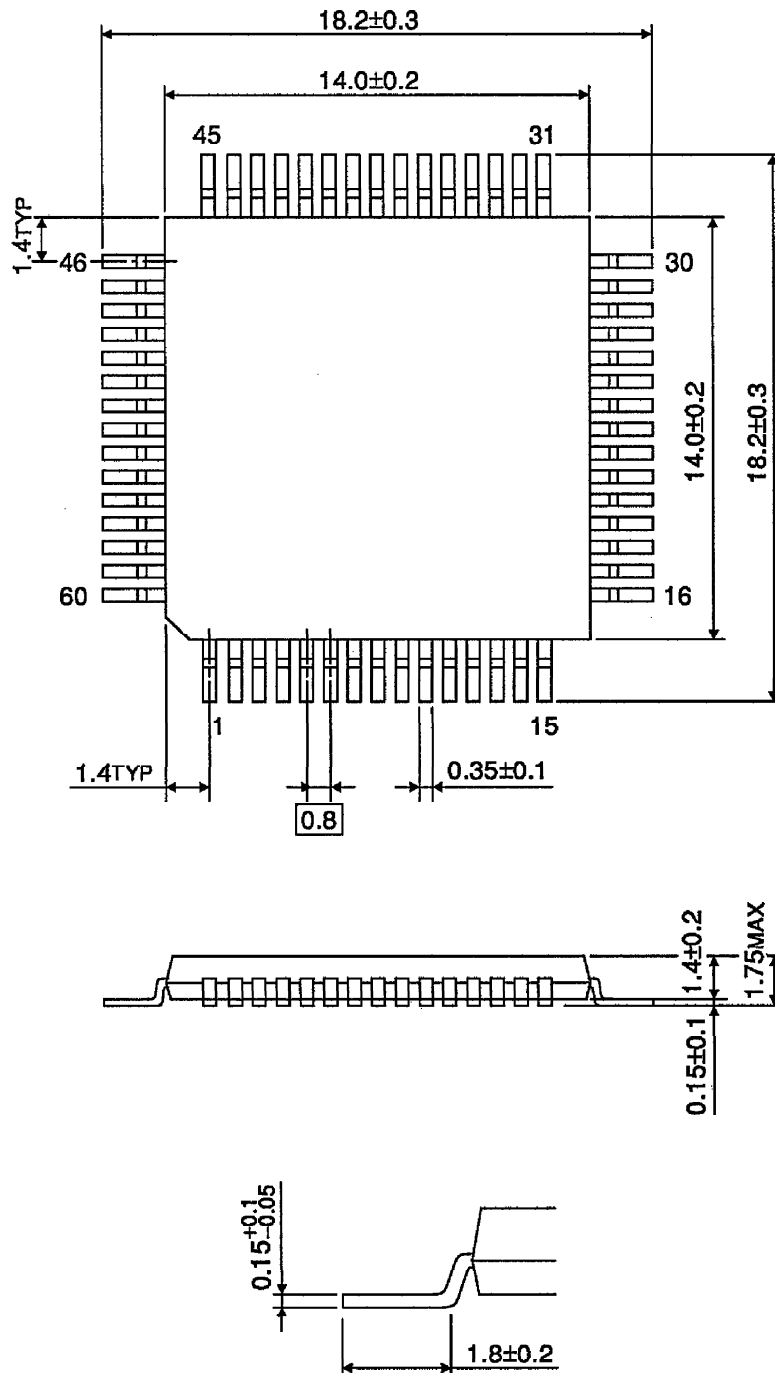
Chip size : 3.04 x 3.02 [mm]
 Chip thickness : 440 ± 30 [μm]
 Substrate : V_{DD}

PAD LAYOUT



OUTLINE DRAWING
LQFP60-P-1414-0.80

Unit : mm



Weight : 0.66g (Typ.)

GENERAL SPECIFICATION FOR CALCULATOR LSI BARE CHIP**1. Purpose**

This is to specify the quality standard for the integrated circuit produced by TOSHIBA CORPORATION (hereinafter referred as to VENDOR) to be delivered to PURCHASER.

2. Definition

This specification applies only to the calculator LSI bare chip produced by VENDOR and purchased by PURCHASER and defined the general specification items.

3. Priority of specifications

When the discrepancies or questions happen to the specifications and instructions provided by VENDOR, the priority shall be ranked as follows.

- 1) Individual specification for the calculator LSI bare chip.
(Both PURCHASER and VENDOR are confirmed by the special sheets.)
- 2) General specifications for the calculator LSI bare chip.
- 3) Other related specifications and standards.

4. Characteristics

To be shown in the individual specification sheets.

The individual specification shall consist of the following 4 items in principle.

- 1) Rated specifications.
- 2) Electrical characteristics.
- 3) Pin configuration & mechanical dimensions.
- 4) Others.

5. Inspection of product for delivery**5.1 Inspection lot**

- a) Inspection lot shall consist of products produced by same material under same design, through same production process, and same facilities and assured same quality by same quality assurance method, and lot number shall be put on all trays to be able to trace the lot history.
- b) The quantity of products per Inspection lot shall consist of all the same VENDOR's lot number.

5.2 Sampling plan

Statistical sampling and inspection shall be in accordance with MIL-STD-105D single sampling plans for normal inspections, general inspection level II.

The acceptable quality level (AQL) shall be specified in following table :

TEST ITEM	AQL (%)
Electrical	2.5
Visual	4.0

5.3 Electrical criteria

Criteria of Electrical Characteristics are prescribed in Attachment-1.

5.4 Visual criteria

Visual Criteria are prescribed in Attachment-2.

6. Incoming inspection

6.1 General

- a) PURCHASER's incoming inspection should be done within 15 days after PURCHASER receives the quantity of products in principle.
- b) PURCHASER shall report the results of incoming inspection to VENDOR and provide VENDOR with detailed data in failure rate and items regarding VENDOR's lot number respectively, if VENDOR demands the report from PURCHASER.

6.2 Inspection procedure

PURCHASER should do his incoming inspection according to the following procedure.

- a) First : Visual inspection should be done.
- b) Next : Electrical and other inspection should be done under condition with bare chip before going into PURCHASER's process.

7. Treatment for defective lot and products

Regarding the defective lot and defective products which are found through PURCHASER's incoming inspection, PURCHASER can be returned to VENDOR with detailed description on failures concerned.

However, if VENDOR cannot receive the defective items within 30 days after PURCHASER's incoming inspection, VENDOR should be able to make no reference to the defective problem.

8. Packing and labeling

- a) Dice shall be placed in die tray with the top metalization facting up in order.
- b) In principle, a pile consists of 5 trays and several piles are packed in a package. These piles and packages are indicated with printed labels as shown below.

Date	
Name	
Lot No.	
Net	
TOSHIBA MADE IN JAPAN	

- c) PURCHASER shall return these packing materials to VENDOR on VENDOR's demand.

9. Storage criteria

Solid state chips, unlike packaged devices, are non-hermetic devices normally fragile and small in physical size, and therefore, require special handling considerations as follows :

- 9.1 Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that alter their electrical, physical, or mechanical characteristics.
After the shipping container is opened, the chips must be stored under the following conditions :
 - A. Storage temperature, 40°C max.
 - B. Relative humidity, 50% max.
 - C. Clean, dust-free environment.
- 9.2 The user must exercise proper care when handling chips or wafers to prevent even the slightest physical damage to the chip.
- 9.3 During mounting and lead bounding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
- 9.4 After the chip has been mounted and bounded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces.
In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

10. Handling criteria

The user should find the following suggested precautions helpful in handling chips.

In any event, because of the extremely small size and fragile nature of chips, care should be taken in handling these devices.

10.1 Grounding

- a) Bonders, pellet pickup tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.
- b) Operator should be properly grounded.

10.2 In-process handling

- a) Assemblies or subassemblies of chips should be transported and stored in conductive carriers.
- b) All external leads of the assemblies or subassemblies should be shorted together.

VISUAL INSPECTION CRITERIA

1. Visual inspection magnification shall be 40 × in principle.

2. Defects defined :

2.1 Thickness

See the technical data sheet.

2.2 Chip and crack

A die shall be rejected if :

- a) Any crack of chip extends greater than 35 μ m in length into the inside of the scribble line. (see Fig.1)

2.3 Metallization

A die shall be rejected if :

- a) More than 25% of the designed area of the metallization is missing at any bonding pad.
- b) There is a short or break which affects electrical characteristics in any lead pattern. (see Fig.2)

2.4 Glass protection coat

A die shall be rejected if :

- a) It exhibits glass protection coat which covers more than 25% of any active bonding pad.

2.5 Attached foreign material

A die shall be rejected if :

- a) A die is covered by stains or attached foreign material which size is more than 5 times as large as a bonding pad area.
- b) It exhibits residual ink, stains or attached foreign material which covers more than 20% of any active bonding pad. (see Fig.3)

2.6 Others

A die shall be rejected if :

- a) There have no evident probed impression on the bonding pads.
- b) A inked die, defective die, is intermized.

3. Limit samples should be fized, if necessary.

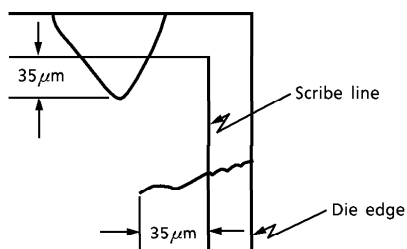


Fig.1

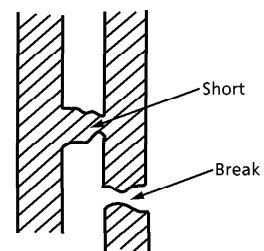


Fig.2 Lead pattern

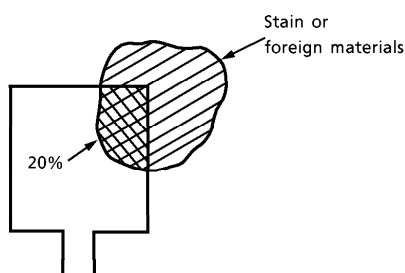
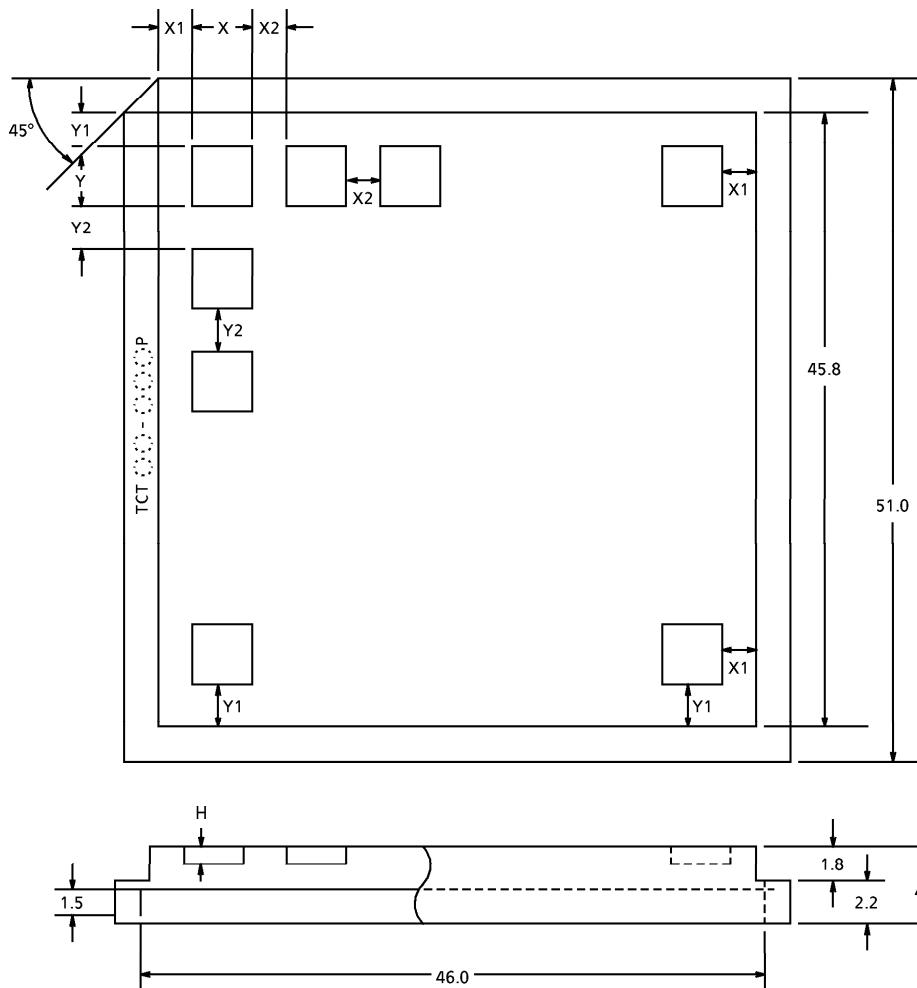


Fig.3

OUTSIDE DIMENSIONS OF CHIP TRAY



Unit : mm

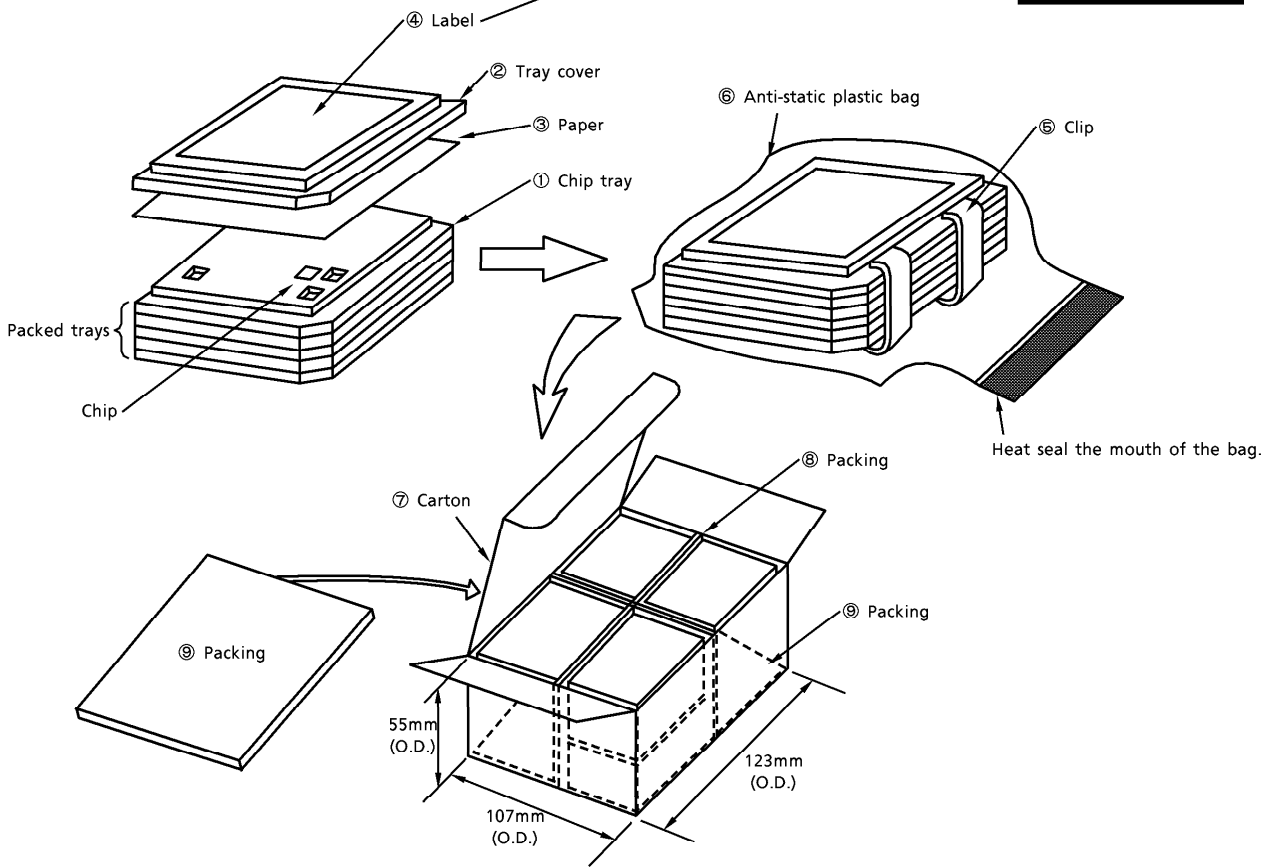
CHIP NAME	TRAY NAME	X	Y	(H)	No. OF POCKETS	X1	X2	Y1	Y2
JT6A36X-AS	TCT33-060P	3.30	3.30	0.60	10 × 10 (100)	1.900	1.000	1.900	1.000

Tray material :

Carbon-containing polypropylene

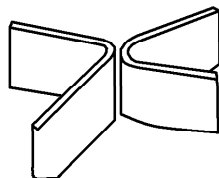
PACKING METHOD-1

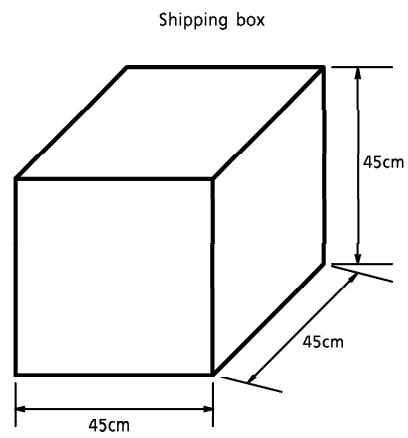
Name	
Net	
DATA	
Lot. No	
TOSHIBA MADE IN JAPAN	
7LY510C2	



Place eight bags of chip trays in each carton box ⑦. Lay one sheet of packing ⑨ (7UF44F) before closing the lid of the cart box. (See the diagram above.)

Prepare packing ⑨ by cutting 7UF44F into halves and folding each in half as shown below ; use them as inner partitions.



PACKING METHOD-2

- Inner box : Containing 20 boxes
- Weight : Approx. 15kg (including packing material)
- Material : Corrugated cardboard
- IC contents : $36 \times 5 \times 8 \times 20 = 28.8\text{kpcs}$.