


 IBM0165805B  
 IBM0165805P

**8M x 8 12/11 EDO DRAM**
**Features**

- 8,388,608 word by 8 bit organization
- Single  $3.3 \pm 0.3V$  power supply
- Extended Data Out
- $\overline{CAS}$  before  $\overline{RAS}$  Refresh
  - 4096 cycles/Retention Time
- $\overline{RAS}$  only Refresh
  - 4096 cycles/Retention Time
- 64ms Standard Power (SP) Retention Time
- 128ms Low Power (LP) Retention Time
- Hidden Refresh
- Self Refresh (400 $\mu$ A) - LP Version Only

- Read-Modify-Write
- Performance:

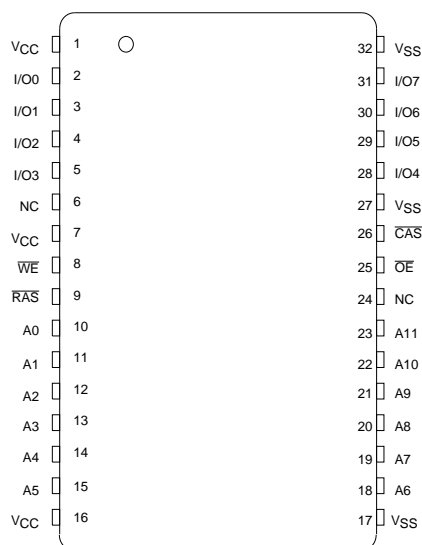
		-50	-60
$t_{RAC}$	$\overline{RAS}$ Access Time	50ns	60ns
$t_{CAC}$	$\overline{CAS}$ Access Time	13ns	15ns
$t_{AA}$	Column Address Access Time	25ns	30ns
$t_{RC}$	Cycle Time	84ns	104ns
$t_{HPC}$	Hyper Page Mode Cycle Time	20ns	25ns

- Max. Power Dissipation (-50)
  - Active: 504mW
  - Standby (SP version): 2.0 mA
  - Standby (LP version): 0.2 mA
- Package: SOJ-32 (400mil), TSOP-32 (400mil)

**Description**

The IBM0165805B/P is a dynamic RAM organized 8,388,608 words by 8 bits. This device is fabricated in IBM's most advanced CMOS silicon gate process technology. The circuit and process design allow this DRAM to achieve high performance and low power dissipation. The IBM0165805B/P operates with a single  $3.3 \pm 0.3V$  power supply, and interfaces directly with either TTL or CMOS levels. The 23 addresses required to access any bit of data are

multiplexed (12 are strobed with  $\overline{RAS}$ , 11 are strobed with  $\overline{CAS}$ ). They are packaged in a 32 pin plastic SOJ (400mil $\times$ 825mil), and a 32pin plastic TSOP type II (400mil $\times$ 825mil). The IBM0165805P parts are low power devices supporting Self Refresh and a 128ms retention time.

**Pin Assignments (Top View)**

**Pin Description**

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
$\overline{OE}$	Output Enable
I/O0 - I/O7	Data Input/output
$V_{CC}$	Power (+3.3V)
$V_{SS}$	Ground



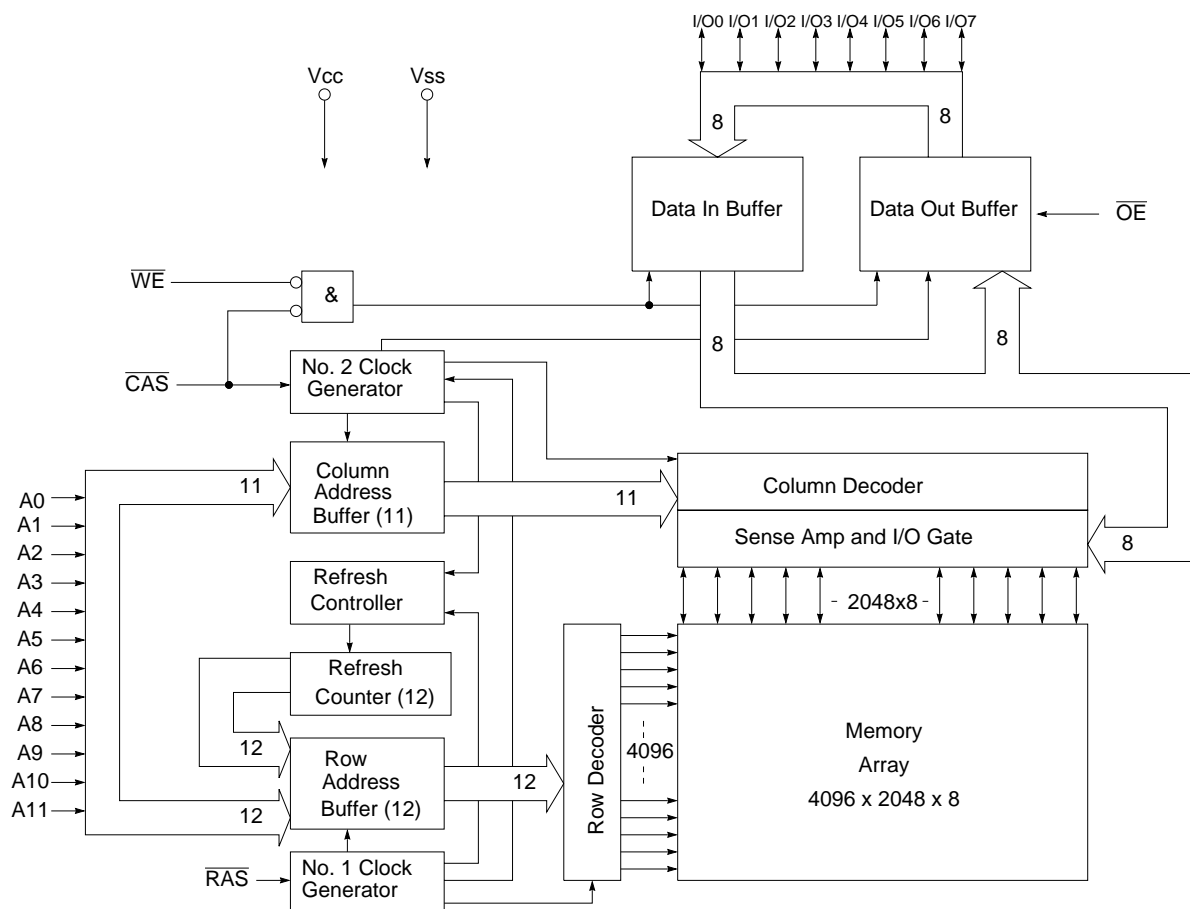
IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

### Ordering Information

Part Number	Power	Self Refresh	Power Supply	Speed	Package	Notes
IBM0165805BJ3D-50	SP	No	3.3V	50ns	400mil SOJ 32	1
IBM0165805BJ3D-60	SP	No	3.3V	60ns	400mil SOJ 32	1
IBM0165805BT3D-50	SP	No	3.3V	50ns	400mil TSOP 32	1
IBM0165805BT3D-60	SP	No	3.3V	60ns	400mil TSOP 32	1
IBM0165805PT3D-50	LP	Yes	3.3V	50ns	400mil TSOP 32	1
IBM0165805PT3D-60	LP	Yes	3.3V	60ns	400mil TSOP 32	1

1. SP = Standard Power version (IBM0165805B); LP = Low Power version (IBM0165805P)

### Block Diagram





## Truth Table

Function		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Row Address	Column Address	I/O0 - I/O7
Standby		H	H→X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col.	Data Out
Early-Write		L	L	L	X	Row	Col.	Data In
Delayed-Write		L	L	H→L	H	Row	Col.	Data In
Read-Modify-Write		L	L	H→L	L→H	Row	Col.	Data Out, Data In
EDO (Hyper Page) Mode Read	1st Cycle	L	H→L	H	L	Row	Col.	Data Out
	2nd Cycle	L	H→L	H	L	N/A	Col.	Data Out
EDO (Hyper Page) Mode Write	1st Cycle	L	H→L	L	X	Row	Col.	Data In
	2nd Cycle	L	H→L	L	X	N/A	Col.	Data In
EDO (Hyper Page) Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	L→H	Row	Col.	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	N/A	Col.	Data Out, Data In
$\overline{\text{RAS}}$ -Only Refresh		L	H	X	X	Row	N/A	High Impedance
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh		H→L	L	H	X	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col.	Data Out
	Write	L→H→L	L	L→H	X	Row	Col.	Data In
Self Refresh (LP version only)		H→L	L	H	X	X	X	High Impedance



IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
$V_{CC}$	Power Supply Voltage	-0.5 to 4.6	V	1
$V_{IN}$	Input Voltage	-0.5 to min ( $V_{CC}+0.5$ , 4.6)	V	1
$V_{OUT}$	Output Voltage	-0.5 to min ( $V_{CC}+0.5$ , 4.6)	V	1
$T_{OPR}$	Operating Temperature	0 to +70	°C	1
$T_{STG}$	Storage Temperature	-55 to +150	°C	1
$P_D$	Power Dissipation	1.0	W	1
$I_{OUT}$	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions ( $T_A=0$ to $70^\circ\text{C}$ )

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$V_{CC}$	Supply Voltage	3.0	3.3	3.6	V	1
$V_{IH}$	Input High Voltage	2.0	—	$V_{CC} + 0.3$	V	1, 2
$V_{IL}$	Input Low Voltage	-0.3	—	0.8	V	1, 2

1. All voltages referenced to  $V_{SS}$ .
2.  $V_{IH}$  may overshoot to  $V_{CC} + 2.0\text{V}$  for pulse widths of  $\leq 4.0\text{ns}$  with 3.3 Volt.  $V_{IL}$  may undershoot to  $-2.0\text{V}$  for pulse widths  $\leq 4.0\text{ns}$  with 3.3 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference

## Capacitance ( $T_A=0$ to $+70^\circ\text{C}$ , $V_{CC}=3.3 \pm 0.3\text{V}$ , $f=1\text{MHz}$ )

Symbol	Parameter	Min.	Max.	Units	Notes
$C_{I1}$	Input Capacitance (A0 - A11)	—	5	pF	
$C_{I2}$	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	—	7	pF	
$C_{I3}$	Data I/O Capacitance (I/O0 - I/O7)	—	7	pF	


**DC Electrical Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3 \pm 0.3\text{V}$ )

Symbol	Parameter	Min.	Max.	Units	Notes
$I_{CC1}$	Operating Current Average Power Supply Operating Current (RAS, CAS, Address Cycling: $t_{RC} = t_{RC \text{ min}}$ )	-50	—	140	mA 1, 2, 3
		-60	—	115	
$I_{CC2}$	Standby Current (TTL) Power Supply Standby Current (RAS = CAS = $V_{IH}$ )	—	2	mA	
$I_{CC3}$	RAS Only Refresh Current Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS = $V_{IH}$ ; $t_{RC} = t_{RC \text{ min}}$ )	-50	—	130	mA 1, 3
		-60	—	110	
$I_{CC4}$	EDO Mode Current Average Power Supply Current, Hyper Page Mode (RAS = $V_{IL}$ , CAS, Address Cycling: $t_{PC} = t_{PC \text{ min}}$ )	-50	—	100	mA 1, 2, 3
		-60	—	80	
$I_{CC5}$	Standby Current (CMOS) Power Supply Standby Current (RAS = CAS = $V_{CC} - 0.2\text{V}$ )	LP version	—	200	$\mu\text{A}$
		SP version	—	1	mA
$I_{CC6}$	CAS Before RAS Refresh Current Average Power Supply Current, CAS Before RAS Mode (RAS, CAS, Cycling: $t_{RC} = t_{RC \text{ min}}$ )	-50	—	140	mA 1, 2
		-60	—	115	
$I_{CC7}$	Self Refresh Current (LP version only) Average Power Supply Current during Self Refresh CBR cycle with RAS $\geq t_{RASS}$ (min); CAS held low; $WE = V_{CC} - 0.2\text{V}$ ; Addresses and $D_{IN} = V_{CC} - 0.2\text{V}$ or $0.2\text{V}$ .	—	400	$\mu\text{A}$	
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input ( $0.0 \geq V_{IN} \geq V_{CC}$ ), All Other Pins Not Under Test = 0V	-2	+2	$\mu\text{A}$	
$I_{O(L)}$	Output Leakage Current ( $D_{OUT}$ is disabled, $0.0 \geq V_{OUT} \geq V_{CC}$ )	-2	+2	$\mu\text{A}$	
$V_{OH}$	Output High Level (TTL) Output "H" Level Voltage ( $I_{OUT} = -2\text{mA}$ )	2.4	—	V	
$V_{OL}$	Output Low Level (TTL) Output "L" Level Voltage ( $I_{OUT} = +2\text{mA}$ )	—	0.4	V	

1.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
2.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
3. Column address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$  and  $\overline{\text{CAS}} = V_{IH}$ .



IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

## AC Characteristics ( $T_A=0$ to $+70^\circ\text{C}$ , $V_{CC}=3.3 \pm 0.3\text{V}$ )

1. An initial pause of  $100\mu\text{s}$  is required after power-up followed by 8  $\overline{\text{RAS}}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS before  $\overline{\text{RAS}}$  refresh cycles instead of 8  $\overline{\text{RAS}}$  only refresh cycles is required.
2. AC measurements assume  $t_T=2\text{ns}$ .
3.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
4. Valid column addresses are only A0 through A10.

## Read, Write, Read-Modify-Write and Refresh Cycle (Common Parameters)

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{RC}$	Random Read or Write Cycle Time	84	—	104	—	ns	1
$t_{RP}$	$\overline{\text{RAS}}$ Precharge Time	30	—	40	—	ns	
$t_{CP}$	$\overline{\text{CAS}}$ Precharge Time	8	—	10	—	ns	
$t_{RAS}$	$\overline{\text{RAS}}$ Pulse Width	50	100k	60	100k	ns	1
$t_{CAS}$	$\overline{\text{CAS}}$ Pulse Width	8	100k	10	100k	ns	1
$t_{ASR}$	Row Address Setup Time	0	—	0	—	ns	
$t_{RAH}$	Row Address Hold Time	7	—	10	—	ns	
$t_{ASC}$	Column Address Setup Time	0	—	0	—	ns	
$t_{CAH}$	Column Address Hold Time	7	—	10	—	ns	
$t_{RCD}$	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	11	37	14	45	ns	2
$t_{RAD}$	$\overline{\text{RAS}}$ to Col. Address Delay Time	9	25	12	30	ns	3
$t_{RSH}$	$\overline{\text{RAS}}$ Hold Time	8	—	10	—	ns	
$t_{CSH}$	$\overline{\text{CAS}}$ Hold Time	40	—	50	—	ns	1
$t_{CRP}$	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	ns	1
$t_{DZO}$	$\overline{\text{OE}}$ Delay Time From $D_{IN}$	0	—	0	—	ns	4
$t_{DZC}$	$\overline{\text{CAS}}$ Delay Time From $D_{IN}$	0	—	0	—	ns	4
$t_T$	Transition Time (Rise and Fall)	1	50	1	50	ns	5

1. In a Test Mode Read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$  are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the  $t_{RCD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
3. Operation within the  $t_{RAD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .
4. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
5. AC measurements assume  $t_T = 2\text{ns}$



## Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{WCS}$	Write Command Set Up Time	0	—	0	—	ns	1
$t_{WCH}$	Write Command Hold Time	7	—	10	—	ns	
$t_{WP}$	Write Command Pulse Width	7	—	10	—	ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	8	—	10	—	ns	
$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	8	—	10	—	ns	
$t_{OED}$	$\overline{OE}$ to $D_{IN}$ Delay Time	13	—	15	—	ns	2
$t_{DS}$	$D_{IN}$ Setup Time	0	—	0	—	ns	3
$t_{DH}$	$D_{IN}$ Hold Time	7	—	10	—	ns	3

- $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$ , and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$  (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- Either  $t_{CDD}$  or  $t_{OED}$  must be satisfied.
- These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in Read-Modify-Write cycles.



IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

## Read Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{RAC}$	Access Time from $\overline{RAS}$	—	50	—	60	ns	1, 2, 3, 5
$t_{CAC}$	Access Time from $\overline{CAS}$	—	13	—	15	ns	1, 2, 5
$t_{AA}$	Access Time from Address	—	25	—	30	ns	1, 2, 5
$t_{OEA}$	Access Time From $\overline{OE}$	—	13	—	15	ns	1, 5
$t_{RCS}$	Read Command Setup Time	0	—	0	—	ns	
$t_{RCH}$	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	6
$t_{RRH}$	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	ns	1
$t_{CLZ}$	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	5
$t_{OEZ}$	Output Buffer Turn-Off Delay From $\overline{OE}$	0	13	0	15	ns	7
$t_{CDD}$	$\overline{CAS}$ to $D_{IN}$ Delay Time	13	—	15	—	ns	4
$t_{OFF}$	Output Buffer Turn-Off Delay	0	13	0	15	ns	7
$t_{OES}$	$\overline{OE}$ Setup Time Prior to $\overline{CAS}$	5	—	5	—	ns	
$t_{ORD}$	$\overline{OE}$ Setup Time Prior to $\overline{RAS}$ (Hidden Refresh)	0	—	0	—	ns	

1. In a Test Mode Read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$  are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the  $t_{RCD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
3. Operation within the  $t_{RAD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .
4. Either  $t_{CDD}$  or  $t_{OED}$  must be satisfied.
5. Measured with the specified current load and 100pF.
6. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
7.  $t_{OFF}(\text{max.})$  and  $t_{OEZ}(\text{max.})$  define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.





## Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{RWC}$	Read-Modify-Write Cycle Time	109	—	135	—	ns	
$t_{RWD}$	$\overline{RAS}$ to $\overline{WE}$ Delay Time	65	—	79	—	ns	1
$t_{CWD}$	$\overline{CAS}$ to $\overline{WE}$ Delay Time	28	—	34	—	ns	1
$t_{AWD}$	Column Address to $\overline{WE}$ Delay Time	40	—	49	—	ns	1
$t_{OEH}$	$\overline{OE}$ Command Hold Time	7	—	10	—	ns	

1.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$ , and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$  (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

## Extended Data Out (Hyper Page) Mode Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{HCAS}$	$\overline{CAS}$ Pulse Width (Hyper Page Mode)	8	100K	10	10K	ns	
$t_{HPC}$	Hyper Page Mode Cycle Time (Read/Write)	20	—	25	—	ns	
$t_{HPRWC}$	Hyper Page Mode Read Modify Write Cycle Time	54	—	66	—	ns	
$t_{DOH}$	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	ns	
$t_{WHZ}$	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	10	ns	
$t_{WPZ}$	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	7	—	10	—	ns	
$t_{CPRH}$	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	27	—	35	—	ns	
$t_{CPA}$	Access Time from $\overline{CAS}$ Precharge	—	27	—	35	ns	1
$t_{RASP}$	Hyper Page Mode $\overline{RAS}$ Pulse Width	50	200K	60	200K	ns	
$t_{OEP}$	$\overline{OE}$ High Pulse Width	5	—	10	—	ns	
$t_{OEHC}$	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	5	—	10	—	ns	

1. Measured with the specified current load and 100pF at  $V_{OL} = 0.8V$  and  $V_{OH} = 2.0V$ .



IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

### Self Refresh Cycle - Low Power Version Only

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{RASS}$	$\overline{RAS}$ Pulse Width During Self Refresh Cycle	100	—	100	—	$\mu$ s	1
$t_{RPS}$	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	84	—	104	—	ns	1
$t_{CHS}$	$\overline{CAS}$ Hold Time During Self Refresh Cycle	-50	—	-50	—	ns	1

- When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:  
 If row addresses are being refreshed in an EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.  
 If row addresses are being refreshed in any other manner (ROR- Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

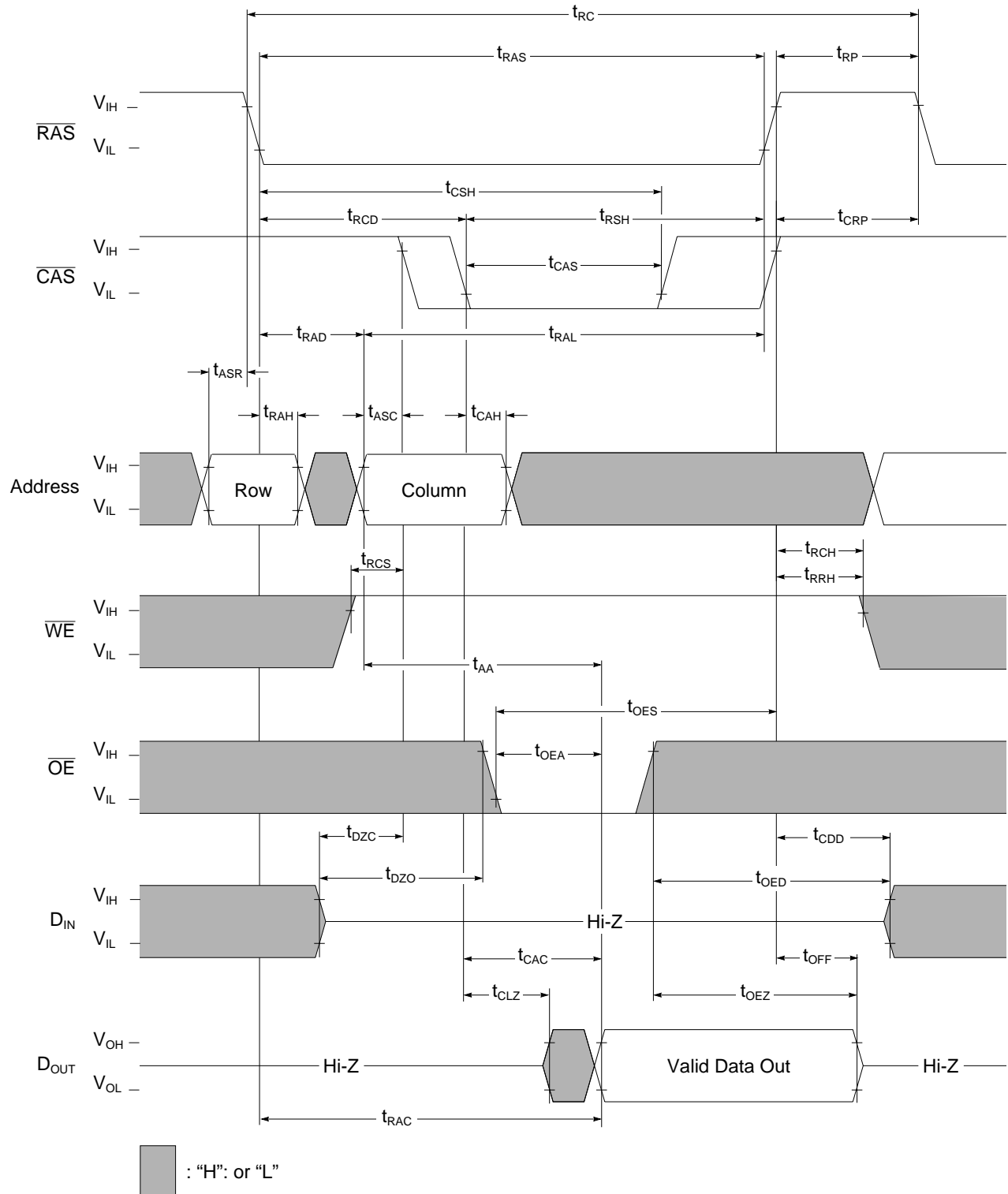
### Refresh Cycle

Symbol	Parameter	-50		-60		Units	Notes	
		Min.	Max.	Min.	Max.			
$t_{CSR}$	$\overline{CAS}$ Setup Time ( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns		
$t_{CHR}$	$\overline{CAS}$ Hold Time ( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	10	—	ns		
$t_{WRP}$	$\overline{WE}$ Setup Time ( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	10	—	ns		
$t_{WRH}$	$\overline{WE}$ Hold Time ( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	10	—	ns		
$t_{RPC}$	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns		
$t_{REF}$	Refresh Period	SP version	—	64	—	64	ms	1
		LP version	—	128	—	128		

- 8192 cycles for RAS Only Refresh; 4096 cycles for CBR Refresh.



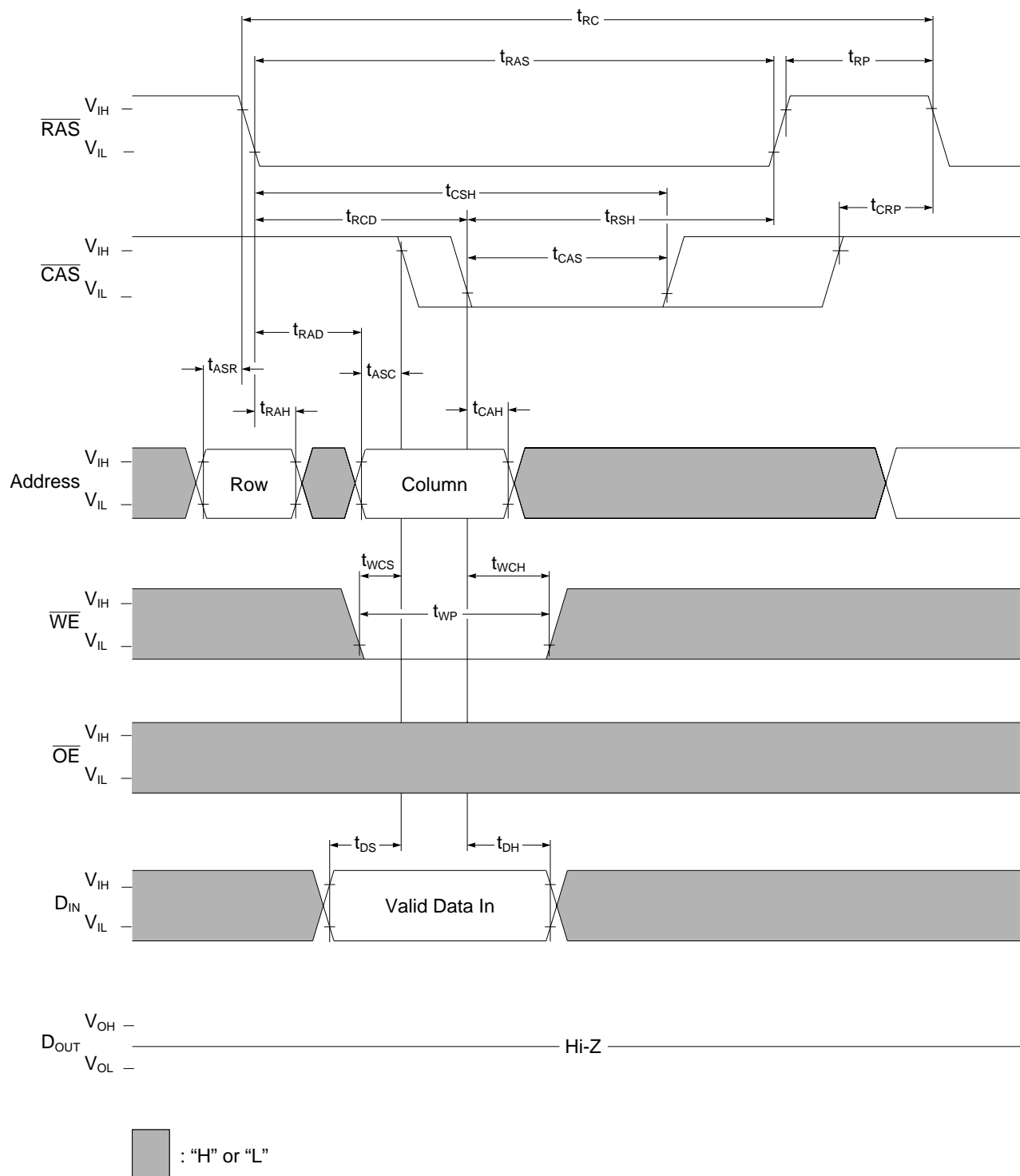
### Read Cycle





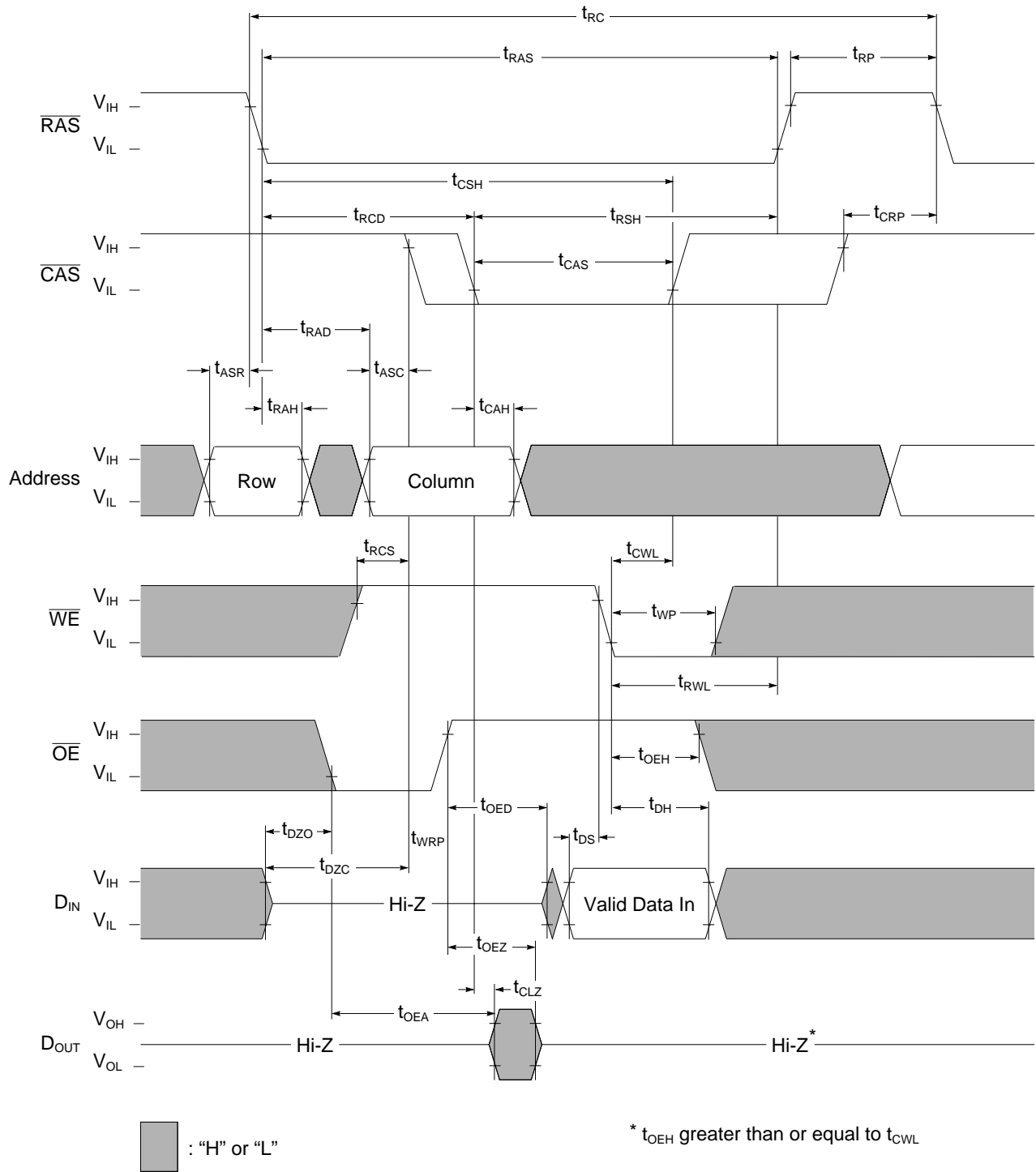
IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

### Write Cycle (Early Write)





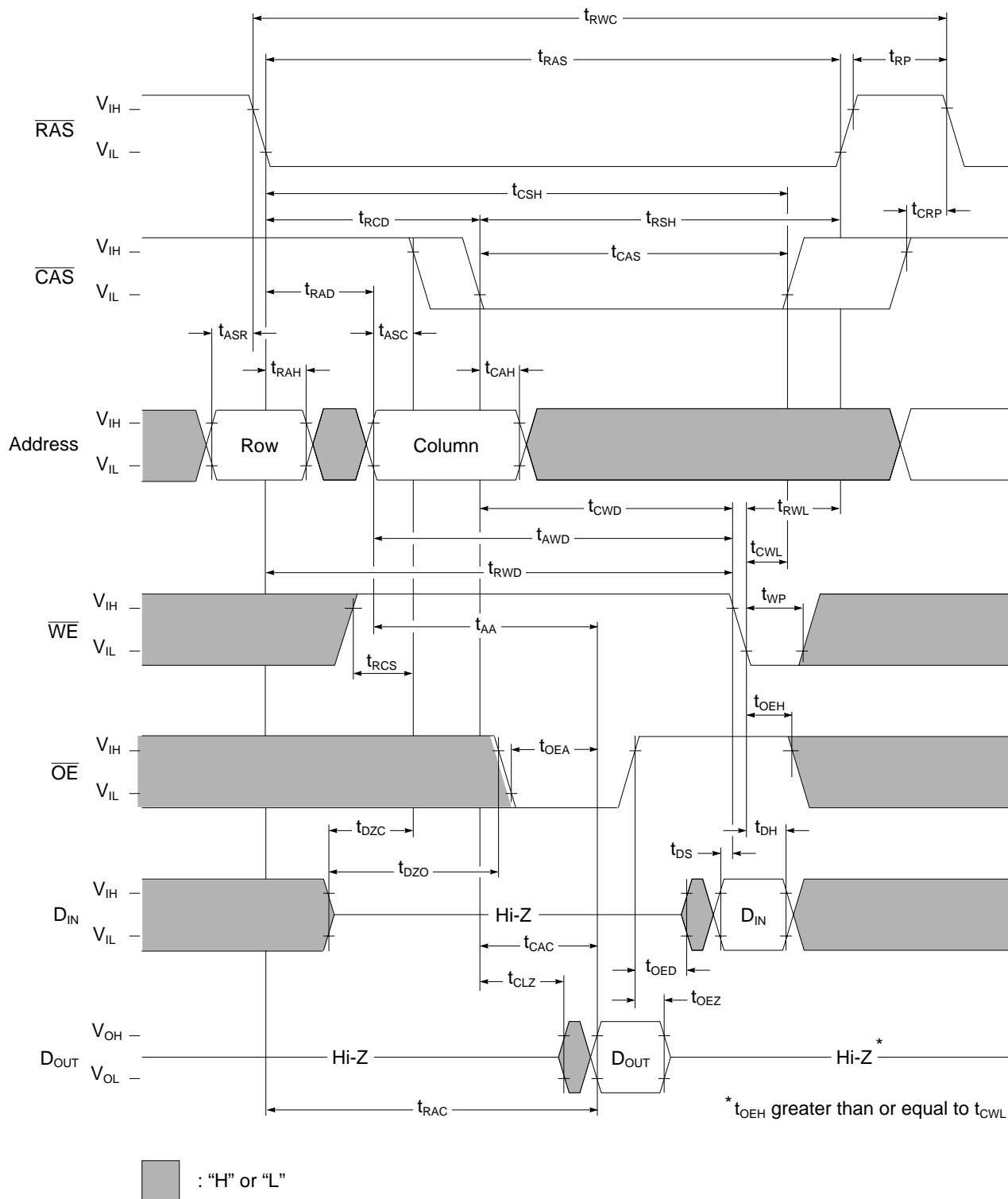
### Write Cycle (Delayed Write)





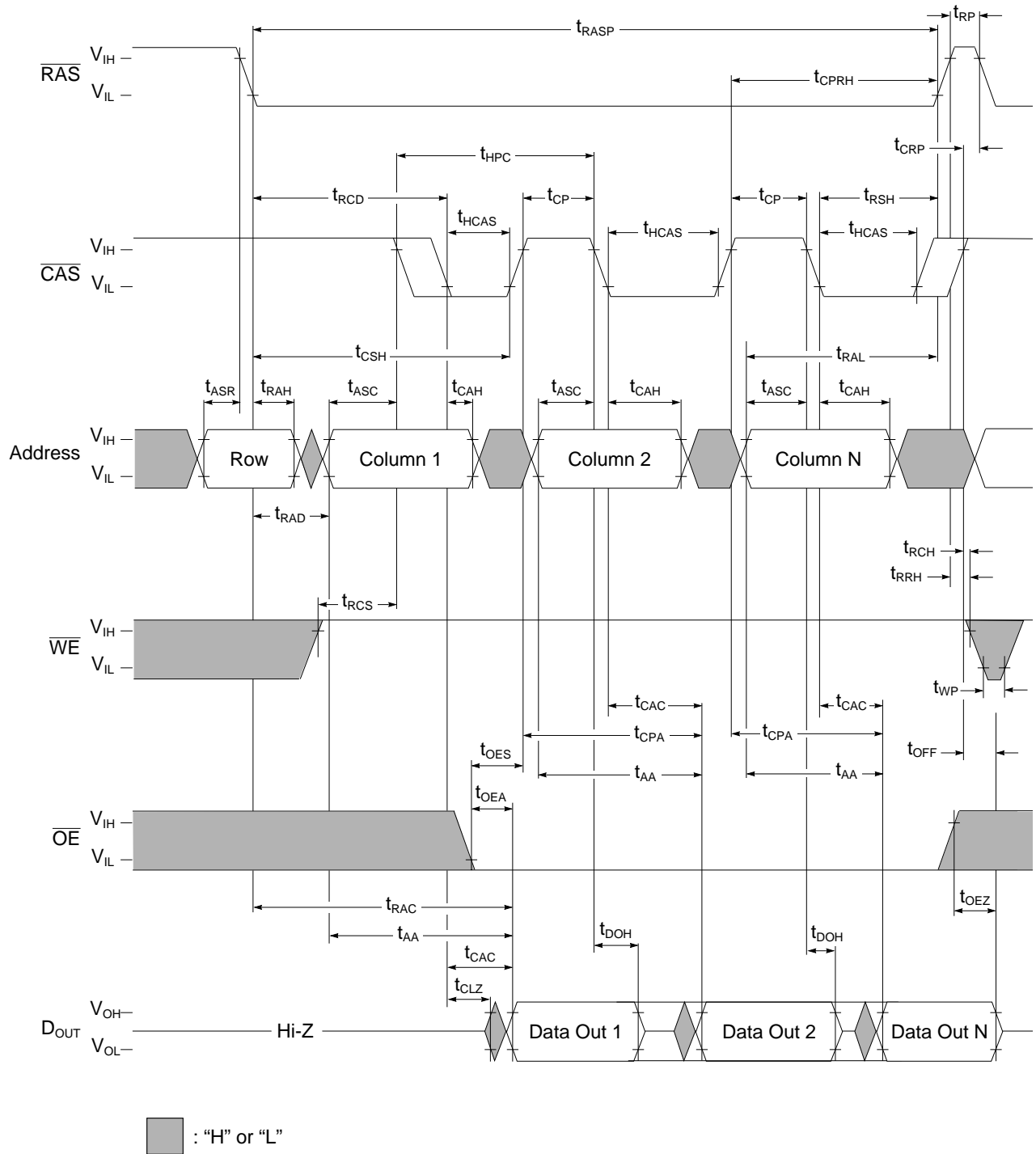
IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

### Read-Modify-Write Cycle





### EDO (Hyper Page) Mode Read Cycle

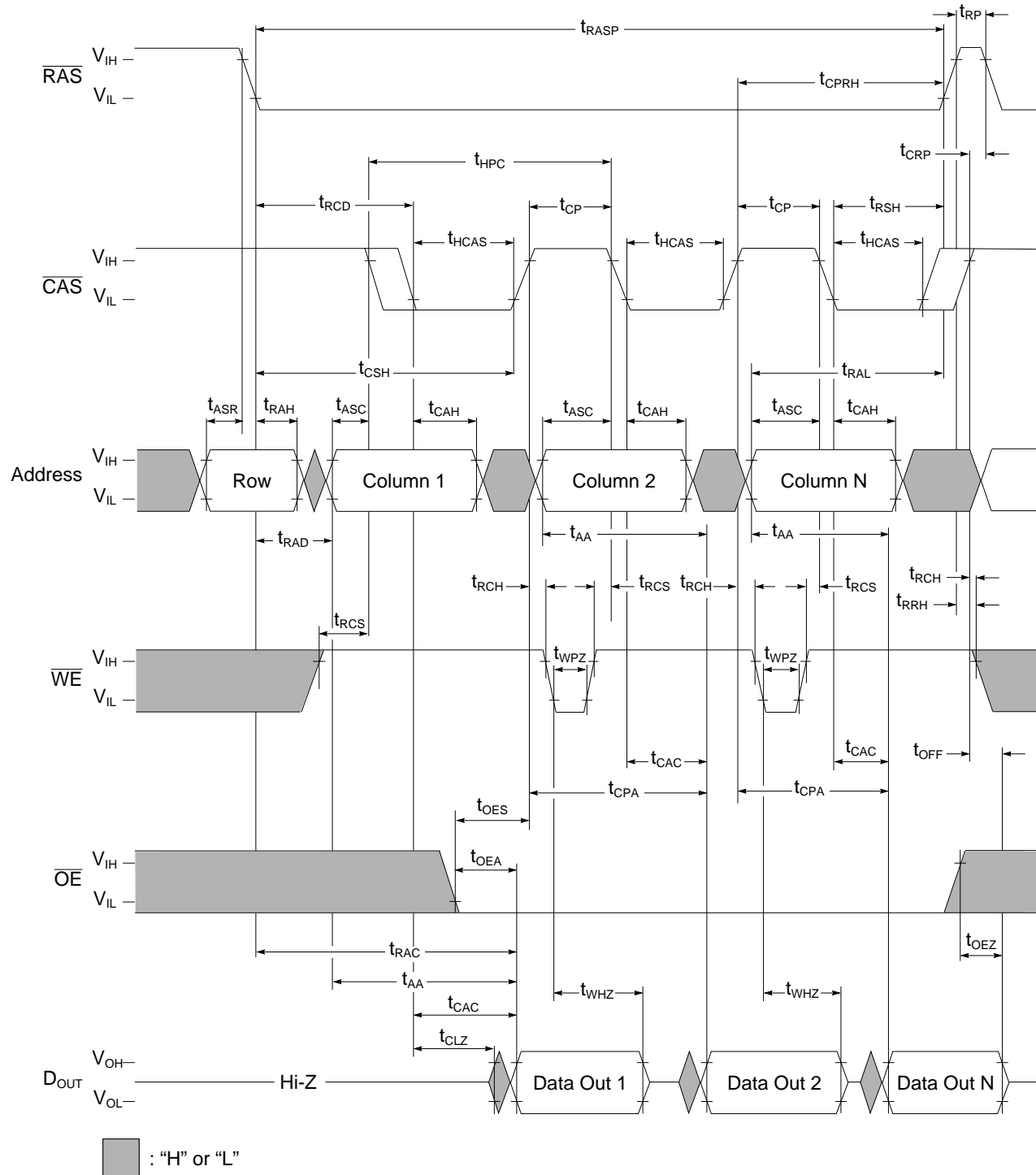








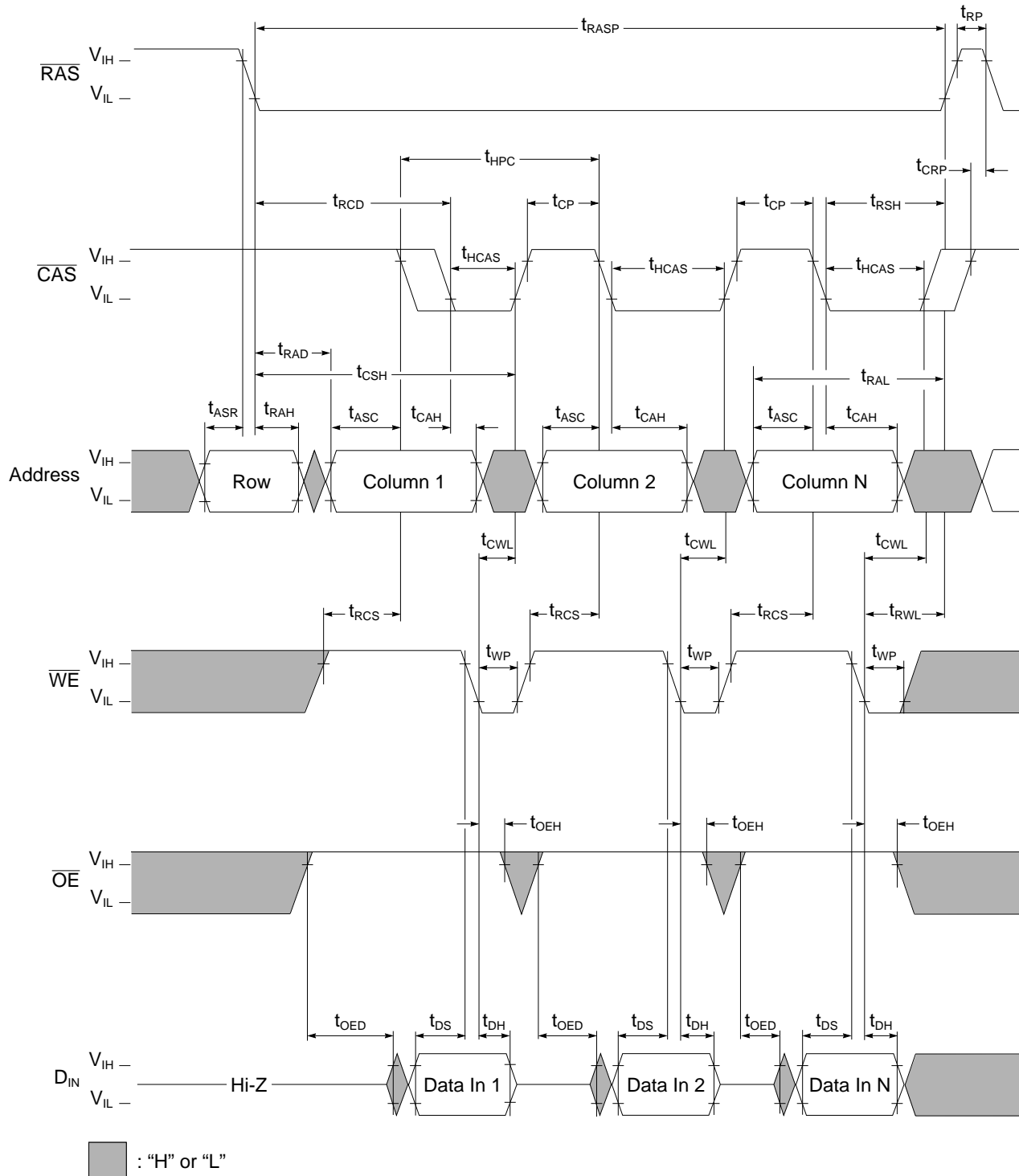
### EDO (Hyper Page) Mode Read Cycle ( $\overline{WE}$ Control)







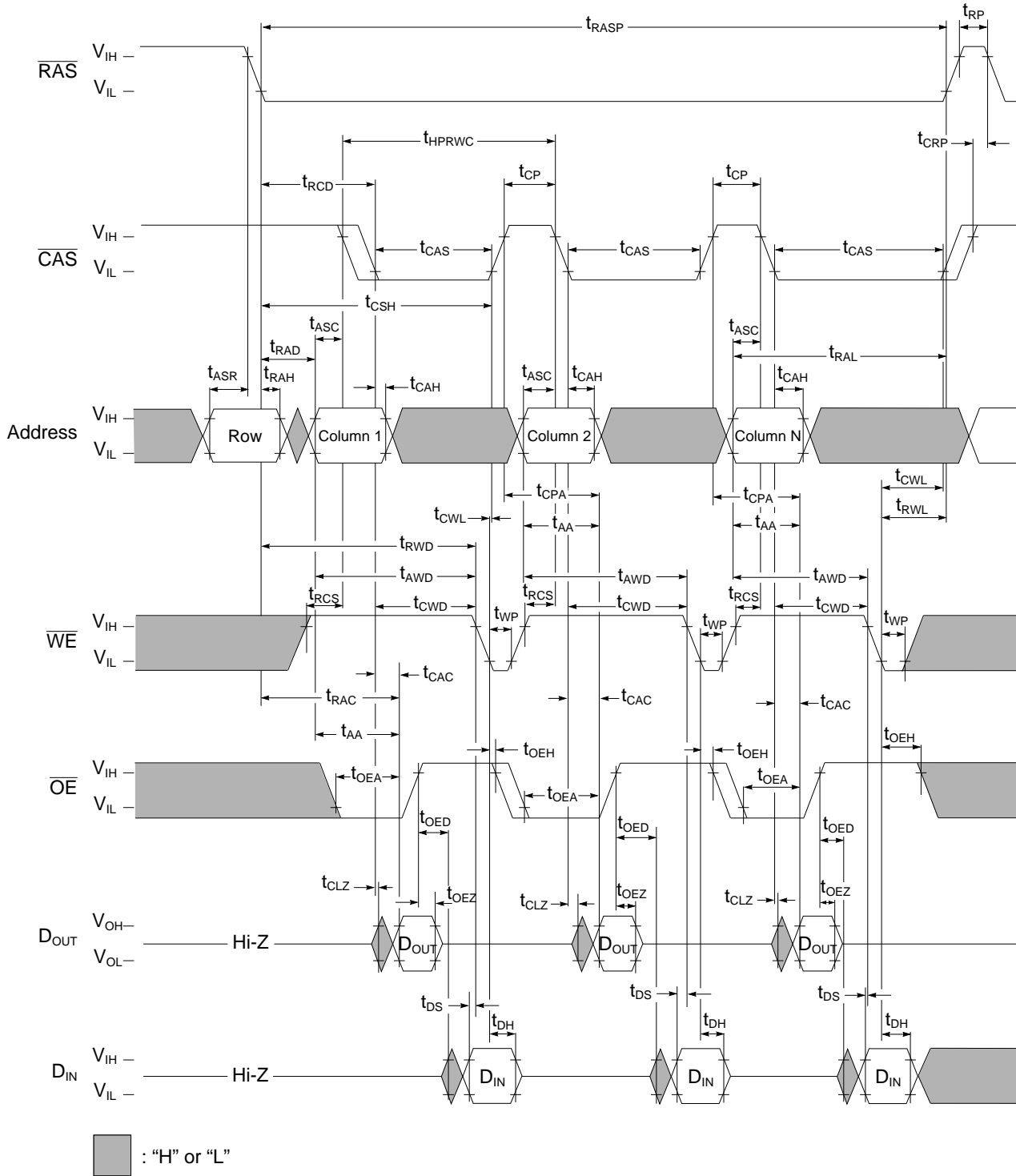
### EDO (Hyper Page) Mode Late Write Cycle





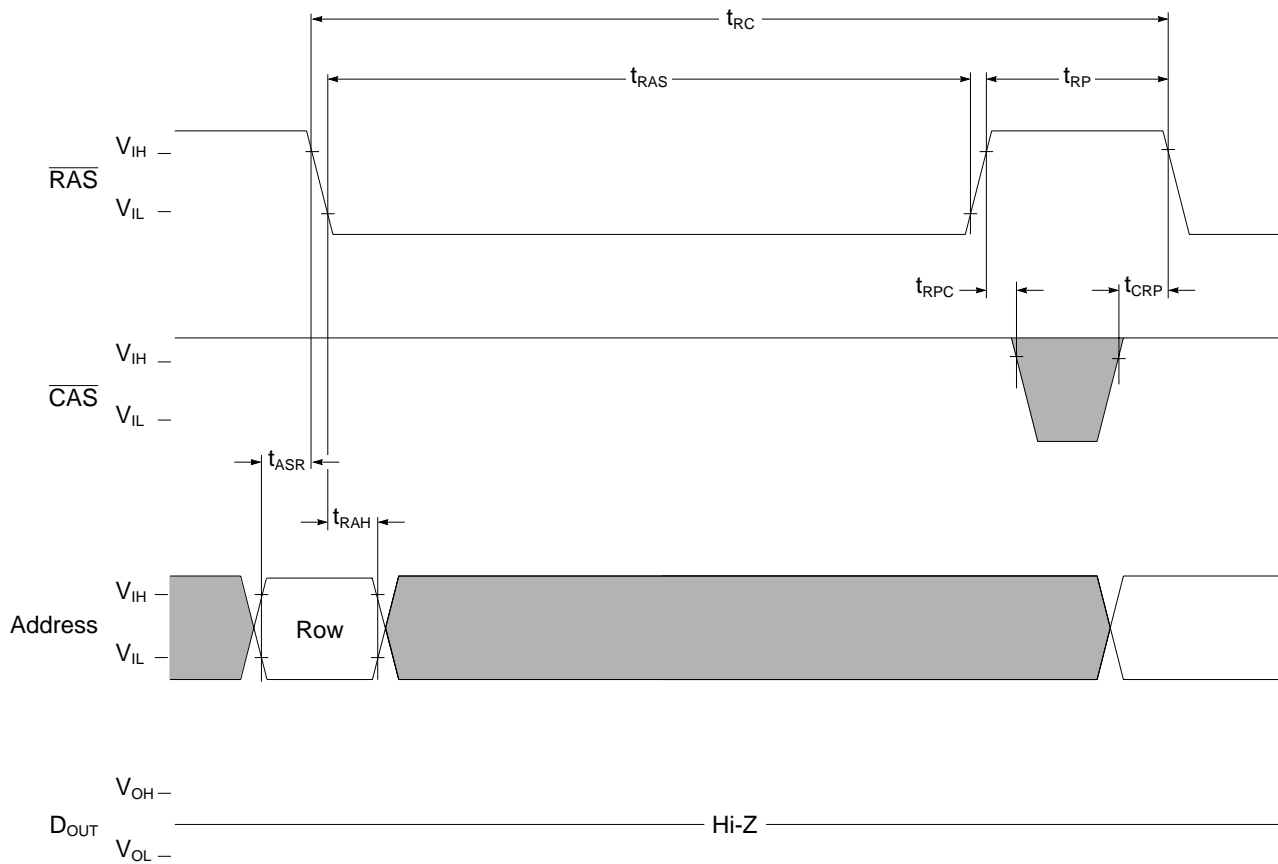
IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM


### EDO (Hyper Page) Mode Read Modify Write Cycle





**RAS Only Refresh Cycle**



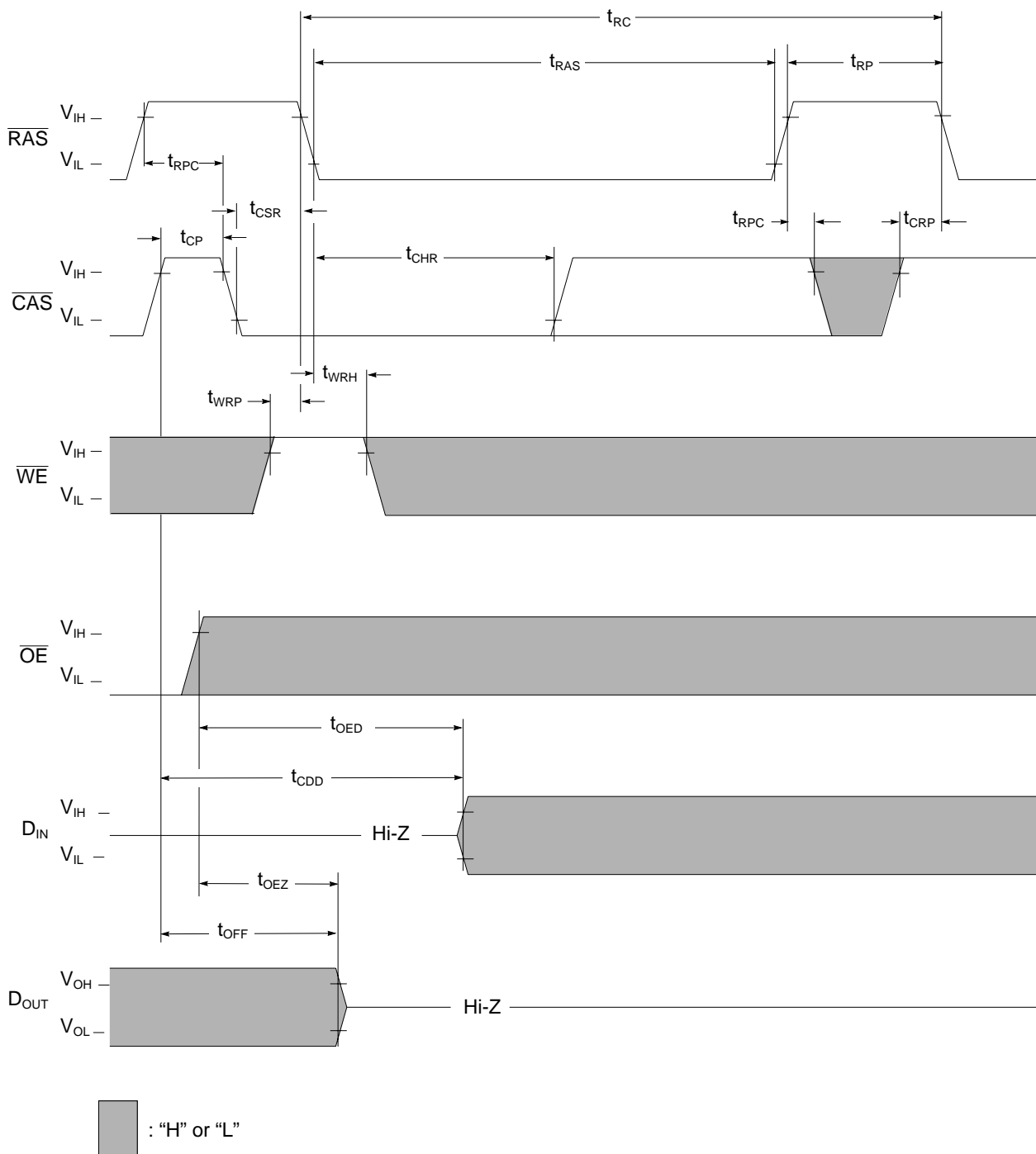
 : "H" or "L"

NOTE:  $\overline{WE}$ ,  $\overline{OE}$  and D<sub>IN</sub> are "H" or "L"



IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

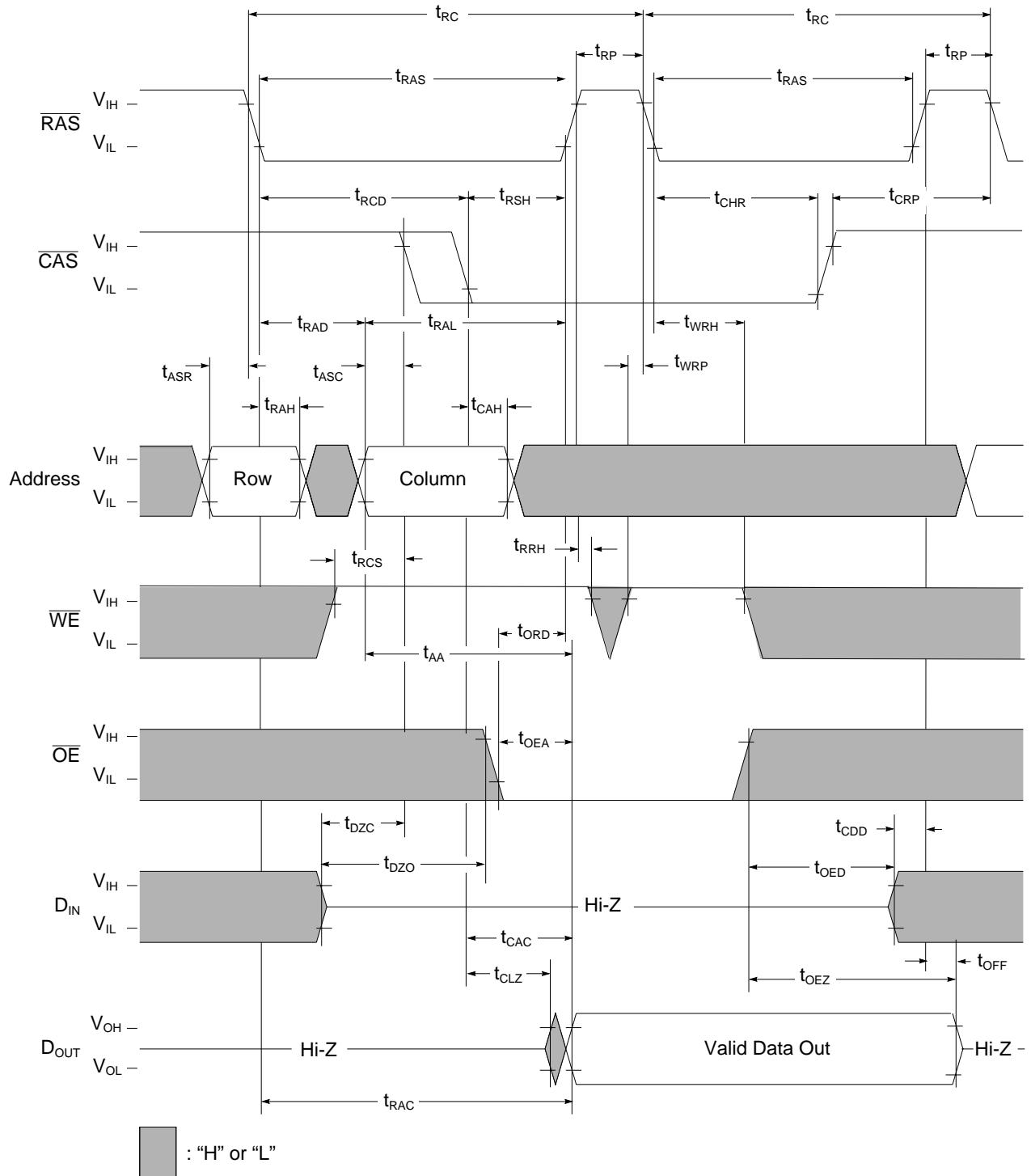
### $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



NOTE: Address is "H" or "L"



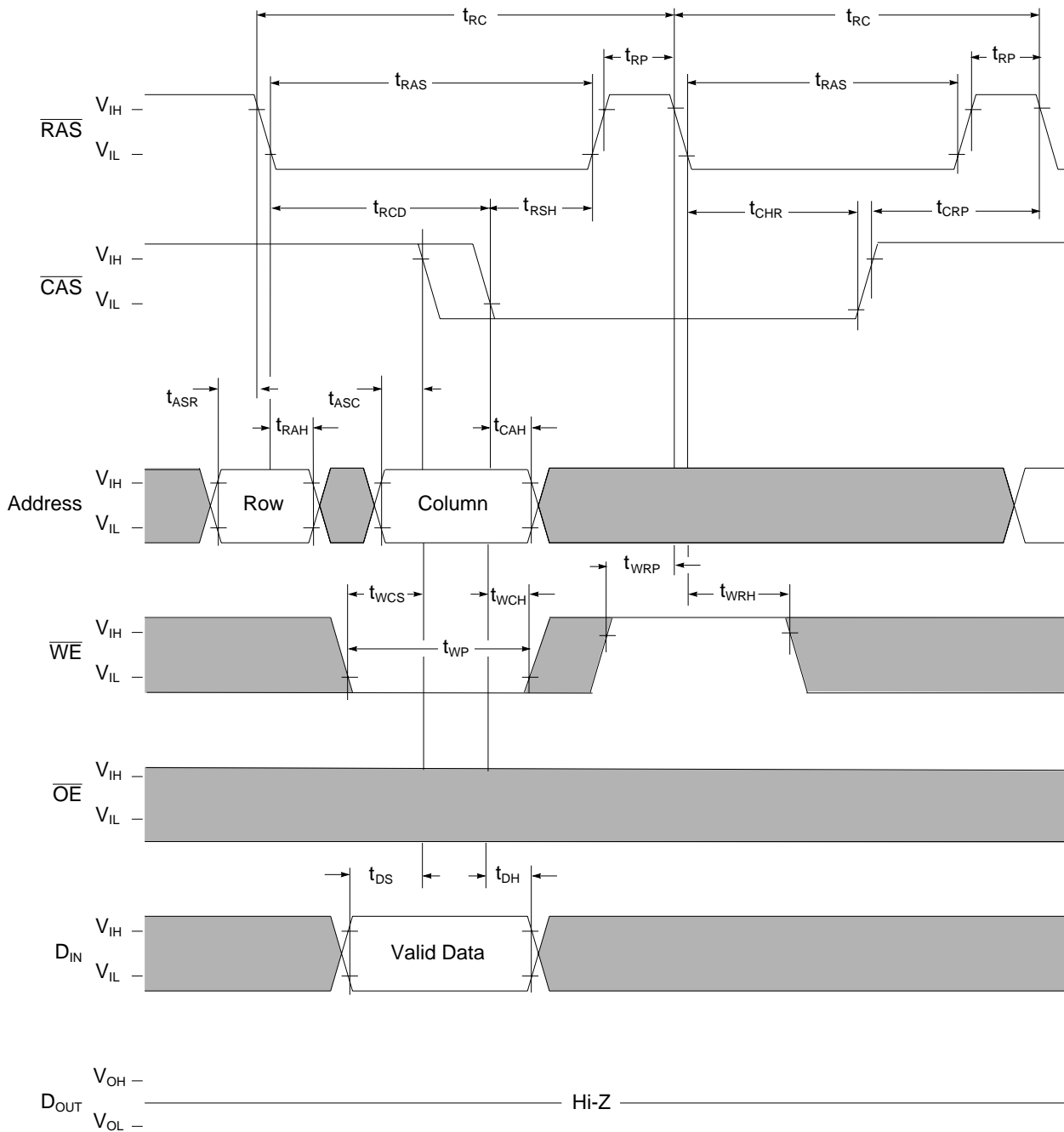
### Hidden Refresh Cycle (Read)






IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

### Hidden Refresh Cycle (Write)

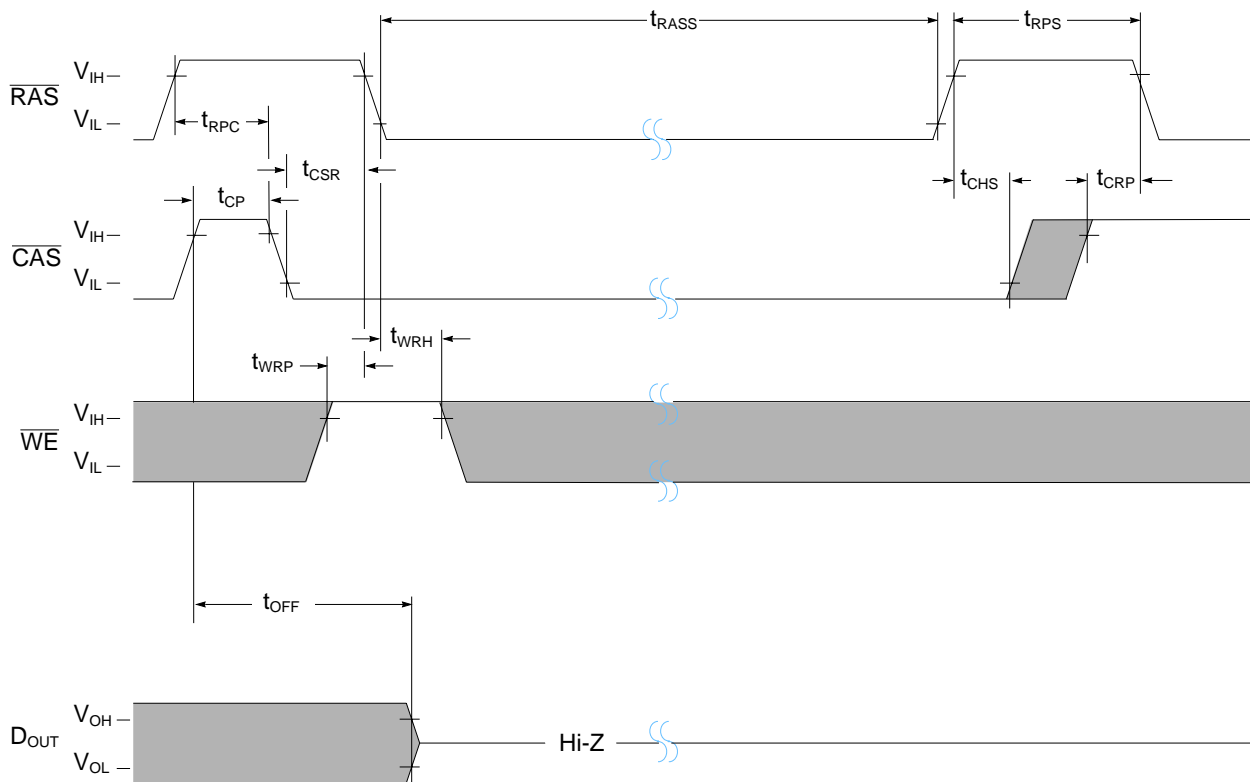



 : "H" or "L"





**Self Refresh Cycle (Sleep Mode) - Low Power version only**



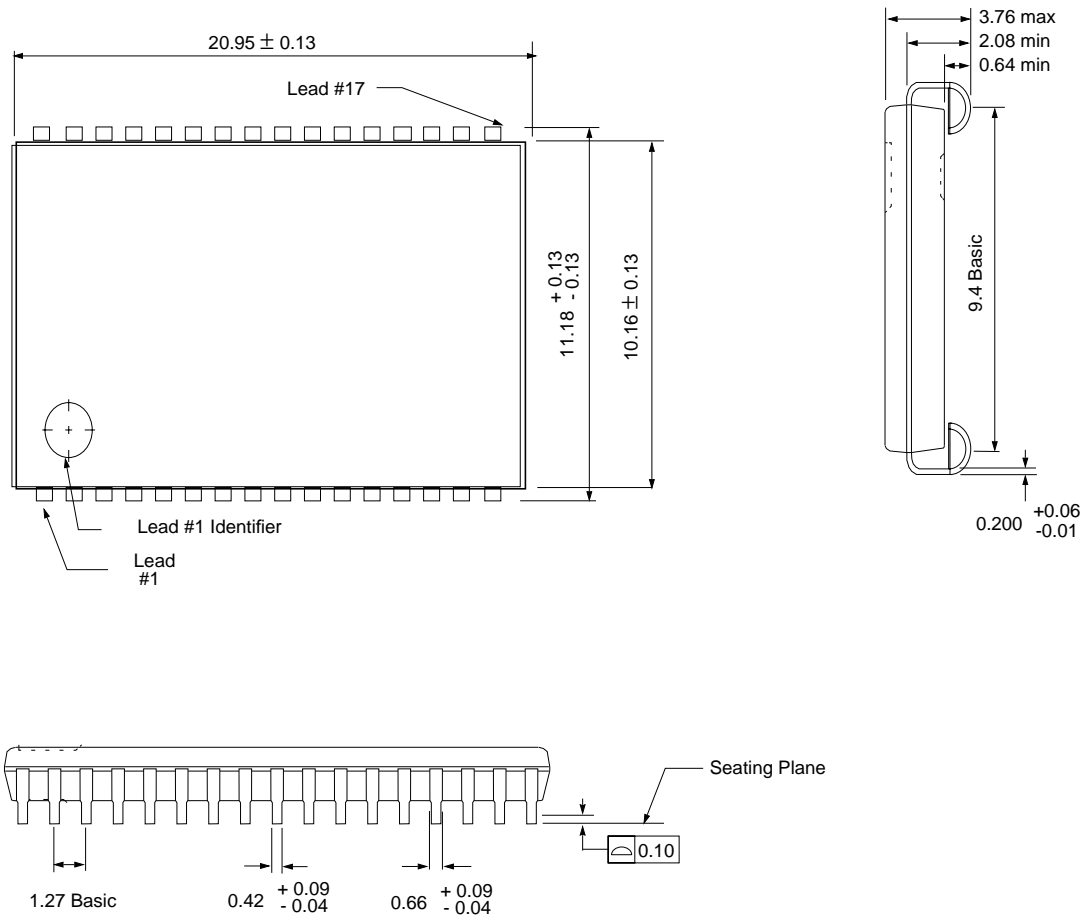
 : "H" or "L"

NOTE: Address and OE are "H" or "L"  
 Once  $t_{RASS}$  (min) is provided and RAS remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."



IBM0165805B  
IBM0165805P  
8M x 8 12/11 EDO DRAM

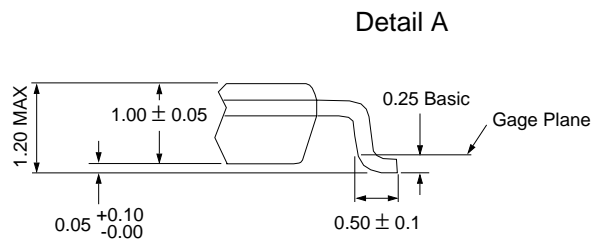
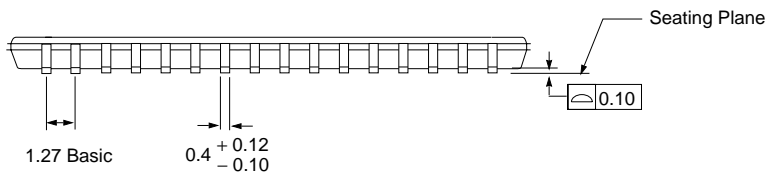
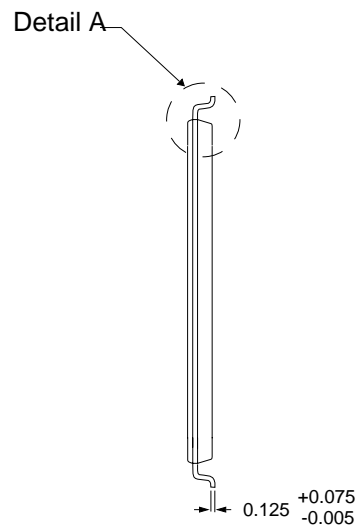
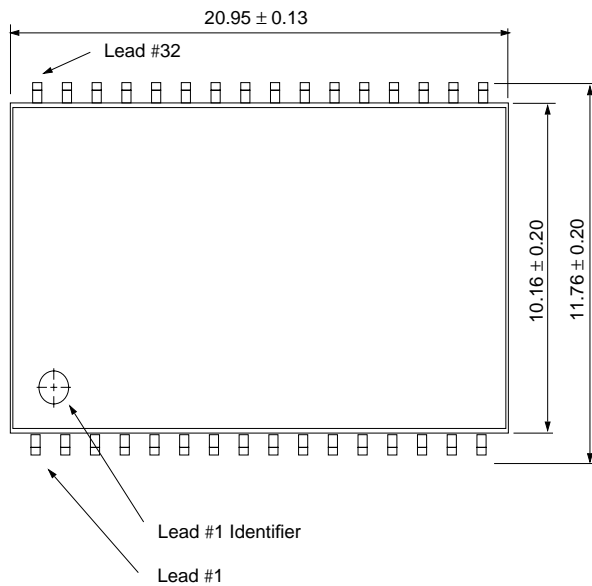
**Package Dimensions** (400 mil; 32 lead; Small Outline J-Lead)



**NOTE:** All dimensions are in millimeters. Reference JEDEC Standard MS-027



**Package Dimensions** (400mil; 32 lead; Thin Small Outline Package)



**NOTE:** All dimensions are in millimeters. Reference JEDEC Standard MS-024



IBM0165805B  
 IBM0165805P  
 8M x 8 12/11 EDO DRAM

## Revision Log

Revision	Contents of Modification
1/2/97	Initial specification release.
03/19/97	<ol style="list-style-type: none"> <li>1. <math>\overline{WE}</math> for the Hidden Refresh Write cycle in the Truth Table was changed from "H" to "L→H".</li> <li>2. <math>t_{OED}</math> was moved from the Common Parameters table to the Write Cycle Parameters Table.</li> <li>3. The note "Implementing <math>\overline{WE}</math> at <math>\overline{RAS}</math> time during a Read or Write cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs." was removed from all of the Read and Write timing diagrams.</li> <li>4. <math>t_{ODD}</math> was changed to <math>t_{OED}</math> in notes in the Write Cycle and Read Cycle Parameters tables.</li> <li>5. "Hyper Page Mode" was changed to "EDO (Hyper Page) Mode" in the timing diagram titles.</li> <li>6. Removed the Test Mode parameters and timing diagrams.</li> <li>7. LVTTL/LVCMOS changed to TTL/CMOS.</li> <li>8. LVCMOS currents were removed.</li> <li>9. Power numbers on the spec cover were recalculated.</li> </ol>
11/97	<ol style="list-style-type: none"> <li>1. Changed RetentionTime from 256ms to 128ms on Low Power DRAMs.</li> </ol>



© International Business Machines Corp.1997

Printed in the United States of America  
All rights reserved

IBM and the IBM logo are registered trademarks of the IBM Corporation.

This document may contain preliminary information and is subject to change by IBM without notice. IBM assumes no responsibility or liability for any use of the information contained herein. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. The products described in this document are not intended for use in implantation or other direct life support applications where malfunction may result in direct physical harm or injury to persons. **NO WARRANTIES OF ANY KIND, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE OFFERED IN THIS DOCUMENT.**

For more information contact your IBM Microelectronics sales representative or visit us on World Wide Web at <http://www.chips.ibm.com>

IBM Microelectronics manufacturing is ISO 9000 compliant.