Data Sheet | August 2000 | File Number 3039.2

Radiation Hardened 256 x 8 CMOS RAM

The HS-81C55/56RH are radiation hardened RAM and I/O chips fabricated using the Intersil radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

The HS-81C55/56RH is intended for use with the HS-80C85RH radiation hardened microprocessor system. The RAM portion is designed as 2048 static cells organized as 256 x 8. A maximum post irradiation access time of 500ns allows the HS-81C55/56RH to be used with the HS-80C85RH CPU without any wait states. The HS-81C55RH requires an active low chip enable while the HS-81C56RH requires an active high chip enable. These chips are designed for operation utilizing a single 5V power supply.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-96766. A "hot-link" is provided on our homepage for downloading. http://www.intersil.com/spacedefense/space.asp

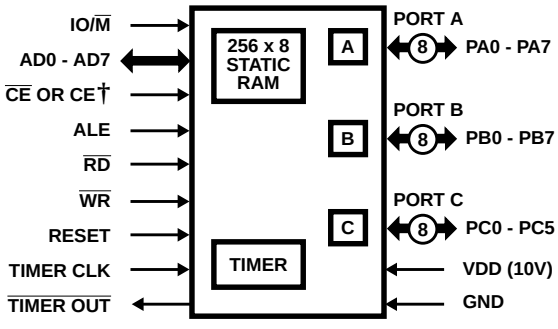
Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^{o}C)
5962R9676601QXC	HS1-81C55RH-8	-55 to 125
5962R9676601QYC	HS9-81C55RH-8	-55 to 125
5962R9676601VXC	HS1-81C55RH-Q	-55 to 125
5962R9676601VYC	HS9-81C55RH-Q	-55 to 125
5962R9676602QXC	HS1-81C56RH-8	-55 to 125
5962R9676602QYC	HS9-81C56RH-8	-55 to 125
5962R9676602VXC	HS1-81C56RH-Q	-55 to 125
5962R9676602VYC	HS9-81C56RH-Q	-55 to 125

Features

- Electrically Screened to SMD # 5962-96766
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Hardened EPI-CMOS
  - Total Dose . . . . . 100 krad(Si) (Max)
  - Transient Upset . . . . . >1 x 10^{8} rad(Si)/s
  - Latch-Up Free . . . . . >1 x 10^{12} rad(Si)/s
- Electrically Equivalent to Sandia SA 3001
- Pin Compatible with Intel 8155/56
- Bus Compatible with HS-80C85RH
- Single 5V Power Supply
- Low Standby Current . . . . . .200µA Max
- Low Operating Current 2mA/MHz
- Completely Static Design
- Internal Address Latches
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range . . . . . -55^{o}C to 125^{o}C

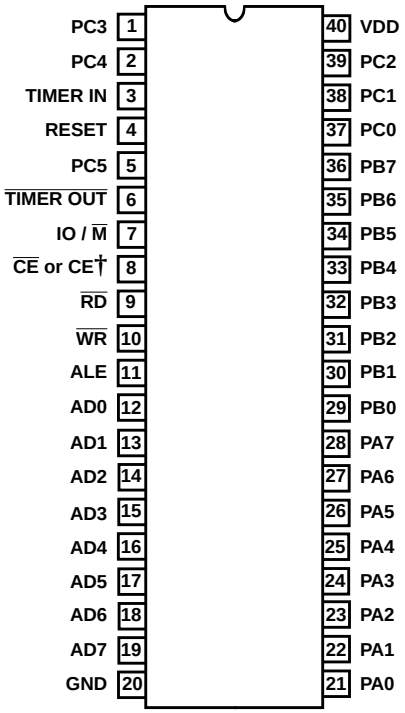
Functional Diagram



† 81C55RH = $\overline{CE}$
81C56RH = CE

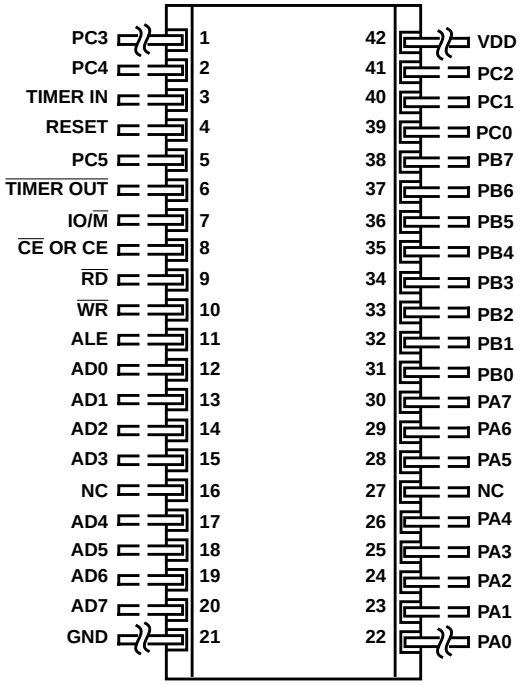
Pinouts

40 LEAD DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T40
TOP VIEW



† 81C55RH = $\overline{CE}$
81C56RH = CE

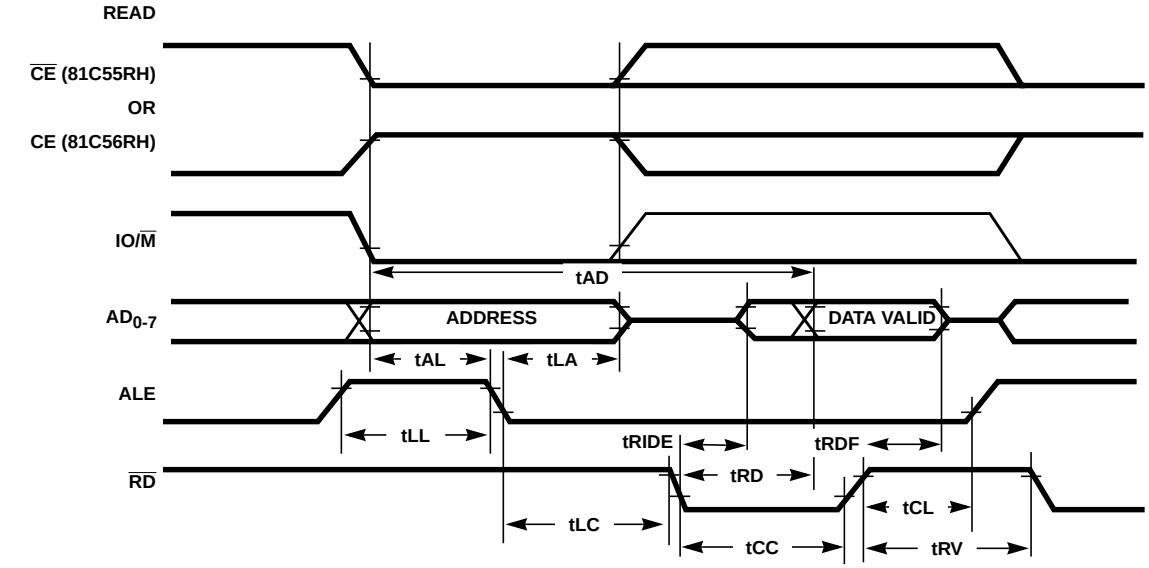
42 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
INTERSIL OUTLINE K42.A
TOP VIEW

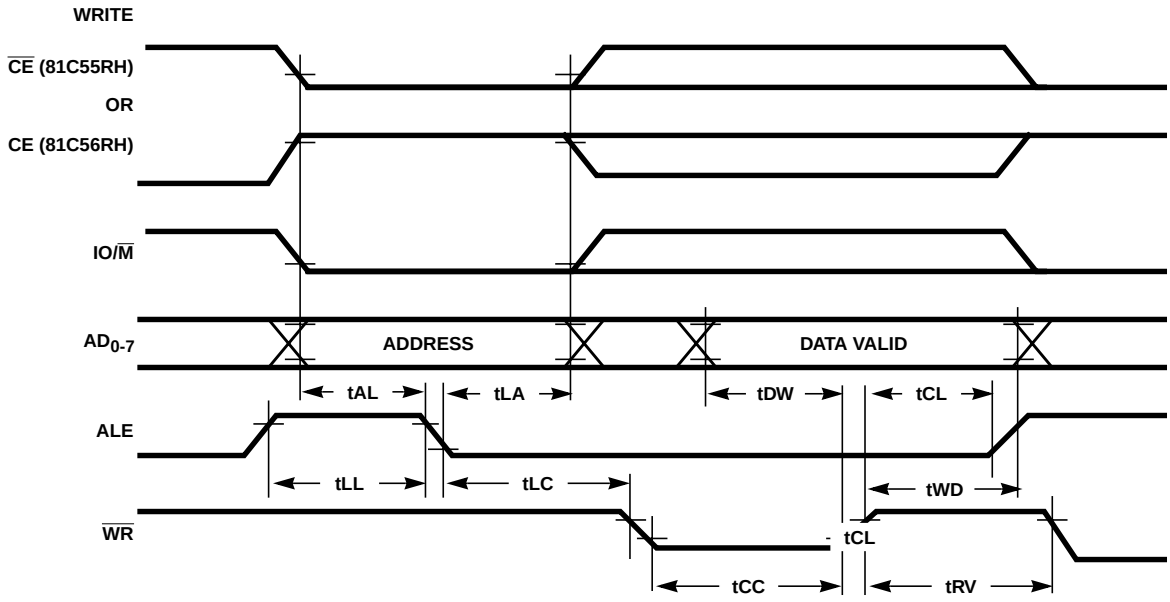


Pin Descriptions

SYMBOL	TYPE	NAME AND FUNCTION
RESET	I	**Reset:** Pulse provided by the HS-80C85RH to initialize the system (connect to HS-80C85RH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two HS-80C85RH clock cycle times.
AD0 - AD7	I/O	**Address/Data:** Three-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the HS-81C55 and HS-81C56RH on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
$\overline{CE}$ or CE	I	**Chip Enable:** On the HS-81C55RH, this pin is $\overline{CE}$ and is ACTIVE LOW. On the HS-81C56RH, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	I	**Read Control:** Input low on this line with the Chip Enable active enables and AD0 - AD7 buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$	I	**Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$.
ALE	I	**Address Latch Enable:** This control signal latches both the address on the AD0 - AD7 lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O Memory:** Selects memory if low and I/O and command/status registers if high.
PA0 - PA7 (8)	I/O	**Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB0 - PB7 (8)	I/O	**Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC0 - PC7 (8)	I/O	**Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC0 - PC5 are used as control signals, they will provide the following: PC0 - A INTR (Port A Interrupt) PC1 - ABF (Port A Buffer Full) PC2 - $\overline{A}$ $\overline{STB}$ (Port A Strobe) PC3 - B INTR (Port B Interrupt) PC4 - B BF (Port B Buffer Full) PC5 - $\overline{B}$ $\overline{STB}$ (Port B Strobe)
TIMER IN	I	**Timer Input:** Input to the counter-timer.
$\overline{TIMER\ OUT}$	O	**Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode.
VDD	I	**Voltage:** +5V.
GND	I	**Ground:** Ground reference.

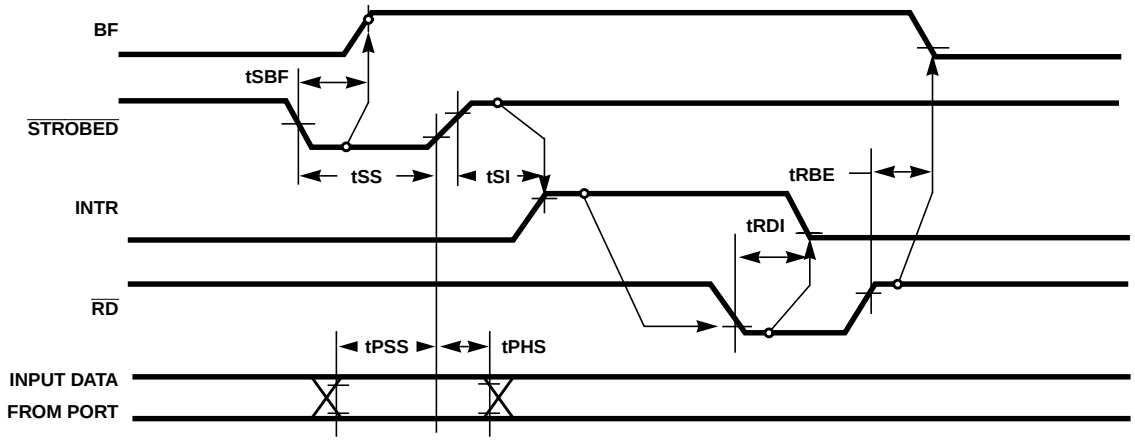
Waveforms


READ
CE (81C55RH)
OR
CE (81C56RH)
IO/M
tAD
AD0-7
ADDRESS
DATA VALID
tAL
tLA
ALE
tLL
tRIDE
tRDF
RD
tRD
tCL
tLC
tCC
tRV

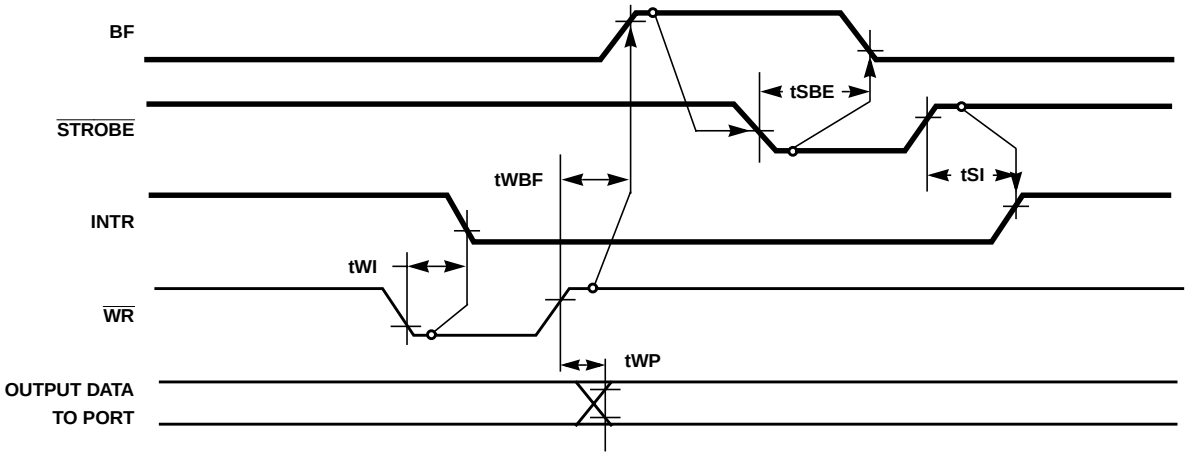

WRITE
CE (81C55RH)
OR
CE (81C56RH)
IO/M
AD0-7
ADDRESS
DATA VALID
tAL
tLA
tDW
tCL
ALE
tLL
tLC
tWD
WR
tCL
tCC
tRV

Waveforms (Continued)

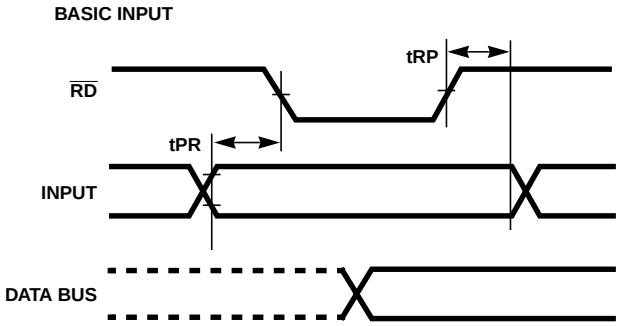
STROBED INPUT

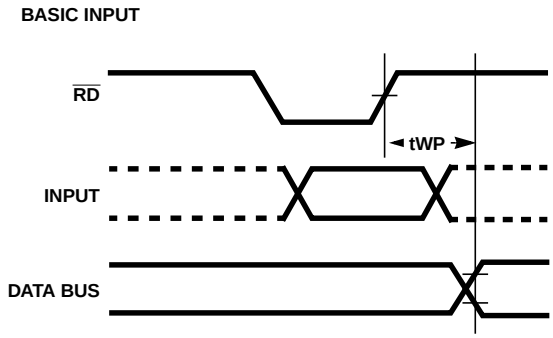


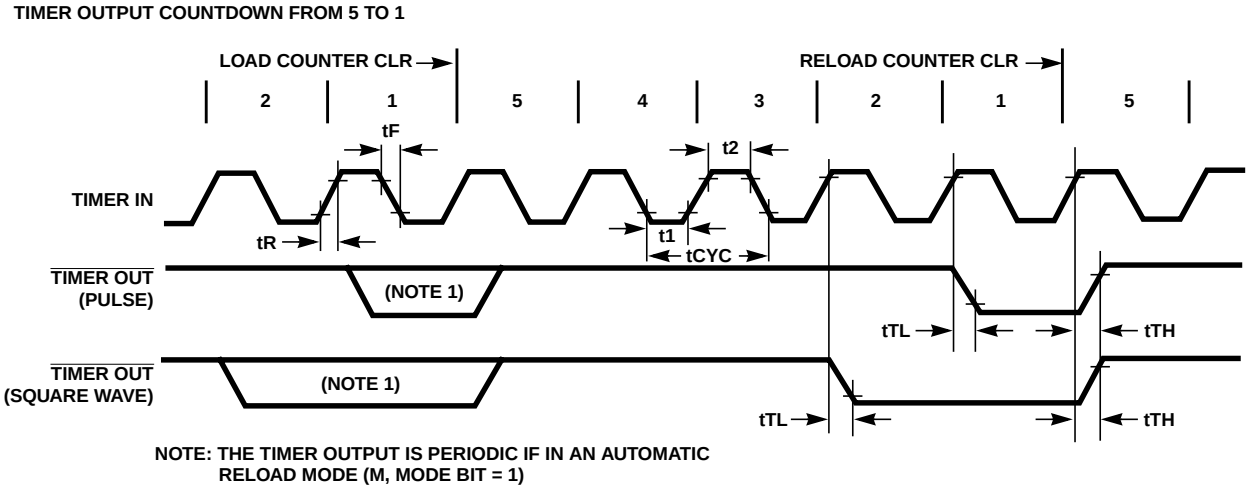
STROBED OUTPUT



Waveforms (Continued)







NOTE: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M, MODE BIT = 1)

Functional Description

The HS-81C55RH and 81C56RH contains the following:

- 2K Bit Static RAM Organized as 256 x 8
- Two 8-Bit I/O Ports (PA and PB) and One 6-Bit I/O Port (PC)
- 14-Bit Timer-Counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five register (Command, Status, PA0 - PA7, PB0 - PB7, PC0 - PC5) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input $\overline{CE}$ or CE and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

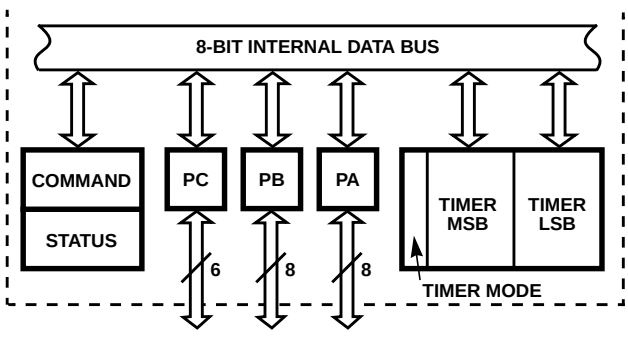


FIGURE 1. INTERNAL REGISTERS

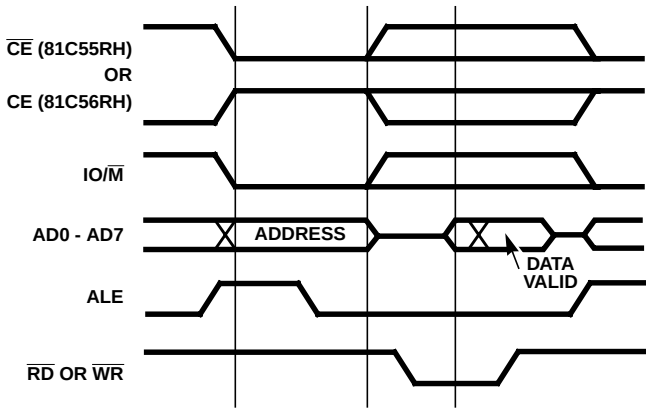


FIGURE 2. ON-BOARD MEMORY READ/WRITE CYCLE

Programming of the Command Register

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bit (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at anytime by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 3. The contents of the command register may never be read.

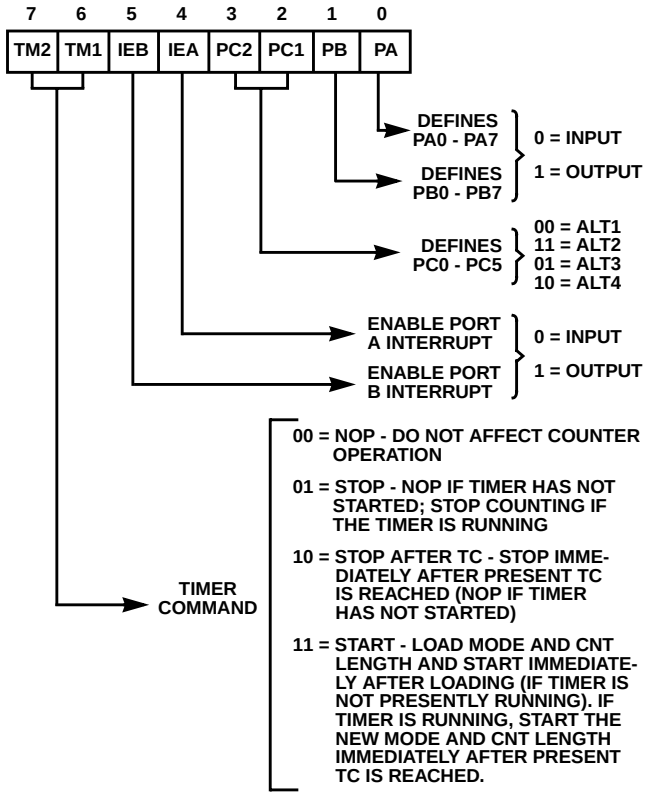


FIGURE 3. COMMAND REGISTER BIT ASSIGNMENT

Reading the Status Register

The status register consists of seven latches, one for each bit six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 4. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

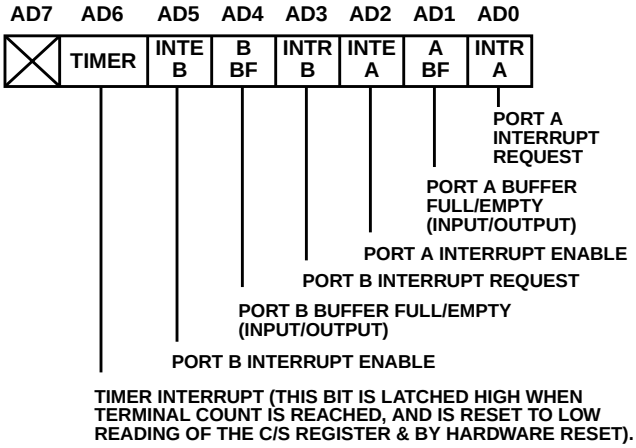


FIGURE 4. STATUS REGISTER BIT ASSIGNMENT

Input/Output Section

The I/O section of the HS-81C55RH and HS-81C56RH consists of five registers: (See Figure 5)

- **Command/Status Register (C/S)** - Both register are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are not accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD0 - AD7 lines.

- **PA Register** - This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). the I/O pins assigned in relation to this register are PA0 - PA7. The address of this register is XXXXX001.

- **PB Register** - This register functions the same as PA Register. the I/O pins assigned are PB0 - PB7. The address of this register is XXXXX010

- **PC Register** - This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as

control signals for PA and PB by properly programming the AD2 and AD3 bits of the C/S register.

When PC0 - PC5 is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an Interrupt that the HS-81C55RH and HS-81C56RH sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 1).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS†								
A7	A6	A5	A4	A3	A2	A1	A0	SELECTION
X	X	X	X	X	0	0	0	Interval Command/ Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	General Purpose I/O or Control Port C
X	X	X	X	X	1	0	0	Low-Order 8 Bits of Timer Count
X	X	X	X	X	1	0	1	High 6 Bits of Timer Count and 2 Bits of Timer Mode

† I/O Address must be qualified by CE = 1(81C56RH) or $\overline{CE}$ = 0(81C55RH) and IO/$\overline{M}$ = 1 in order to select the appropriate register.

X = Don't Care

FIGURE 5. I/O PORT AND TIMER ADDRESSING SCHEME

Figure 6 shows how I/O Ports A and B are structured within the HS-81C55RH and HS-81C56RH.

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the HS-81C55/56RH are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. the output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the HS-81C55/56RH is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT1 or ALT2 modes, the bits of Port C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

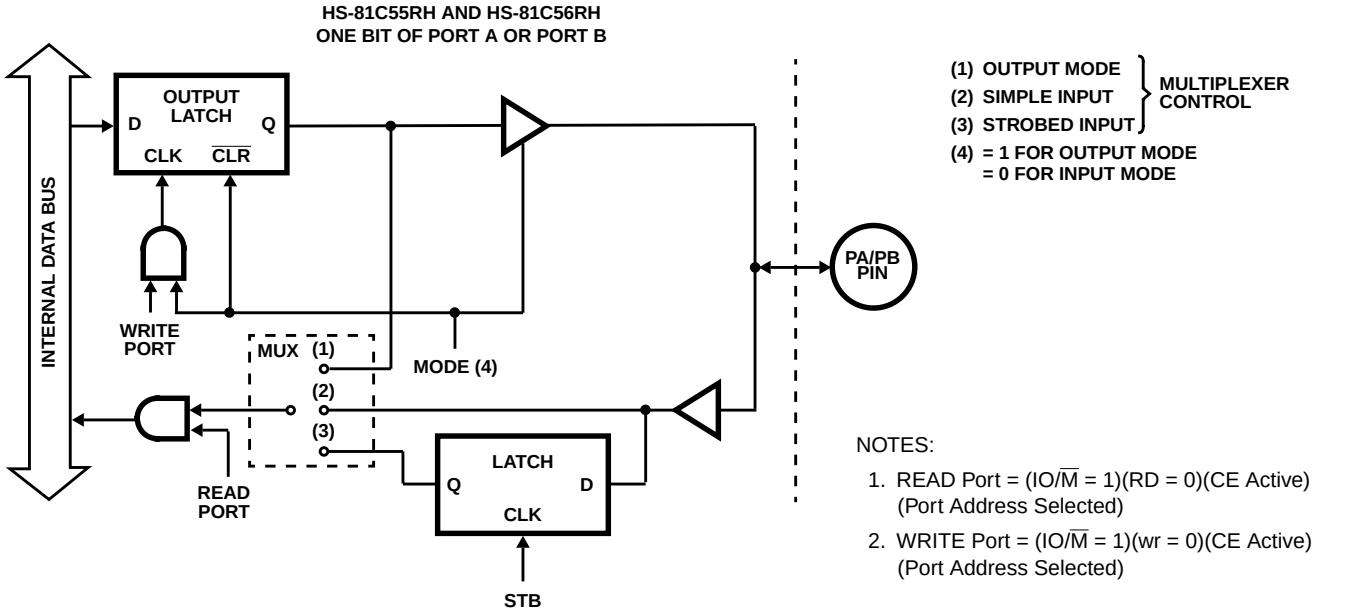


FIGURE 6. HS-81C55RH AND HS-81C56RH PORT FUNCTION

Figure 7 shows how the HS-81C55/56RH I/O ports might be configured in a typical system.

Timer Section

The timer is a 14-bit down counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 5).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 8). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

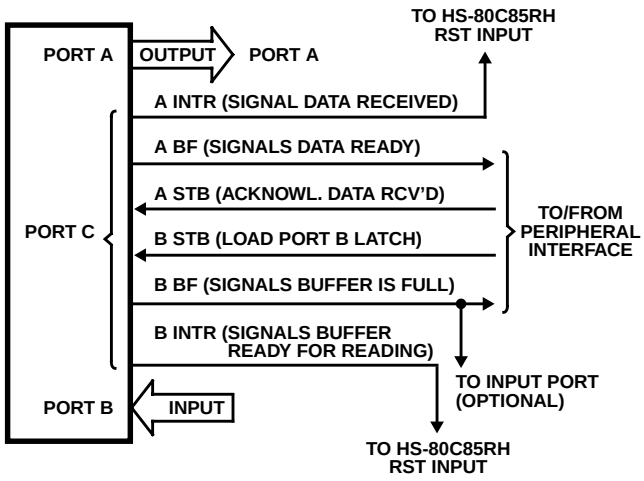


FIGURE 7. EXAMPLE: COMMAND REGISTER = 00111001

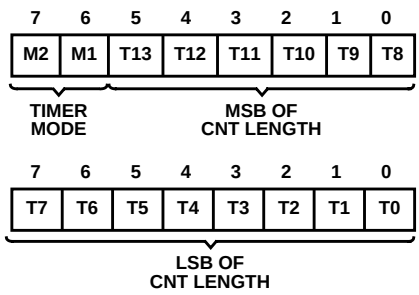


FIGURE 8. TIMER FORMAT

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

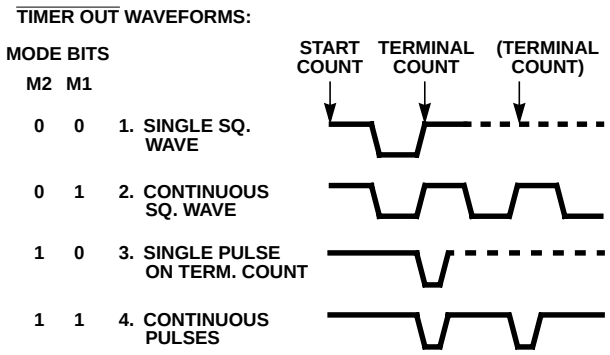


FIGURE 9. TIMER MODES

Bits 6-7 (TM2 and TM1) of command register contents are used to start and stop the counter. there are four commands to choose from:

TM2	TM1	
0	0	NOP - Do not affect counter operation
0	1	STOP-NOP - If timer has not started; stop counting if the timer is running
1	0	STOP AFTER TC - Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START - Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you *must* issue a START command to the counter. This applies even thought you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 10.

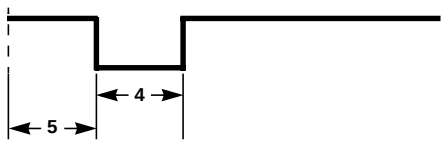


FIGURE 10. ASYMMETRICAL SQUARE-WAVE OUTPUT RESULTING FROM COUNT OF 9

The counter in the HS-81C55/56RH is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the HS-81C55/56RH chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the HS-80C85RH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count - 1 if full count is odd).

NOTE: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the HS-81C55/56RH always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

Die Characteristics

DIE DIMENSIONS:

222mils x 202mils x 14mils ± 1mil (Die Thickness)

INTERFACE MATERIALS:

Glassivation:

Type: SiO2
Thickness: 8kÅ ± 1kÅ

Top Metallization:

Type: AlSi
Thickness: 11kÅ ± 2kÅ

Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish:

Silicon

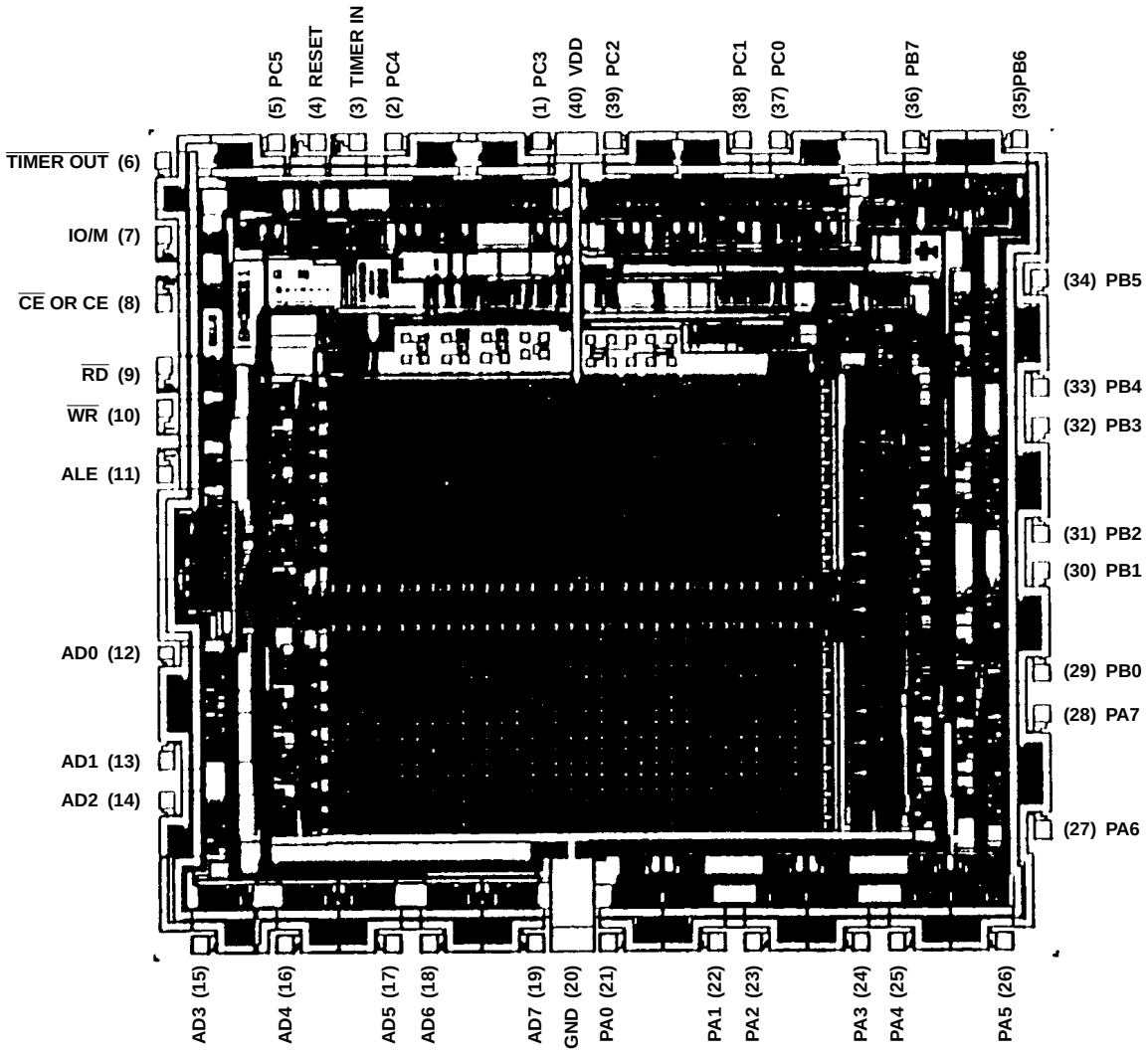
ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

Metallization Mask Layout

HS-81C55RH, HS-81C56RH



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.