



CMOS 12-Bit Buffered Multiplying DAC

ANALOG DEVICES INC.

AD7545A**1.1 Scope.**

This specification covers the detail requirements for a monolithic CMOS multiplying digital-to-analog converter with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to 12- and 16-bit microprocessor based systems. The AD7545A is an improved version of the AD7545 and will operate with any supply voltage from +5 V to +15 V.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number ¹
-1	AD7545AT(X)/883B
-2	AD7545AU(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	 -0.3 V, +17 V
Digital Input Voltage to DGND	 -0.3 V, $V_{DD} + 0.3$ V
V_{RFB} , V_{REF} to DGND	 +25 V
V_{PIN1} to DGND	 -0.3 V, $V_{DD} + 0.3$ V
AGND to DGND	 -0.3 V, $V_{DD} + 0.3$ V
Power Dissipation to $+75^\circ\text{C}$	 450 mW
Derates above $+75^\circ\text{C}$ by	 6 mW/ $^\circ\text{C}$
Operating Temperature Range	 -55°C to $+125^\circ\text{C}$
Storage Temperature	 -65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	 $+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 30^\circ\text{C}/\text{W}$ for Q-20 and E-20A
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-20 and E-20A

Table 1.

Test	Symbol	Device	Design Limit T_{min}/T_{max}	Sub Group 1	Sub Group 2, 3	Test Conditions/Comments $V_{DD} = +5\text{ V}$	Units
Resolution	RES	-1, 2	12				Bits
Relative Accuracy	RA	-1, 2	1/2	1/2	1/2		±LSB max
Differential Nonlinearity	DNL	-1, 2	1	1	1	12-Bit Monotonic T_{min} to T_{max}	±LSB max
Gain Error ²	A_E	-1	4	3	4	DAC Register Loaded with 1111 1111 1111	±LSB max
		-2	2	1	2		
Gain Tempco	TC_{AE}	-1, 2	5				±ppm/°C max
Power Supply Rejection	PSRR	-1, 2	0.004	0.002	0.004	$V_{DD} = \pm 5\%$	±%/ % max
Output Leakage Current	OUT1	-1, 2	200	10	200	DB0-DB11 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V	±nA max
Output Current Settling Time	t_{SL}	-1, 2	1			To +1/2 LSB; OUT1 Load = 100 Ω , DAC Output Measured from Falling Edge of $\overline{WR}$, $\overline{CS}$ = 0 V	µs max
Feedthrough Error	FT	-1, 2	10				mV p-p max
Reference Input Resistance Pin 19 to Ground	R_{IN}	-1, 2	10	10	10		k min
			20	20	20		k max
Digital Input High Voltage	V_{IH}	-1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{IL}	-1, 2	0.8	0.8	0.8		V max
Digital Input Leakage Current	I_{IN}	-1, 2	10	1	10	$V_{IN} = 0\text{ V or }V_{DD}$	±µA max
Digital Input Capacitance	C_{IN}	-1, 2	8			DB0-DB11; $\overline{WR}$, $\overline{CS}$	pF max
			15				
Output Capacitance	C_{OUT1}	-1, 2	70			DB0-DB11 = 0 V, $\overline{WR}$, $\overline{CS}$ = 0 V	pF max
			150			DB0-DB11 = V_{DD} ; $\overline{WR}$, $\overline{CS}$ = 0 V	
Chip Select to Write Setup Time ³	t_{CS}	-1, 2	170			$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	ns min
Chip Select to Write Hold Time ³	t_{CH}	-1, 2	0				
Write Pulse Width ³	t_{WR}	-1, 2	170				
Data Setup Time ³	t_{DS}	-1, 2	150				
Data Hold Time ³	t_{DH}	-1, 2	5				
Supply Current from V_{DD}	I_{DD}	-1, 2	2	2	2	All Digital Inputs V_{IL} or V_{IH}	mA max
			100	100	100	All Digital Inputs 0 or V_{DD}	µA max

NOTES

¹ $V_{OUT1} = 0\text{ V}$, $V_{REF} = +10\text{ V}$, AGND = DGND unless otherwise stated.²Measured using internal feedback resistor.³Timing per Figure 1.

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Table 2.

Test	Symbol	Device	Design Limit T_{min}/T_{max}	Sub Group 1	Sub Group 2, 3	Test Conditions/Comments $V_{DD} = +15\text{ V}$	Units
Resolution	RES	-1, 2	12				Bits
Relative Accuracy	RA	-1, 2	1/2	1/2	1/2		$\pm$ LSB max
Differential Nonlinearity	DNL	-1, 2	1	1	1	12-Bit Monotonic T_{min} to T_{max}	$\pm$ LSB max
Gain Error ²	A_E	-1	4	3	4	DAC Register Loaded with 1111 1111 1111	$\pm$ LSB max
		-2	2	1	2		
Gain Tempco	TC_{AE}	-1, 2	5				$\pm$ ppm/ $^{\circ}\text{C}$ max
Power Supply Rejection	PSRR	-1, 2	0.004	0.002	0.004	$V_{DD} = \pm 5\%$	$\pm$ %/% max
Output Leakage Current	OUT1	-1, 2	200	10	200	DB0-DB11 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V	$\pm$ nA max
Output Current Settling Time	t_{SL}	-1, 2	1			To +1/2 LSB; OUT1 Load = 100 Ω , DAC Output Measured from Falling Edge of $\overline{WR}$.	μs max
Feedthrough Error	FT	-1, 2	10				mV p-p max
Reference Input Resistance Pin 19 to Ground	R_{IN}	-1, 2	10	10	10		k min
			20	20	20		k max
Digital Input High Voltage	V_{IH}	-1, 2	13.5	13.5	13.5		V min
Digital Input Low Voltage	V_{IL}	-1, 2	1.5	1.5	1.5		V max
Digital Input Leakage Current	I_{IN}	-1, 2	10	1	10	$V_{IN} = 0\text{ V or }V_{DD}$	$\pm$ μA max
Digital Input Capacitance	C_{IN}	-1, 2	8			DB0-DB11; $\overline{WR}$, $\overline{CS}$	pF max
Output Capacitance	C_{OUT1}	-1, 2	70			DB0-DB11 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V	pF max
			150			DB0-DB11 = V_{DD} ; $\overline{WR}$, $\overline{CS}$ = 0 V	
Chip Select to Write Setup Time ³	t_{CS}	-1, 2	95			$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	ns min
Chip Select to Write Hold Time ³	t_{CH}	-1, 2	0				
Write Pulse Width ³	t_{WR}	-1, 2	95				
Data Setup Time ³	t_{DS}	-1, 2	80				
Data Hold Time ³	t_{DH}	-1, 2	5				
Supply Current from V_{DD}	I_{DD}	-1, 2	2	2	2	All Digital Inputs V_{IL} or V_{IH}	mA max
			100	100	100	All Digital Inputs 0 or V_{DD}	μA max

NOTES

¹ $V_{OUT1} = 0\text{ V}$, $V_{REF} = +10\text{ V}$, AGND = DGND unless otherwise stated.

²Measured using internal feedback resistor.

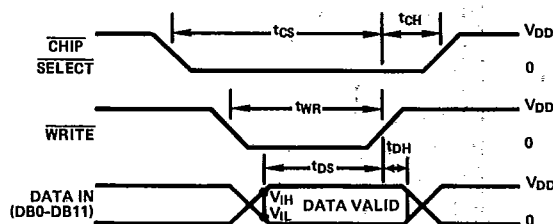
³Timing per Figure 1.


Figure 1. Write Cycle Timing Diagram

MODE SELECTION

WRITE MODE:

CS and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.

HOLD MODE:

Either CS or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or CS assumed high state.

NOTES:

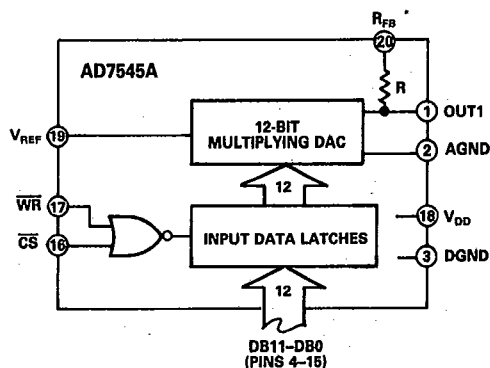
 $V_{DD} = +5\text{ V}$; $t_r = t_f = 20\text{ ns}$
 $V_{DD} = +15\text{ V}$; $t_r = t_f = 40\text{ ns}$

All input signal rise and fall times measured from 10% to 90% of V_{DD} .

Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

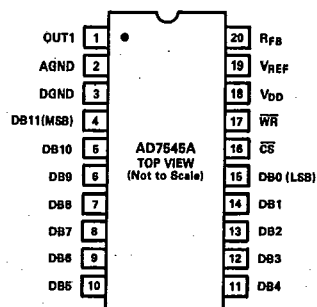
3.2.1 Functional Block Diagram and Terminal Assignments.

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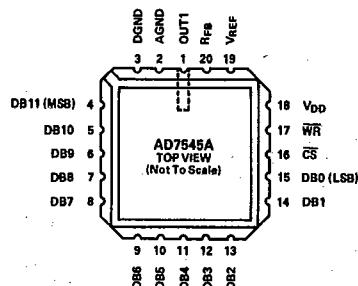


Pin Assignments

Cerdip (Q)



LCC (E)



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883, Method 1005. Burn-in is per MIL-STD-883 Method 1015, Test Condition (B).

